U6209B-FFP

Frequency Synthesizer for TV Tuner

Features

- 1.3 GHz divide-by-8 prescaler integrated (can be bypassed)
- 15 bit counter accepts input frequencies up to 170 MHz
- Programable reference divider: divide by 512 or 1024
- P-controlled by I²C-Bus (MC44818 data format compatible)
- 5 port outputs (open collector)
- 4 addresses selectable at Pin 10 for multituner application
- 31.25 kHz (-1.3 GHz) / 3.90625 kHz (-170 MHz) tuning steps with 4MHz Xtal
- Electrostatic protection according to MILSTD 883
- SO16 small package

Package: SO16

Block Diagram

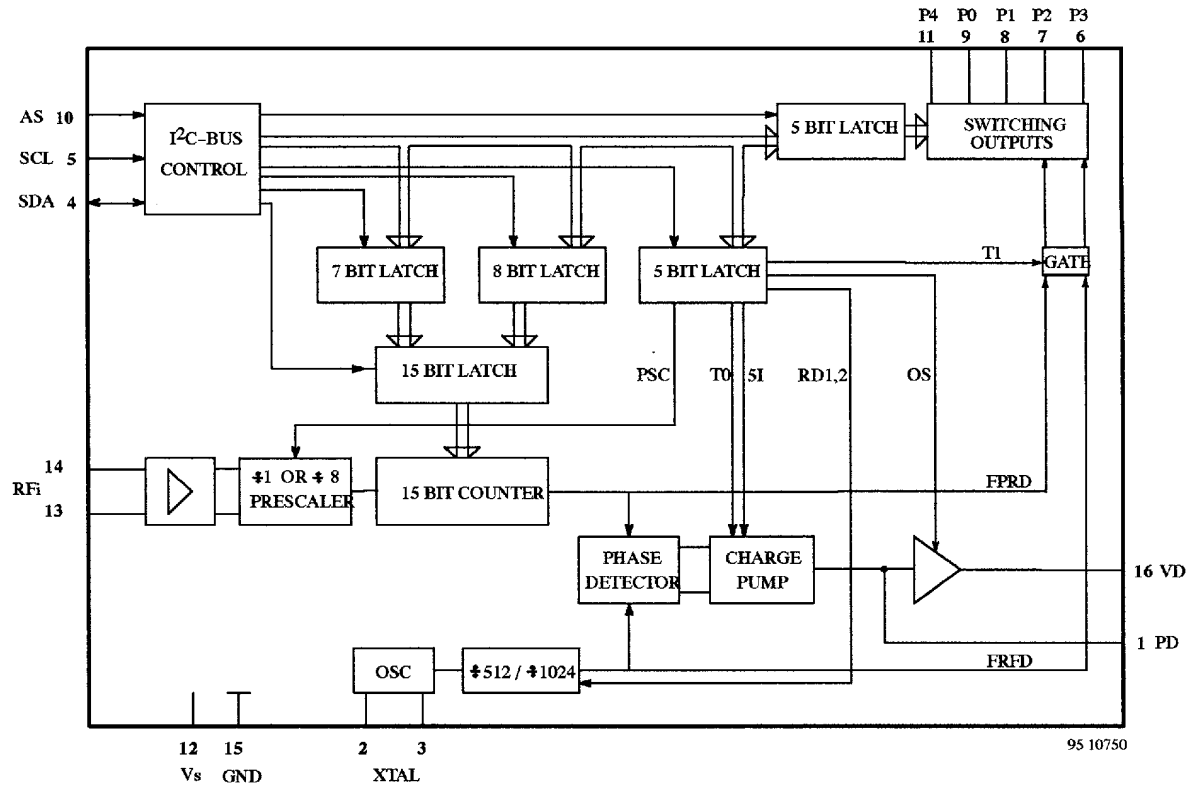

Figure 1.

Pin Configuration

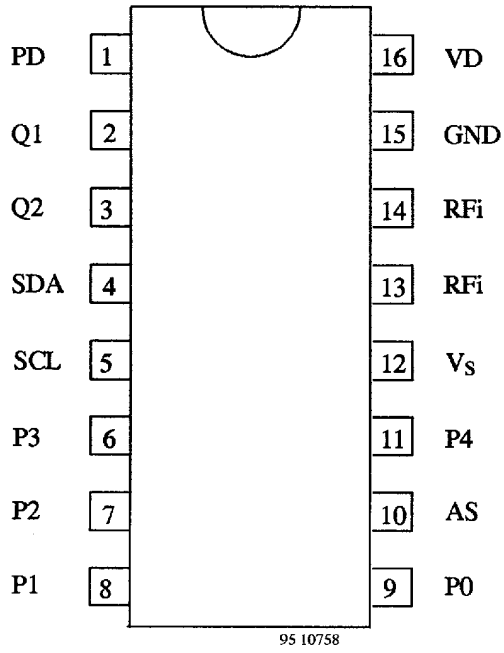

Figure 2.

Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data in/output
5	SCL	Clock
6	P3	Port output (open collector)
7	P2	Port output (open collector)
8	P1	Port output (open collector)
9	P0	Port output (open collector)
10	AS	Address select input
11	P4	Port output (open collector)
12	Vs	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output

Description

The U6209B is a single chip PLL designed for TV and VCR receiver systems. It consists of an bridgeable divide-by-8 prescaler with an integrated preamplifier, a 15bit programmable divider, a crystal oscillator and a reference divider with two selectable divider ratios (512 / 1024), a phase/frequency detector together with a charge-pump, which is driving the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via I^2C-bus format. There are four programmable addresses selectable, programmed by applying a specific input voltage to the address select input, enabling the use of up to four synthesizers in a system. Five open collector outputs for port functions are included, which are capable of sinking at least 10mA.

Functional Description

The U6209B is programmed via 2-wire I^2C bus data format. The three bus inputs pin 4,5,10 are used as *SDA*, *SCL* and *address select* inputs. The data includes the scaling factor SF (15bit) and port output information. There are some additional functions for testing of the device included.

Oscillator frequency calculation:

fvco = PSF * SF * frefosc / 1024

fvco: Locked frequency of voltage controlled oscillator
PSF : Scaling factor of prescaler (1 or 8)
SF : Scaling factor of programmable 15-bit-divider
frefosc :Reference oscillator frequency:
3.2/ 4 MHz crystal or external reference frequency

In addition there are port outputs available for band-switching and other purposes.

Application

A typical application is shown on page 11. All input / output interface circuits are shown on page 10.

Some special features which are related to test- and alignment procedures for tuner production are explained together within the following I^2C bus mode description.

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15).

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	Vs	-0.3		6	V
RF input voltage	Pins 13,14	RFi	-0.3		Vs+0.3	V
Xtal input voltage	Pin 2	Q1	-0.3		Vs+0.3	V
Charge pump output voltage	Pin 1	PD	-0.3		Vs+0.3	V
Active filter output voltage	Pin 16	VD	-0.3		Vs+0.3	V
Bus input/output voltage	Pin 4	VSDA	-0.3		6	V
	Pin 5	VSCL	-0.3		6	V
SDA output current	Open collector Pin 4	ISDA	-1		5	mA
Address select voltage	Pin 10	VAS	-0.3		Vs+0.3	V
Port output currentopen collector	Pins 6-9,11	P0-4	-1		15	mA
Total port output currentopen collector	Pins 6-9,11	P0-4	-1		50	mA
Port output voltagein off state		P0-4	-0.3		15	V
in on state	Pins 6-9,11		-0.3		6	V
Junction temperature		Tj	-40		125	°C
Storage temperature		Tstg	-40		125	°C

Operating Range

All voltages are referred to GND (Pin 15).

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	Vs	4.5		5.5	V
Ambient temperature		T_{amb}	0		70	C
Input frequency	PSC = 1 Pins 13,14	RFi	64		1300	MHz
Input frequency	PSC = 0 Pins 13,14	RFi	1		170	MHz
Progr. divider		SF	256		32767	
Xtal oscillator	Pin 2	fXTAL	3	4	4.48	MHz

Thermal Resistance

Parameters	Symbol	Value	Unit
SO16 small	RthJA	110	K/W

Electrical Characteristics

Test Conditions (unless otherwise specified) : Vs = 5V, Tamb = 25 C.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (prescaler on)	SW 0–4 = 0 ; PSC =1 Pin 12	Is	32	42	52	mA
(prescaler off)	SW 0–4 = 0 ; PSC =0 Pin 12	Is	22	28	35	mA
Input sensitivity						
fi = 80 - 1000 MHz	PSC = 1 Pin 13	Vi 1)	10		315	mVrms
fi = 1300 MHz	PSC = 1 Pin 13	Vi 1)	40		315	mVrms
fi = 10 - 170 MHz	PSC = 0 Pin 13	Vi 1)	10		315	mVrms
Port outputs (open collector)	P0–4 Pins 6–9,11					
Leakage current	VH = 13.5 V	IL			10	uA
Saturation voltage	IL = 10 mA	VSL 2)			0.5	V
Charge pump output		PD				
Charge pump current 'H'	5I = 1 , VPD = 2V Pin 1	IPDH		180		uA
Charge pump current 'L'	5I = 0 , VPD = 2V Pin 1	IPDL		50		uA
Charge pump leakage current	T0 = 0,VPD = 2V Pin 1	IPDTRI		5		nA
Charge pump amplifier gain	Pins 1, 16			6400		
Bus inputs		SDA,SCL				
Input voltage high	Pins 4,5	Vi 'H'	3		5.5	V
Input voltage low	Pins 4, 5	Vi 'L'			1.5	V
Input current high	Vi 'H' =Vs Pins 4, 5	Ii 'H'			10	uA
Input current low	Vi 'L' = 0 V Pins 4,5	Ii 'L'	- 20			uA
Output voltage SDA(open collector)	ISDA 'L' = 2 mA Pin 4	VSDA 'L'			0.4	V
Address selection		AS				
Input current	VAS "H" = Vs Pin 8 VAS "L" = 0 V Pin 8	IiAS "H" IiAS "L"	 - 100		10	uA
Bus timing						
Rise time SDA, SCL		tR			15	us
Fall time SDA, SCL		tF			15	us
Clock frequency SCL		fSCL	0		100	kHz
Clock "H" Pulse		tHIGH	4			us
Clock "L" Pulse		tLOW	4			us
Hold time start		tHSTA	4			us
Waiting time start		tWStt	4			us
Set up time start		tSSTT	4			us
Set-up time stop		tSSTO	4			us
Set-up time data		tSDAT	0.3			us
Hold time data		tHDAT	0			us

Notes:
1) RMS-voltage calculated from the measured available power on 50 Ω
2) Tested with one switch active

I²C - Bus Description

The U6209B is controlled via 2-wire I²C-bus format by feeding data and clock signals into the SDA and SCL lines respectively. The table 'I²C-BUS DATA FORMAT' describes the format of the data and shows how to select the device address by applying a voltage at pin 10. When the correct address byte is received, the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. The table 'I²C-BUS PULSE DIAGRAM' shows some possible data transfer examples.

Programmable divider bytes PDB1 and PDB2 are stored in a 15 bit latch and are controlling the division ratio of the 15 bit programmable divider. The control Byte CB1 allows to control the following special functions:5I-bit switches between low and high charge pump current

- T1-bit enables divider test mode when it is set to logic 1
- T0-bit allows to disable the charge pump when it is set to logic 1
- RD1 and RD2-bit allow to select the reference divider ratio
- PSC-bit switches prescaler off when it is set to logic 0
- OS-bit disables the charge pump drive amplifier output when it is set to logic 1.

When T1 is set to logic 1 then the programmable divider output signal is switched to pin7 and the reference divider output signal is switched to pin6. The OS-bit function disables the complete PLL function. This allows tuner alignment by supplying the tuning voltage directly via the 30V supply voltage of the tuner. The control byte CB2 programs the port outputs P0-4; a logic 0 for high impedance output (off) and a logic 1 for low impedance output (on).

Description	Data Format								
	MSP							LSB	
Address byte	1	1	0	0	0	AS1	AS2	0	A
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	X	X	PSC	OS	A
Control byte 2	X	X	X	P4	P3	P2	P1	P0	A

A = Acknowledge ; X = not used ; Unused bits of controlbyte 2 should be 0 for lowest power consumption

n0..n14 :	Scaling factor (SF)	SF = 16384*n14 + 8192*n13 + ... + 2*n1 + n0	
PSC :	Prescaler on / off	PSC = 1 : prescaler on (PSF = 8)	
		PSC = 0 : prescaler off (PSF = 1)	
T0, T1 :	Testmode selection	T1 = 1 : divider test mode on	T1 = 0 : divider test mode off
		T0 = 1 : charge pump disable	T0 = 0 : charge pump enable
P0-4:	Port outputs	P0-4 = 1: open collector active	
5I :	Charge pump current switch	5I = 1 : high current	5I = 0 : low current
OS :	Output switch	OS = 1 : varicap drive disable	OS = 0 : varicap drive enable

RD1,RD2 : Reference divider selection

RD2	RD1	Reference divider ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

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AS1	AS2	Address	Hex. value	Dec. Value	Voltage at Pin 10
0	1	1	C2	194	open
0	0	2	C0	192	0 to 10% Vs
1	0	3	C4	196	40 to 60% Vs
1	1	4	C6	198	90 to 100% Vs

Pulse Diagram

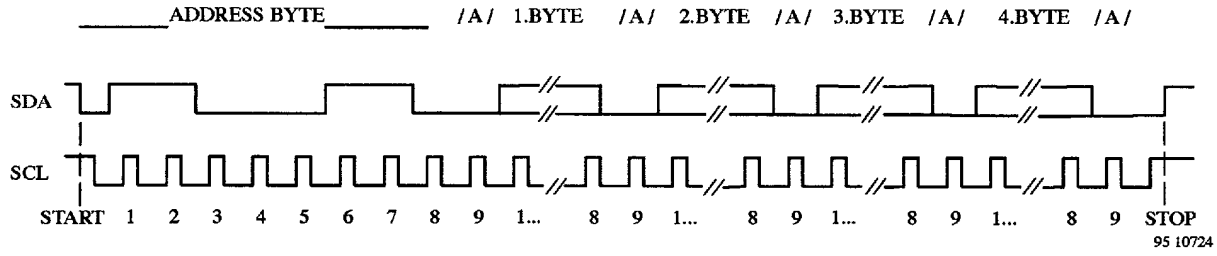

Figure 3.

Data transfer examples

START - ADR - PDB1 - PDB2 - CB1 - CB2 - STOP
START - ADR - CB1 - CB2 - -PDB1 - PDB2 - STOP
START - ADR - PDB1 - PDB2 - CB1 - STOP
START - ADR - CB1 - CB2 - PDB1 - STOP
START - ADR - PDB1 - PDB2 - STOP
START - ADR - CB1 - CB2 - STOP
START - ADR - CB1 - STOP

Description

START= Start condition
ADR= Address byte
PDB1= Progr.divider byte 1
PDB2= Progr. divider byte 2
CB1= Control byte 1
CB2= Control byte 2
STOP= Stop condition

Bus Timing

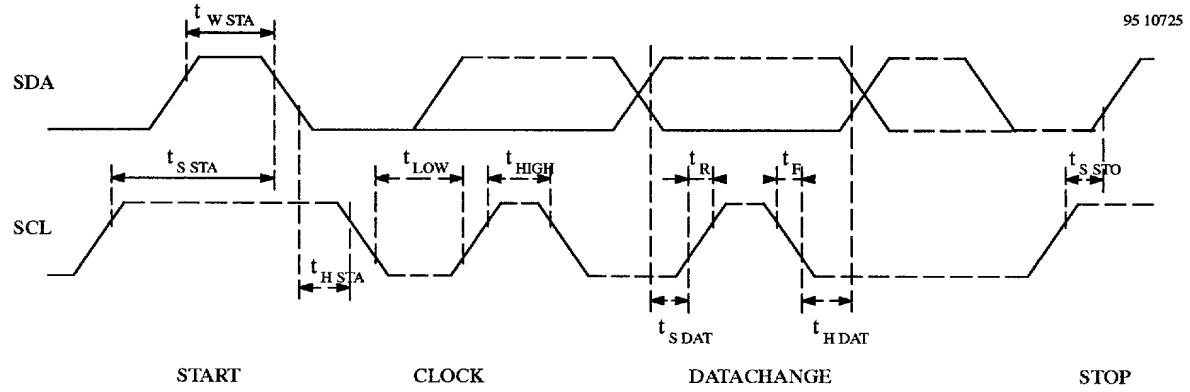

Figure 4.

tS STT	- Set - up time start	tS DAT	- Set - up time data
tW STT	- Waiting time start	tH DAT	- Hold time data
tH STT	- Hold time start	tS STO	- Set - up time stop
tLOW	- "L" - Pulse width clock	tR	- Rise time
tHIGH	- "H" - Pulse width clock	tF	- Fall time

Typical Prescaler Input Sensitivity (Prescaler on: PSC = 1) :

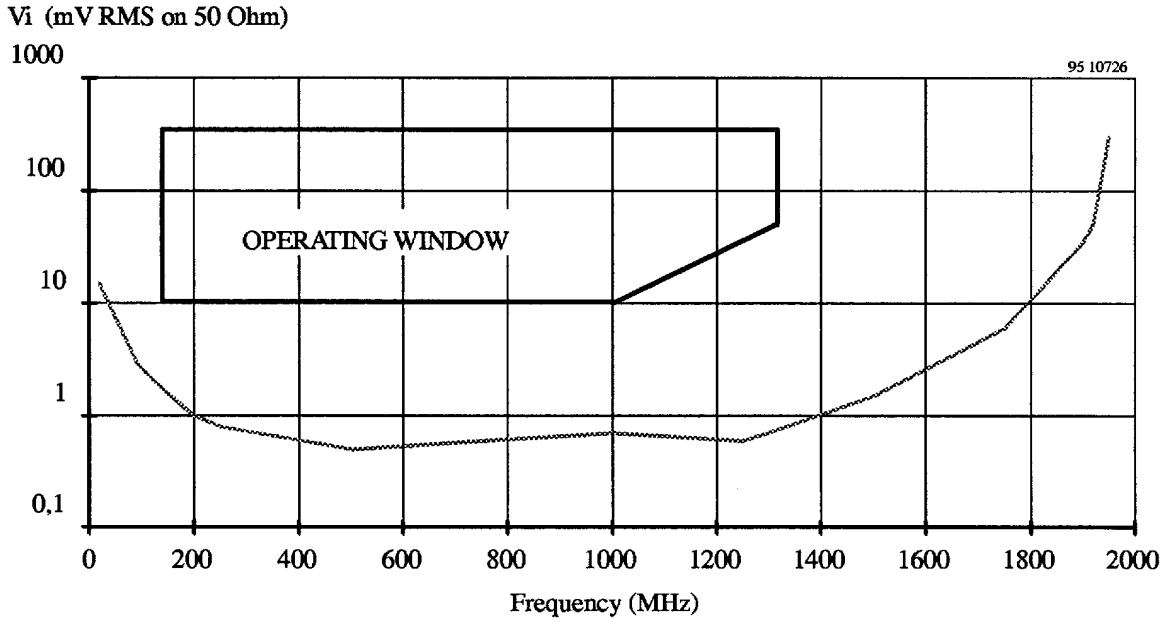

Figure 5.

Typical Prescaler Input Sensitivity (Prescaler off: PSC = 0) :

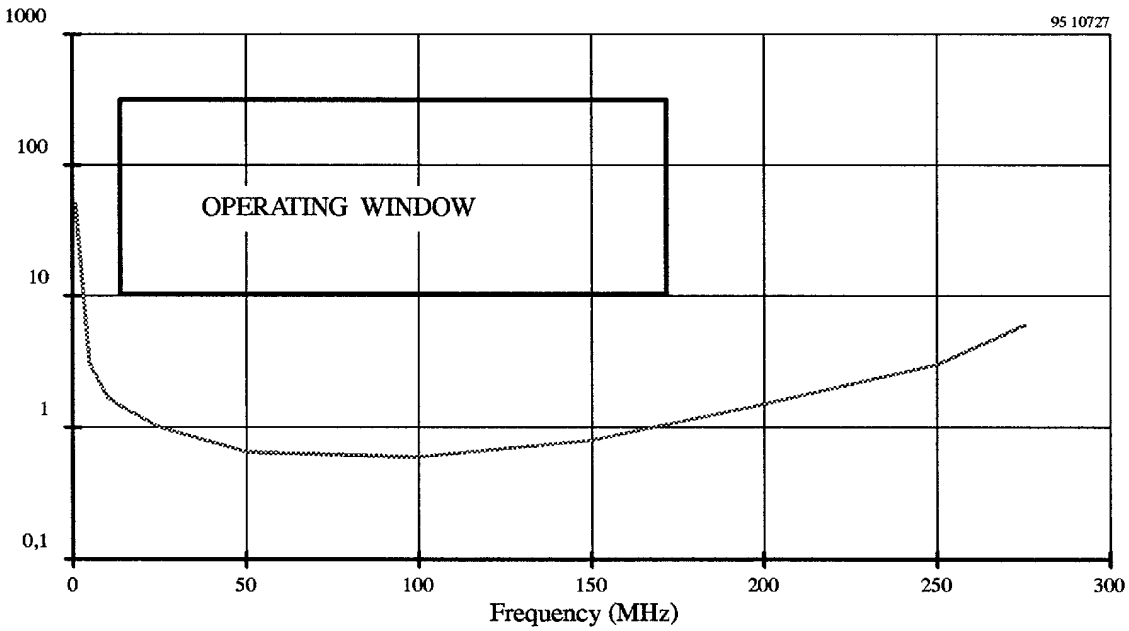

Figure 6.

Input/Output Interface Circuits

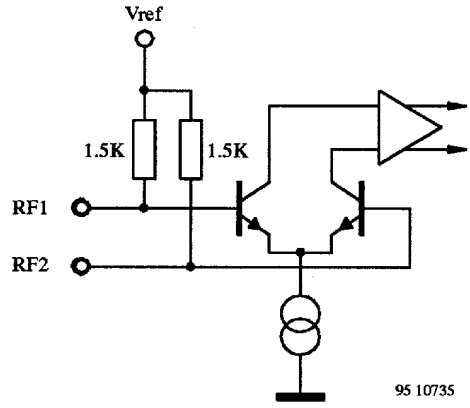

Figure 7. RF input

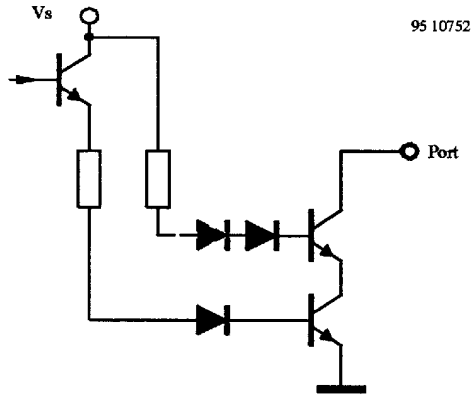

Figure 10. Ports

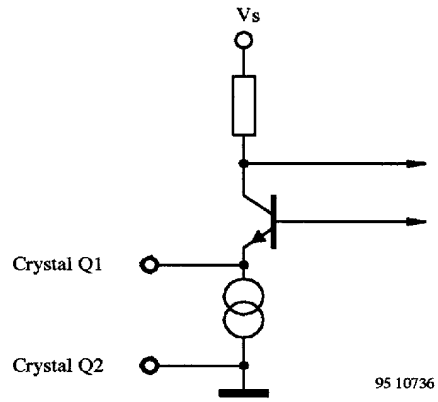

Figure 8. Reference oscillator

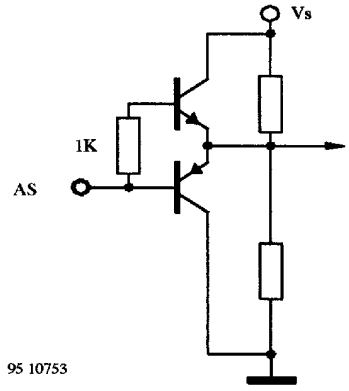

Figure 11. Address select input

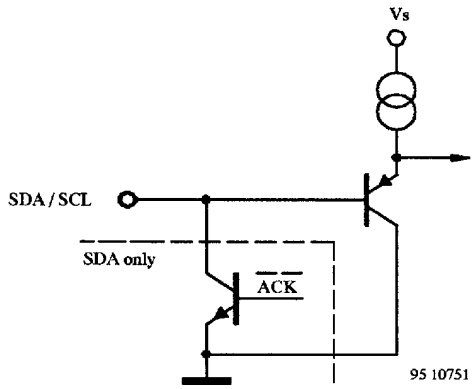

Figure 9. SCL and SDA input

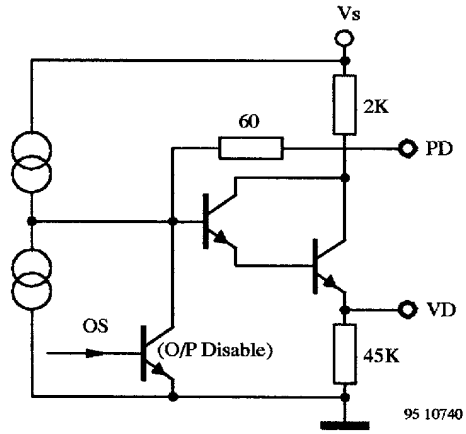

Figure 12. Loop amplifier

Application Circuit

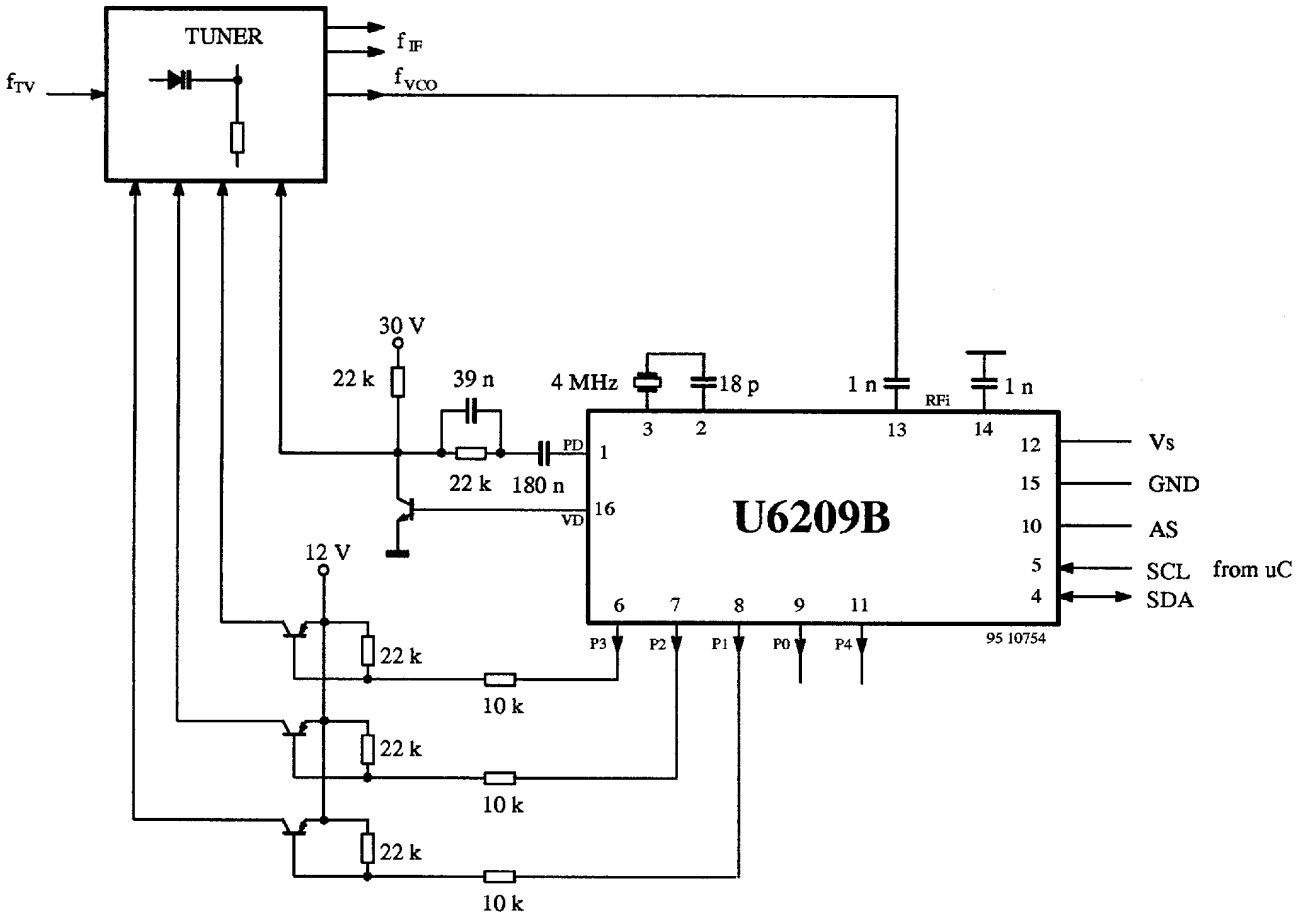

Figure 13.

Dimensions in mm

Package: SO16