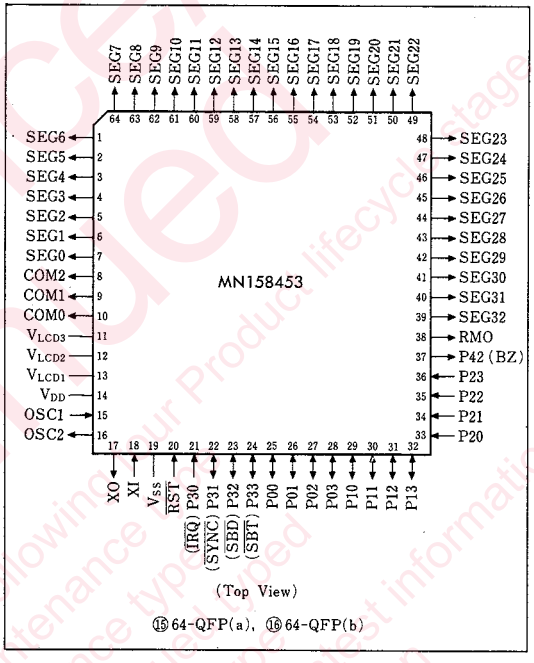
MN158453

■ Features

- ROM capacity: 4,096 × 8 bits
- RAM capacity: 256 × 4 bits
- Machine cycle: 8 μs(2.5 to 5.5 V), 2 μs(4.5 to 5.5 V)
- Interrupt: External interrupt 1, Timer interrupt 1, Serial interrupt 1
- Timer/counter:Timer and event count functions provided by 8-bit programmable timer with 7-bit prescaler
- Serial interface: 8-bit synchronous type
- LCD driver circuit incorporated: 3 Commons, 33 segments(max.)
- Time base generator circuit incorporated: 2 Hz, 64 Hz
- 8-bit preset counter circuit incorporated: Interrupt allowed with an overflow signal
  (Clock source: OSC/128, XI/128)
- Remote control carrier output circuit incorporated: 1/8 fosc, 1/12 fosc
  1/6 fosc, 1/16 fosc
  (1/2, 1/3 duty)
- Buzzer driver circuit incorporated: 2 kHz, 4 kHz
- Back up mode: STOP/HALT mode
- Operating voltage range: 2.2 to 5.5 V
- I/O pins: 8 for general purpose output or I/O
  8 for general purpose input
  1 for serial data I/O
  1 for serial clock I/O
  1 for buzzer output
  1 for remote control carrier output
  3 for LCD drive Common output
  33 for LCD drive segment output
- Process: Silicon gate CMOS
- Package: 64-QFP
- Piggyback: EP158453

■ Pin Configuration



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■ Pin Descriptions

Pin	Symbol	Pin name	I/O	Description
14 19	V_{DD} V_{SS}	Power supply pin	I	Connect +2.5-5.5 V to V_{DD}, and 0 V to V_{SS}.
13 12 11	V_{LCD1} V_{LCD2} V_{LCD3}	LCD power supply pin	I	LCD drive power supply pin. $V_{LCD1}=V_{DD}-(1/3)$ $V_{LCD2}=V_{DD}-(2/3)V_{LCD}$, $V_{LCD3}=V_{DD}-V_{LCD}$ (V_{LCD}:LCD drive voltage)
15 16	OSC1 OSC2	Clock input Clock output	I O	Oscillation pins to connect f_{osc} ceramic oscillator or crystal oscillator. A feedback resistor is incorporated between OSC1 and OSC2.
18 17	XI XO	Clock input Clock output	I O	Oscillation pins to connect a crystal oscillator(32.768 KHz)for time base. A feedback resistor between XI and XO can be specified with a mask option.
20	$\overline{RST}$	Reset input	I	Reset is apllied if the "L" level is inputted over 1 machine cycle. A pull-up resistor can be specified with a mask option.
22	$\overline{SYNC}$ (P31)	Sync. signal output pin/input pin	I/O	An internal timing signal is outputted every machine cycle at reset time. It can be used as a normal input port after cancelling reset. A pull-up resistor can be specified with a mask option.
21	$\overline{IRQ}$ (P30)	External interrupt/input pin	I	External interrupt pin which receives an interrpt at a negative edge. Also available as a normal input port. A pull-up resistor can be specified with a mask option.
24	$\overline{SBT}$ (P33)	Serial interface clock I/O/input pin	I/O /I	Serial interface send/receive clock I/O pin. It serves as an output pin in the internal clock mode, and as an input pin in the external clock mode.Also available as a normal input port. A pull-up resistor can be specified with a mask option.
23	$\overline{SBD}$ (P32)	Serial interface data I/O/input pin	I/O /I	Serial interface send/receive data I/O pin. It inputs 8-bit serial data in the receive mode and outputs it in the send mode. Also available as a normal input port. A pull-up resistor can be specified with a mask option.
37	BZ (P42)	Buzzer output/output pin	O	A buzzer clock is outputted if P42 is set to the "L" level. It can be also specified as a normal output port with a mask option.
38	RMO	Remote control carrier output	O	A remote control carrier signal is outputted if P40 is set to the "L"level. "L" at reset time.
25~28 29~32	P00~P03 P10~P13	Parallel data I/O pin	O /I/O	4-bit parallel data output or I/O ports. "H" level at reset time. A pull-up resistor can be specified with a mask option.
33~36	P20~P23	Parallel data input pin	I	4-bit parallel data input ports. A pull-up resistor can be specified with a mask option.
21~24	P30~P33	Parallel data input pin	I	4-bit parallel data input ports. P30-P33 are also used as $\overline{IRQ}$, $\overline{SYNC}$, $\overline{SBT}$ and $\overline{SBD}$, respectively. A pull-up resistor can be specified with a mask option.
8~10	COM0 ~COM3	LCD common output pin	O	LCD common signal output pins.
39~64 1~7	SEG0 ~SEG32	LCD segment output pin	O	LCD segment signal output pins. Each segment has a 4-bit display data latch. Display data can be also read.

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