# ❑ MN101D10F , MN101D10G

| Type | MN101D10F | MN101D10G |
|---|---|---|
| ROM (×8-bit) | 96 K | 128 K |
| RAM (×8-bit) | 2.5 K | 3.5 K |
| Package | QFP100-P-1818B *Lead-free | |
| Minimum Instruction Execution Time | With main clock operated: 0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)<br>71.5 µs (at 2.7 V to 5.5 V fixed to 14.32 MHz internal frequency division)<br>When sub-clock operated: 61 µs (at 2.5 V to 5.5 V, 32.768 kHz) | |
| Interrupts | • RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4<br>• Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Capstan FG • Control • HSW<br>• Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0<br>• Serial 1 • Serial 2 • PWM 4 • OSDV-sync | |
| Timer Counter | Timer counter 0: 8-bit × 1 (timer function)<br>Clock source ····· 1/4, 1/16 of system clock frequency<br>Interrupt source ····· overflow of timer counter 0<br><br>Timer counter 1: 8-bit × 1 (timer function, linear timer counter function)<br>Clock source ····· 1/4 of system clock frequency; CTL signal<br>Interrupt source ····· overflow of timer counter 1<br><br>Timer counter 2: 16-bit × 1 (timer function, input capture,duty judgment of CTL signal(VISS/VASS detection function), generation of remote control output carrier frequency)<br>Clock source ····· 1/4, 1/16, 1/24 of system clock frequency<br>Interrupt source ····· overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register<br><br>Timer counter 3: 16-bit × 1 (timer function, generation of serial transmission clock)<br>Clock source ····· 1/4, 1/16 of system clock frequency<br>Interrupt source ····· overflow of timer counter 3<br><br>Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)<br>Clock source ····· system clock<br>Watchdog interrupt source ··· $1/2^{16}$, $1/2^{19}$ of timer counter 5 frequency<br>Clear by stable oscillation ··· after 256 counts by timer counter 5 ($2^{18}$ counts of OSC oscillation clock)<br><br>Timer counter 6: 16-bit × 1 (clock function [max. 2 s])<br>Clock source ····· 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency<br>Interrupt source ····· $1/2^{13}$, $1/2^{14}$, $1/2^{15}$ overflow of timer counter 6 | |
| Serial Interface | Serial 0: 8-bit × 1 (synchronous type)<br>(transfer direction of MSB/LSB selectable, start condition function)<br>Clock source ····· 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; NSBT0 pin input<br>Serial 1: 8-bit × 1 (synchronous type/remote control transmission)<br>(transfer direction of MSB/LSB selectable, start condition function)<br>Clock source ····· 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 3 output; NSBT1 pin input<br>Remote control clock ····· 2-division timer 3 output<br><br>Serial 2: 8-bit × 1 ($I^2C$) (master transmission/reception, slave transmission/reception)<br>Clock source ····· 1/144 to 1/252 of system clock; SCK pin input | |

| | | | |
|---|---|---|---|
| **OSD** | Display mode | : | menu(internal synchronized) display, superimpose(externally synchronized) display |
| | Applicable broadcasting system | : | NTSC, PAL, PAL-M, PAL-N |
| | Screen configuration | : | 24 characters × 2n rows (n = 1 to 6) |
| | Character type | : | max. 256 character types (variable, include special characters) |
| | Character size | : | 12 × 18 dots (vertical direction: 1 dot for 2H at not enlargement) |
| | Enlarged characters | : | each × 2 settings in horizontal and vertical |
| | Character interpolation | : | none |
| | Line background color | : | 8-hue settable in the row unit at menu display |
| | Line background intensity | : | 8 gradations settable in the row unit |
| | Screen background color : | : | 8-huesettable at menu display |
| | Character color | : | white |
| | Character intensity | : | 8 gradations settable in the row unit |
| | Border function | : | 1-dot border in 8 directions |
| | Border brightness | : | 4 gradations settable in the row unit |
| | Blinking | : | none (covered by software) |
| | Inverted character | : | settable in the character unit |
| | Halftone | : | none |
| | Input | : | composite video signal input (output level: 1 V[p-p] / 2 V[p-p]) |
| | Clamp method | : | sync tip clamp, clamp level in 4 levels |
| | Output | : | composite video output |
| | Measure against image fluctuation | : | built-in AFC circuit |
| | Dot clock | : | 1/2 of OSC oscillation clock (automatic phase adjustment) |
| | MESECAM compatibility | : | Subcarrier leak function for superimpose display |

| | | | |
|---|---|---|---|
| **XDS** | Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.) | | |
| **ROM Correction** | Correcting address designation: up to 3 addresses possible<br>Correction method: correction program being saved in internal RAM | | |
| **I/O Pins** | **I/O** | 76 | • Common use: 56 |
| | **Input** | 1 | • Common use: 1 |
| **A/D Inputs** | 8-bit × 12-ch. (without S/H) | | |
| **PWM** | 13-bit × 2-ch. (at repetition cycle 572 µs at 14.32 MHz),<br>8-bit × 1-ch. (at repetition cycle 35.7 µs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz) | | |
| **ICR** | 16-bit × 2-ch.(Speed system),<br>18-bit × 4-ch.(Phase system) | | |
| **OCR** | 16-bit × 3 (Synchronous output × 2, Rec CTL × 1 ) | | |
| **Special Ports** | 3-state output (PTO) VLP pin; CTL input;Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output;<br>Head amp/ Rotary outputs; built-in FG amp; output of 1/4 OSC oscillation clock (1 V[p-p]) | | |
| **Notes** | | | |

**See the next page for electrical characteristics, pin assignment and support tool.**

## Electrical Characteristics

### Supply current

| Parameter | Symbol | Condition | Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Operating supply current | IDD1 | 14.32 MHz operation without load, VDD = 5 V | | 50 | 100 | mA |
| | IDD2 | 1/1024 of 14.32 MHz operation without load, VDD = 2.7 V | | 2 | 5 | mA |
| | IDD3 | Stop of 14.32 MHz oscillation, VDD = 2.7 V<br>32 kHz oscillation operation without load | | 50 | 100 | µA |
| Supply current at STOP | IDSP | Stop of oscillation without load, VDD = 5 V, Ta = 55 °C | | | 10 | µA |
| Supply current at HALT | IDHT0 | 14.32 MHz oscillation without load, VDD = 5 V | | 5 | 15 | mA |
| | IDHT1 | Stop of 14.32 MHz oscillation, VDD = 2.7 V<br>32 kHz oscillation operation without load | | 5 | 20 | µA |

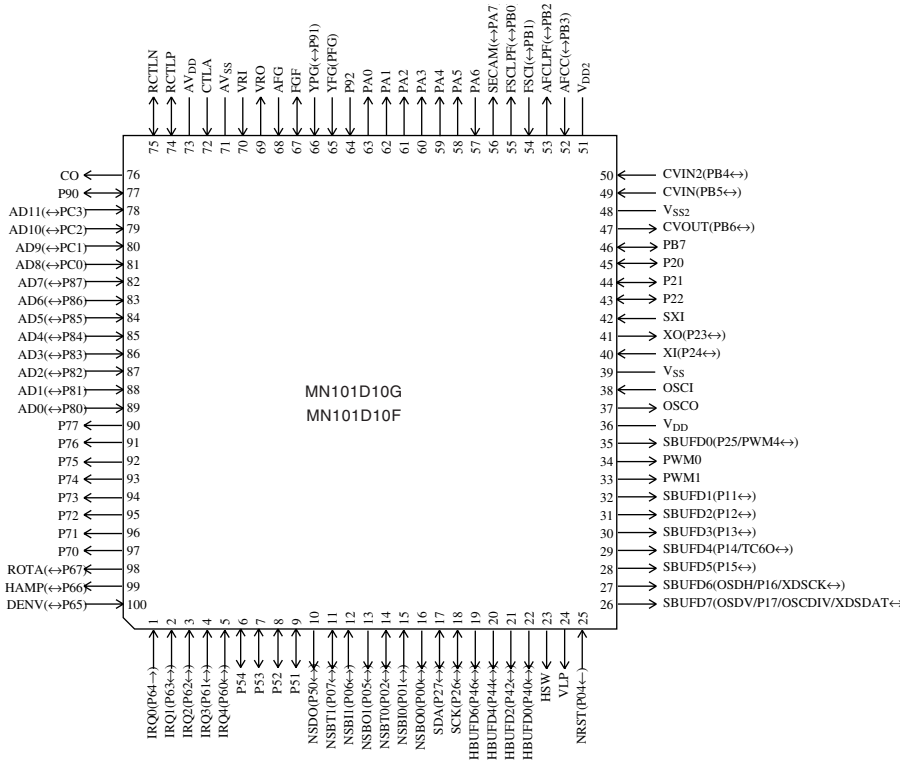
(Ta = 25 °C ± 2 °C , VSS = 0 V)

### A/D Converter Performance

| Parameter | Symbol | Condition | Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Conversion relative error | ΔNLAD | | | | ± 3 | LSB |
| A/D Conversion Time | tAD | fosc = 14.32 MHz | | 8 | | µs |
| Analog Input Voltage | | | | | 5 | V |

(Ta = 25 °C ± 2 °C , VDD = 5.0 V, VSS = 0 V)

## Pin Assignment




QFP100-P-1818B *Lead-free

## Support Tool

| | | |
|---|---|---|
| **In-circuit Emulator** | PX-ICE101C / D + PX-PRB101D10-QFP100-P-1818B-CN-M | |
| **Flash Memory Built-in Type** | Type | MN101DF10GAF |
| | ROM (× 8-bit) | 128 K |
| | RAM (× 8-bit) | 4 K |
| | Minimum instruction execution time | 0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)<br>71.5 µs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division)<br>61 µs (at 2.5 V to 5.5 V, 32.768 kHz) |
| | Package | QFP100-P-1818B *Lead-free |