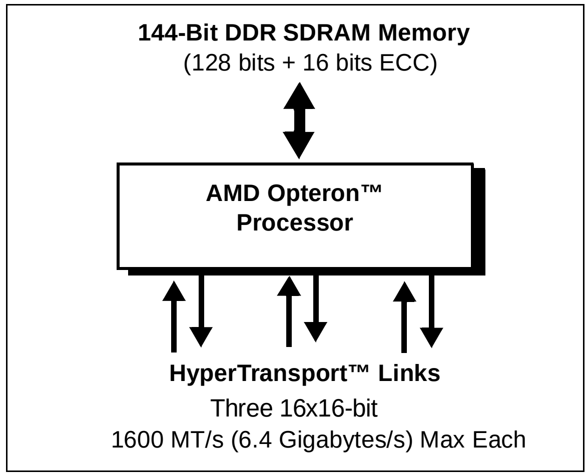
AMD Opteron™ Processor

Data Sheet

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on-chip
- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight new 64-bit integer registers (16 total)
  - Eight new 128-bit SSE/SSE2 registers (16 total)
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz (200MHz supported by Rev C0 and later)
- **HyperTransport™ Technology to I/O Devices**
  - Three links, 16-bits in each direction, each supports up to 1600 MT/s or 3.2 GB/s in each direction
  - Each link can connect to an I/O device or another processor
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction
- **1024-Kbyte (1-Mbyte) 16-Way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture—storage in addition to L1 caches
- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI compliant



- **Electrical Interfaces**
  - HyperTransport technology: LVDS-Like differential, unidirectional
  - DDR SDRAM: SSTL_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
  - 940-pin lidded ceramic micro PGA
  - 1.27-mm pin pitch
  - 31x31 row pin array
  - 40mm x 40mm ceramic substrate
  - Ceramic C4 die attach

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Revision History

Date	Revision	Description
February 2004	3.09	Added CLKIN jitter specification to Table 26. Updated note for VDDIO to VTT stress during power up/down for Table 35. Added note to require VTT tracking VDDIO/2 for Table 35. Clarified power supply relationship note for Table 35. Revised VDD specifications in Table 34. Updated notes in Table 29 to clarify termination usage. Changed ref from 2.5V to VDDIO in Table 6. Separated and revised VID Voh paramter in Table 19. Moved DIMM speed/ loading table out of this document
Novermber 2003	3.06	Removed extended range temp sensor requirement. New logo. Storage temp change in Section 7.1. HT termination change in Table 18. Added Tcase thermal diode specifications for specific revisions and frequencies in Section 7.7. Updated TDO and DBRDY pull-up info in Table 30. Changed title of design guides. Added PWROK clarification in Sequencing Relationships section. Added DDR400 support. General clean-up, added Rev C information and separated power and thermal specifications (moved to a separate document). Updated IDDIO2 I/O current specification in Table 32, changed NC_AE3 to NC_AE13 in Table 30, removed separate THERMTRIP_L electrical section and grouped with DDR pin electricals. Clarified ECC and Chip Kill descriptions in Sections 2.4.2.4 through 2.4.2.5. Corrected AMD64 naming.
April 2003	3.00	Initial release.

1 AMD Opteron™ Processor Overview

The AMD Opteron™ processor is designed for high-performance workstation and server applications. It provides three high-performance HyperTransport™ links to I/O, as well as a 128-bit high-performance DDR SDRAM memory controller. A block diagram of the AMD Opteron processor is shown in Figure 1.

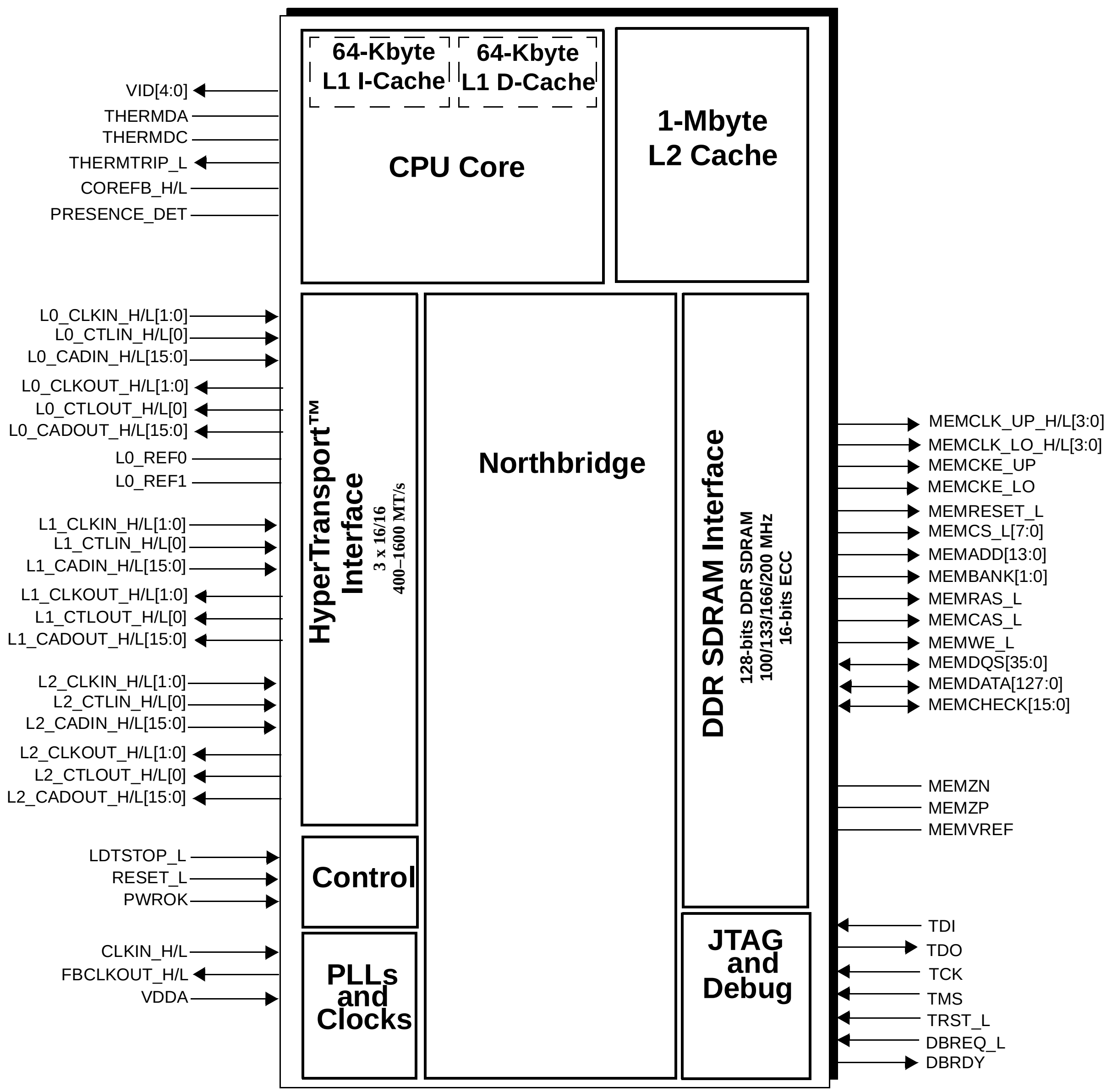


Figure 1. AMD Opteron™ Processor Block Diagram

2 Functional Description

2.1 Instruction Set Support

The AMD Opteron™ processor supports the standard x86-instruction set defined in the *AMD64 Architecture Programmer's Manual*, volumes 3–5, order# 24594. In addition, the processor supports the following extensions to the standard x86 instruction set, which are described in the same volume set:

- AMD64 instructions
- MMX™ and 3DNow!™ technology instructions
- SSE and SSE2 instructions

2.2 Internal Cache Structures

The AMD Opteron processor implements internal caching structures as described in the following sections.

2.2.1 Level 1 Caches

The L1 data cache (L1 D-Cache) contains 64 Kbytes of storage organized as two-way set associative. The L1 data cache is protected with ECC. Two simultaneous 64-bit operations (load, store, or combination) are supported. The L1 instruction cache (L1 I-Cache) contains 64 Kbytes of storage organized as two-way associative. The L1 instruction cache is protected with parity.

2.2.2 Level 2 Cache

The L2 cache contains both instruction and data stream information. It is organized as 16-way set-associative. The L2 cache data and tag store is protected with ECC. When a given cache line in the L2 cache contains instruction stream information, the ECC bits associated with the given line are used to store predecode and branch prediction information.

2.3 Error Handling (Machine Check)

The AMD Opteron processor implements the standard x86 machine check architecture as defined in the *AMD64 Architecture Programmer's Manual, Volume 2*, order# 24593, and the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094.

The machine check architecture is defined with ECC single-bit detection/correction and double-bit detection for the following arrays:

- L1 Data Cache Storage
- L2 Data Cache Storage
- L2 Data Cache Tag
- Instruction Cache
- DRAM. See "Memory Controller" on page 11.

2.4 Northbridge

The Northbridge logic in the AMD Opteron processor refers to the HyperTransport™ technology interface and the memory controller and their respective interfaces to the CPU cores. These interfaces are described in more detail in the following sections.

2.4.1 HyperTransport™ Technology Overview

The AMD Opteron processor includes three 16-bit HyperTransport technology interfaces capable of operating up to 1600 mega-transfers per second (MT/s) with a resulting bandwidth of up to 6.4 Gbytes/s (3.2 Gbytes/s in each direction). The AMD Opteron processor supports HyperTransport technology synchronous clocking mode. Refer to the *HyperTransport™ I/O Link Specification* (www.hypertransport.org) for details of link operation.

2.4.1.1 Link Initialization

The *HyperTransport™ I/O Link Specification* details the negotiation that occurs at power-on to determine the widths and rates used with the link. Refer also to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for information about link initialization and setup of routing tables.

Refer to the *AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180, for details on the proper HyperTransport technology signal termination resistor values.

2.4.1.2 HyperTransport™ Technology Transfer Speeds

The HyperTransport link of the AMD Opteron processor is capable of operating at 400, 800, 1200, and 1600 MT/s. The link transfer rate is determined during the software configuration of the system, as specified in the *HyperTransport™ I/O Link Specification*.

2.4.2 Memory Controller

The processor's memory controller provides a programmable interface to a variety of standard registered DDR SDRAM DIMM configurations. Refer to the *BIOS and Kernel Developer's Guide for* *the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094, for supported DRAM speeds under specific loading conditions.

- Self-Refresh mode
- The controller provides programmable control of DRAM timing parameters to support the following memory speeds:
  - 100 MHz (DDR200) PC-1600 DIMMs
  - 133 MHz (DDR266) PC-2100 DIMMs
  - 166 MHz (DDR333) PC-2700 DIMMs
  - 200 MHz (DDR400) PC-3200 DIMMs*
- DRAM devices that are 4, 8 and 16 bits wide
- DIMM sizes from 32 Mbytes (using 64Mb x16 DRAMs) to 4 Gbytes (using a stacked DIMM with 1Gb x4 DRAMs)
- Interleaving memory within DIMMs
- Stacked registered DIMMs
- ECC checking with single-bit correction and double-bit detection
- Chip Kill ECC allows single symbol correction and double symbol detection
- May be configured for 32-byte or 64-byte burst length
- Programmable page-policy:
  - Supports up to 16 open pages total across all chip-selects
  - Statically idle open-page time
  - Optional dynamic precharge control based on page-hit/miss history

* DDR400 supported by Rev C0 and later, Refer to *AMD Opteron™ Processor Power and Thermal Data Sheet*, order# 30417, for silicon revision determination

For programming information and specific details of the features listed above, refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094.

2.4.2.1 Memory Pin Interface

The memory controller of the AMD Opteron processor supports registered DDR SDRAM DIMMs. The following list applies to the pin interface:

- The MEMRESET_L pin is required for registered DIMMs and is used to reset the register as required to support the Suspend to RAM power management state (ACPI S3).
- The memory controller can be configured to support either 64-bit or 128-bit memory interfaces. Refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™*

Processors, order# 26094, for restrictions based on DDR SDRAM speed.

  - A 64-bit memory system can support up to four DIMMs, each 64-bits wide
  - A 128-bit memory system can support up to eight DIMMs, each 64-bits wide, and must be populated in even numbered pairs as described in the *AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180.

- Registered DIMMs configured with x4 DRAMs require an additional 16 DQS pins without ECC support or 18 DQS pins with ECC support. The processor's memory controller provides a total of 36 DQS pins to accommodate this requirement. The additional DQS pins can be connected to the DIMM Data Mask (DM) pins when connected to x8 or x16 DIMMs. DIMMs populated with x4 devices normally connect the DRAM Data Mask (DM) pins to VSS.

2.4.2.2 DRAM Operation

At power-on reset, the MEMCKE_LO/UP and MEMRESET_L pins are driven Low while the processor PLLs are ramping. Clocks are driven on the MEMCLK_LO_H/L[3:0] and MEMCLK_UP_H/L[3:0] pins only after BIOS programs the appropriate clock ratio value in the memory controller configuration registers. The actual DRAM frequency may vary for some speeds based on the CPU clock multiplier, as shown in Table 1 on page 13 (the memory controller automatically adjusts refresh counters at all speeds as required to meet the device refresh specifications). Refer to "Power-Up Signal Sequencing" on page 65 for further details on the sequencing of the MEMRESET_L and MEMCKE_LO/UP pins.

Table 1. DRAM Interface Speed vs. CPU Core Clock Multiplier

Multiplier	Core Frequency	DRAM Frequency			
		100 MHz	133 MHz	166 MHz	200 MHz[1]
4	800 MHz	100.00	133.33	160.00	160.00
5	1000 MHz	100.00	125.00	166.66	200.00
6	1200 MHz	100.00	133.33	150.00	200.00
7	1400 MHz	100.00	127.27	155.55	200.00
8	1600 MHz	100.00	133.33	160.00	200.00
9	1800 MHz	100.00	128.57	163.63	200.00
10	2000 MHz	100.00	133.33	166.66	200.00
11	2200 MHz	100.00	129.41	157.14	200.00
12	2400 MHz	100.00	133.33	160.00	200.00
13	2600 MHz	100.00	130.00	162.50	200.00

Notes:

1. *DDR400 (200MHz) supported by Rev C0 and later. Refer to the* AMD Opteron™ Processor Power and Thermal Data Sheet, *order# 30417 for silicon revision determination.*

Table 2 on page 15 lists the maximum memory sizes per chip-select for the various supported DRAM device configurations. Note that for DIMMs using two chip-selects, the total memory size per DIMM is doubled. Refer to the *AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180, for details on the connection scheme for registered DIMMs in an AMD Opteron processor system.

Table 2. Total Memory Sizes Per Chip Select

Devices Used on DIMMs	Size Per CS
64 M-bit (4M x4-bits x4 banks)	128 Mbyte
64 M-bit (2M x8-bits x4 banks)	64 Mbyte
64 M-bit (1M x16-bits x4 banks)	32 Mbyte
128 M-bit (8M x4-bits x4 banks)	256 Mbyte
128 M-bit (4M x8-bits x4 banks)	128 Mbyte
128 M-bit (2M x16-bits x4 banks)	64 Mbyte
256 M-bit (16M x4-bits x4 banks)	512 Mbyte
256 M-bit (8M x8-bits x4 banks)	256 Mbyte
256 M-bit (4M x16-bits x4 banks)	128 Mbyte
512 M-bit (32M x4-bits x4 banks)	1 Gbyte
512 M-bit (16M x8-bits x4 banks)	512 Mbyte
512 M-bit (8M x16-bits x4 banks)	256 Mbyte
1 G-bit (64M x4-bits x4 banks)	2 Gbyte
1 G-bit (32M x8-bits x4 banks)	1 Gbyte
1 G-bit (16M x16-bits x4 banks)	512 Mbyte

The controller supports programmable timing and refresh as described in the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094. Auto-refresh is supported and is staggered by t_{RFC} across chip-selects to reduce system noise. Unpopulated DIMM slots are not refreshed.

2.4.2.3 DRAM Power Management

The memory controller supports self-refresh mode to accommodate various power management states such as ACPI S1 and S3 states. The MEMRESET_L pin is provided for resetting the registers on registered DDR SDRAM DIMMs as required for the S3 (Suspend-to-RAM) power management state.

2.4.2.4 Chip Kill

In Chip Kill mode the memory controller can correct single symbol errors and detect double symbol errors across the 128-bit wide data path. This feature optionally takes the place of normal ECC error detection and correction. Operating the memory controller with Chip Kill enabled will result in a two clock latency penalty on memory access due to the detection, correction, and data containment overhead of operating in this mode.

2.4.2.5 Main Memory Hardware Scrubbing

The memory controller scrubs the main memory arrays to prevent the build up of soft errors. Any correctable or non-correctable errors are logged to the machine check logs and non-correctable errors can be programmed to invoke the machine check interrupt. A correctable error is a single-bit error in normal ECC mode or a single symbol error in Chip Kill mode. There are two modes of main memory scrubbing that can be used independently or combined, as described in the following sections.

2.4.2.5.1 Sequential Scrubbing

In this mode, the scrubber sequentially proceeds through main memory, performing a read-write cycle or a read-modify-write cycle if a correctable error is found. The scrubber scrubs one cache line on each scrub interval that is programmable from 40 ns to 84 ms.

2.4.2.5.2 Source Correction Scrubbing

In this mode, the scrubber is directed to scrub any cache line that is the source of any corrected error during normal accesses. During normal operation when source correction scrubbing is disabled, single-bit errors are corrected on the fly and the corrected data is passed without updating the source memory location. When source scrubbing is enabled the scrubber also corrects the source memory location.

2.4.2.5.3 Sequential Plus Source Correction Scrubbing

When both sequential and source correction scrubbing are enabled, the scrubber sequentially proceeds through main memory. If a correctable error is detected during normal operation, the scrubber is redirected to the location of the error, and after it corrects that location in main memory it resumes sequential scrubbing at the previous location.

3 Power Management

The AMD Opteron™ processor provides the following power management features designed to be compliant with the Advanced Configuration and Power Interface (ACPI) Specification and HyperTransport™ technology:

- Halt state with associated programmable power savings
- STPCLK/Stop Grant protocol capable of supporting eight distinct versions of Stop Grant
- LDTSTOP_L signal support
- Memory controller and host bridge power management
- Voltage plane isolation based upon PWROK signal
- Low-power state while RESET_L signal is asserted
- On-die thermal diode

Table 3 maps processor capabilities to ACPI states.

Table 3. Processor Capabilities Mapped to ACPI States

ACPI State	Processor
C1	Halt
Passive Cooling	Passive Cooling is supported by Stop Grant (throttling).
S1	Stop Grant. In response to LDTSTOP_L assertion, memory is placed in self-refresh mode and the host bridge and memory controller are placed into a low-power state.
S3	Processor core and HyperTransport™ technology voltage planes are not powered. DDR SDRAM interface remains powered and holds memory in self-refresh mode.
S4, S5, G3	All power is removed from the processor.

3.1 Halt

When the HLT instruction is executed, the processor stops program execution and issues a Halt special cycle. The power savings associated with the Halt state are determined by configuration registers in the processor (refer to the *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors,* order# 26094, for details of these configuration registers). The CPU clock grid frequency can be divided down in the absence of probe activity that would force the processor caches to be snooped.

The CPU clock grid is automatically brought to full frequency when probe activity is present and returned to the low-power state when probe activity ceases.

If a STPCLK assertion message is received while the processor is in the Halt state, the processor enters the Stop Grant state and issues a Stop Grant special cycle. When a STPCLK deassertion message is received, the processor exits the Stop Grant state and returns to the Halt state.

The processor exits the Halt state in response to PWROK deassertion, RESET_L assertion, INIT, NMI, SMI, or any unmasked interrupt received over the HyperTransport link.

3.2 STPCLK/Stop Grant

When the processor recognizes the STPCLK assertion message, it enters the Stop Grant state on the next instruction boundary and issues a Stop Grant special cycle. The power savings associated with the Stop Grant state are determined by configuration registers in the processor. The power savings mechanisms associated with the Stop Grant state include the following:

- CPU clock grid divisor applied in the absence of probe activity. If probe activity that requires a cache snoop occurs while the processor is in the Stop Grant state, the clock grid is ramped back up to service the probe. When probe activity ceases, the CPU clock grid is ramped back down again.
- Placing system memory into self-refresh mode in response to LDTSTOP_L signal assertion.
- Ramping the processor host bridge/memory controller clock grid down in response to LDTSTOP_L signal assertion.
- Changing HyperTransport link width and/or link frequency in response to LDTSTOP_L signal assertion.

The processor exits the Stop Grant state when it receives the following:

- A STPCLK deassertion message.
- RESET_L pin asserted or an INIT assertion message.
- PWROK is deasserted.

If the LDTSTOP_L signal is asserted after the processor is in the Stop Grant state, then LDTSTOP_L must be deasserted, and the HyperTransport link must be re-initialized before a STPCLK deassertion message can be received by the processor to bring the processor out of the Stop Grant state.

The processor's host bridge ensures that STPCLK messages are passed to the CPU prior to the subsequent I/O response to the cycle that caused STPCLK assertion as long as the subsequent I/O response message has the PassPW bit clear and the Unit ID of the response matches the Unit ID of the STPCLK message.

3.3 PWROK

When PWROK is deasserted, the processor performs the following steps:

- Isolates its VDDIO- and VTT-powered logic from all other internal logic to prevent leakage current paths between power planes.

- Tristates all DDR SDRAM I/O pins except for the MEMCKE_LO/UP and MEMRESET_L outputs, which are driven Low.
- Drives its VID[4:0] outputs to the value that selects the startup core voltage level.

3.4 RESET_L and MEMRESET_L

When RESET_L is asserted, the processor performs the following steps:

- The processor core is held in a low-power state.
- The MEMCKE_LO/UP and MEMRESET_L outputs are forced low.

After RESET_L is deasserted, BIOS must program the appropriate clock divisor in the memory controller configuration registers, causing the MEMCLK_LO_H/L[3:0] and MEMCLK_UP_H/L[3:0] clocks to be driven. Refer to “Power-Up Signal Sequencing” on page 65 for details of RESET_L and MEMRESET_L sequencing during initial power-on.

3.5 Thermal Diode

The processor provides an on-die thermal diode with anode and cathode brought out to processor pins. This diode can be read by an external temperature sensor to determine the processor’s temperature. Refer to the *AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180, for details on connecting the thermal diode.

3.6 THERMTRIP_L

The AMD Opteron processor provides a hardware-enforced thermal protection mechanism. When the processor’s die temperature exceeds a specified temperature, the processor is designed to protect itself from over-temperature conditions by stopping its internal clocks and asserting the THERMTRIP_L output.

THERMTRIP_L assertion is only valid when PWROK is asserted and RESET_L is deasserted.

If the processor’s die temperature still exceeds the thermal trip point when RESET_L is deasserted, THERMTRIP_L will immediately be reasserted and the processor’s internal clocks will be stopped.

THERMTRIP_L assertion indicates the processor die temperature has exceeded normal operating parameters. PWROK must be deasserted in response to a THERMTRIP_L assertion to help ensure proper processor operation.

4 Connection Diagrams

The pinout for the AMD Opteron™ processor is illustrated in this chapter. The ball map is divided into two parts. Figure 2 on page 22 shows the left portion of the top view, and Figure 3 on page 23 shows the right portion of the top view.

The pin designations are defined in Chapter 5. Table 4 on page 26 lists the pins alphabetically by pin name.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			L1_CADOUT_H[0]	L1_CADOUT_L[0]	L1_CADOUT_H[2]	L1_CADOUT_L[2]	L1_CLKOUT_H[0]	L1_CLKOUT_L[0]	L1_CADOUT_H[5]	L1_CADOUT_L[5]	L1_CADOUT_H[7]	L1_CADOUT_L[7]	L1_CTLIN_L[0]	L1_CTLIN_H[0]	L1_CADIN_L[6]
B			VSS	L1_CADOUT_H[1]	VDD	L1_CADOUT_H[3]	VSS	L1_CADOUT_H[4]	VDD	L1_CADOUT_H[6]	VSS	L1_CTLOUT_H[0]	VDD	L1_CADIN_L[7]	VSS
C	VDDA1	VDDA3	L1_CADOUT_L[8]	L1_CADOUT_L[1]	L1_CADOUT_L[10]	L1_CADOUT_L[3]	L1_CLKOUT_L[1]	L1_CADOUT_L[4]	L1_CADOUT_L[13]	L1_CADOUT_L[6]	L1_CADOUT_L[15]	L1_CTLOUT_L[0]	NC_C13	L1_CADIN_H[7]	L1_CADIN_H[14]
D	L0_REF0	VDDA2	L1_CADOUT_H[8]	VDD	L1_CADOUT_H[10]	VSS	L1_CLKOUT_H[1]	VDD	L1_CADOUT_H[13]	VSS	L1_CADOUT_H[15]	VDD	NC_D13	VSS	L1_CADIN_L[14]
E	L0_REF1	VSS	L1_CADOUT_H[9]	L1_CADOUT_L[9]	L1_CADOUT_H[11]	L1_CADOUT_L[11]	L1_CADOUT_H[12]	L1_CADOUT_L[12]	L1_CADOUT_H[14]	L1_CADOUT_L[14]	NC_E11	NC_E12	L1_CADIN_L[15]	L1_CADIN_H[15]	L1_CADIN_L[13]
F	VSS	VSS			VSS	VDD	NC_F7	VSS	VID[3]	VSS	VDD	PWROK	VSS	VSS	VDD
G	L0_CADIN_H[1]	L0_CADIN_L[0]	L0_CADIN_H[0]	VSS	L0_CADIN_H[8]	NC_G6	VDD	DBRDY	VID[4]	VID[2]	VID[0]	RESET_L	VSS	NC_G14	VSS
H	L0_CADIN_L[1]	VDD	L0_CADIN_H[9]	L0_CADIN_L[9]	L0_CADIN_L[8]	VSS	NC_H7	VLDT_1	NC_H9	VLDT_1	VID[1]	NC_H12	NC_H13	NC_H14	VSS
J	L0_CADIN_H[3]	L0_CADIN_L[2]	L0_CADIN_H[2]	VDD	L0_CADIN_H[10]	LDTSTOP_L	DBREQ_L	VSS	VLDT_1	VSS	VLDT_1	VSS	VDD	VSS	VLDT_1
K	L0_CADIN_L[3]	VSS	L0_CADIN_H[11]	L0_CADIN_L[11]	L0_CADIN_L[10]	VDD	CORESENSE_H	NC_K8	VSS	VLDT_1	VSS	VDD	VSS	VLDT_1	VSS
L	L0_CADIN_H[4]	L0_CLKIN_L[0]	L0_CLKIN_H[0]	VSS	L0_CLKIN_H[1]	COREFB_L	COREFB_H	NC_L8	VDD	VSS	VDD	VSS	VDD	VSS	VDD
M	L0_CADIN_L[4]	VDD	L0_CADIN_H[12]	L0_CADIN_L[12]	L0_CLKIN_L[1]	VSS	VSS	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS
N	L0_CADIN_H[6]	L0_CADIN_L[5]	L0_CADIN_H[5]	VDD	L0_CADIN_H[13]	NC_N6	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
P	L0_CADIN_L[6]	VSS	L0_CADIN_H[14]	L0_CADIN_L[14]	L0_CADIN_L[13]	VDD	VSS	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS
R	L0_CTLIN_H[0]	L0_CADIN_L[7]	L0_CADIN_H[7]	VSS	L0_CADIN_H[15]	NC_R6	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
T	L0_CTLIN_L[0]	VDD	NC_T3	NC_T4	L0_CADIN_L[15]	VSS	NC_T7	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
U	L0_CADOUT_L[7]	L0_CTLOUT_H[0]	L0_CTLOUT_L[0]	VDD	NC_U5	NC_U6	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
V	L0_CADOUT_H[7]	VSS	L0_CADOUT_L[15]	L0_CADOUT_H[15]	NC_V5	VDD	VSS	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS
W	L0_CADOUT_L[5]	L0_CADOUT_H[6]	L0_CADOUT_L[6]	VSS	L0_CADOUT_L[14]	NC_W6	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
Y	L0_CADOUT_H[5]	VDD	L0_CADOUT_L[13]	L0_CADOUT_H[13]	L0_CADOUT_H[14]	VSS	VSS	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AA	L0_CLKOUT_L[0]	L0_CADOUT_H[4]	L0_CADOUT_L[4]	VDD	L0_CADOUT_L[12]	NC_AA6	VLDT_0	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AB	L0_CLKOUT_H[0]	VSS	L0_CLKOUT_L[1]	L0_CLKOUT_H[1]	L0_CADOUT_H[12]	VDD	VSS	VDD	VSS	VLDT_2	VSS	VDD	VSS	VLDT_2	VSS
AC	L0_CADOUT_L[2]	L0_CADOUT_H[3]	L0_CADOUT_L[3]	VSS	L0_CADOUT_L[11]	NC_AC6			VLDT_2	VSS	VLDT_2	VSS	VDD	VSS	VLDT_2
AD	L0_CADOUT_H[2]	VDD	L0_CADOUT_L[10]	L0_CADOUT_H[10]	L0_CADOUT_H[11]	VSS	TRST_L	VLDT_2	VSS	VLDT_2	VSS	VDD	VSS	VDD	VSS
AE	L0_CADOUT_L[0]	L0_CADOUT_H[1]	L0_CADOUT_L[1]	VDD	L0_CADOUT_L[9]	TMS	TCK	TDO	NC_AE9	NC_AE10	NC_AE11	NC_AE12	NC_AE13	NC_AE14	THERMTRIP_L
AF	L0_CADOUT_H[0]	VSS	L0_CADOUT_L[8]	L0_CADOUT_H[8]	L0_CADOUT_H[9]	VDD	TDI	VSS	NC_AF9	VDD	NC_AF11	VSS	NC_AF13	VDD	NC_AF15
AG	NC_AG1	VSS	L2_CADIN_H[8]	L2_CADIN_L[8]	L2_CADIN_H[10]	L2_CADIN_L[10]	L2_CLKIN_H[1]	L2_CLKIN_L[1]	L2_CADIN_H[13]	L2_CADIN_L[13]	L2_CADIN_H[15]	L2_CADIN_L[15]	NC_AG13	NC_AG14	L2_CADOUT_L[14]
AH	THERMDC	NC_AH2	VSS	L2_CADIN_L[9]	VDD	L2_CADIN_L[11]	VSS	L2_CADIN_L[12]	VDD	L2_CADIN_L[14]	VSS	NC_AH12	VDD	L2_CADOUT_H[15]	VSS
AJ	THERMDA	NC_AJ2	L2_CADIN_H[0]	L2_CADIN_H[9]	L2_CADIN_H[2]	L2_CADIN_H[11]	L2_CLKIN_H[0]	L2_CADIN_H[12]	L2_CADIN_H[5]	L2_CADIN_H[14]	L2_CADIN_H[7]	NC_AJ12	L2_CTLOUT_L[0]	L2_CADOUT_L[15]	L2_CADOUT_L[6]
AK		PRESENCE_DET	L2_CADIN_L[0]	VDD	L2_CADIN_L[2]	VSS	L2_CLKIN_L[0]	VDD	L2_CADIN_L[5]	VSS	L2_CADIN_L[7]	VDD	L2_CTLOUT_H[0]	VSS	L2_CADOUT_H[6]
AL			L2_CADIN_H[1]	L2_CADIN_L[1]	L2_CADIN_H[3]	L2_CADIN_L[3]	L2_CADIN_H[4]	L2_CADIN_L[4]	L2_CADIN_H[6]	L2_CADIN_L[6]	L2_CTLIN_H[0]	L2_CTLIN_L[0]	L2_CADOUT_L[7]	L2_CADOUT_H[7]	L2_CADOUT_L[5]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 2. AMD Opteron™ Processor Micro PGA—Top View, Left Side

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
L1_CADIN_H[6]	L1_CADIN_L[4]	L1_CADIN_H[4]	L1_CADIN_L[3]	L1_CADIN_H[3]	L1_CADIN_L[1]	L1_CADIN_H[1]	VDDIO	MEMDATA[4]	MEMDATA[1]	MEMDATA[6]	MEMDATA[2]	MEMDATA[3]	MEMDATA[9]			A
L1_CADIN_L[5]	VDD	L1_CLKIN_L[0]	VSS	L1_CADIN_L[2]	VDD	L1_CADIN_L[0]	VSS	MEMDATA[0]	MEMDQS[9]	VSS	MEMDATA[7]	MEMDATA[8]	VSS	MEMDATA[13]		B
L1_CADIN_H[5]	L1_CADIN_H[12]	L1_CLKIN_H[0]	L1_CADIN_H[11]	L1_CADIN_H[2]	L1_CADIN_H[9]	L1_CADIN_H[0]	VDDIO	MEMDATA[5]	MEMDQS[0]	MEMDATA[71]	MEMDATA[72]	MEMDATA[12]	MEMDQS[1]	MEMDQS[10]	MEMDATA[14]	C
VDD	L1_CADIN_L[12]	VSS	L1_CADIN_L[11]	VDD	L1_CADIN_L[9]	VSS	VSS	MEMDATA[69]	MEMDQS[18]	VDDIO	MEMDATA[76]	VDDIO	MEMDATA[77]	VSS	MEMDATA[15]	D
L1_CADIN_H[13]	L1_CLKIN_L[1]	L1_CLKIN_H[1]	L1_CADIN_L[10]	L1_CADIN_H[10]	L1_CADIN_L[8]	L1_CADIN_H[8]	VDDIO	MEMDATA[65]	MEMDATA[70]	MEMDATA[67]	MEMDATA[73]	MEMDQS[19]	MEMDQS[28]	MEMDATA[10]	MEMDATA[11]	E
VSS	VSS	VDD	VDD	VTT	VTT	MEMVREF0	MEMDATA[68]	MEMDQS[27]	MEMDATA[66]	MEMDATA[78]	MEMDATA[79]	MEMDATA[74]	MEMDATA[20]	MEMDATA[16]	MEMDATA[17]	F
CLKIN_H	VSS	FBCLKOUT_H	VTT	MEMCLK_UP_H[3]	MEMCLK_UP_L[3]	VSS	MEMDATA[64]	VSS	MEMRESET_L	VDDIO	MEMDATA[75]	VDDIO	MEMDATA[84]	VSS	MEMDATA[21]	G
CLKIN_L	VSS	FBCLKOUT_L	VTT			VDDIO	MEMCLK_LO_H[3]	MEMCKE_UP	MEMCKE_LO	MEMDATA[80]	MEMDATA[81]	MEMDATA[85]	MEMDQS[2]	MEMDQS[11]	MEMDATA[18]	H
VLDT_1	VSS	VSS	VTT	VSS	VDDIO	VSS	MEMCLK_LO_L[3]	MEMADD[12]	MEMADD[11]	MEMDQS[20]	MEMDQS[29]	MEMDATA[82]	MEMDATA[22]	MEMDATA[23]	MEMDATA[19]	J
VLDT_1	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMADD[9]	VSS	MEMADD[7]	VDDIO	MEMDATA[86]	VDDIO	MEMDATA[87]	VSS	MEMDATA[24]	K
VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	MEMADD[8]	MEMCLK_UP_H[1]	MEMCLK_UP_L[1]	MEMDATA[83]	MEMDATA[88]	MEMDATA[92]	MEMDATA[28]	MEMDATA[29]	MEMDATA[25]	L
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	NC_M23	MEMADD[5]	MEMADD[6]	MEMDATA[93]	MEMDATA[89]	MEMDQS[21]	MEMDQS[3]	MEMDQS[12]	MEMDATA[30]	M
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMADD[3]	VSS	MEMADD[4]	VDDIO	MEMDQS[30]	VDDIO	MEMDATA[94]	VSS	MEMDATA[26]	N
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	MEMADD[2]	MEMCHECK[13]	MEMCHECK[12]	MEMDATA[90]	MEMDATA[91]	MEMDATA[95]	MEMDATA[27]	MEMCHECK[4]	MEMDATA[31]	P
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMCLK_UP_H[0]	MEMCHECK[8]	MEMCHECK[9]	MEMCHECK[10]	MEMDQS[35]	MEMDQS[26]	MEMCHECK[1]	MEMCHECK[5]	MEMCHECK[0]	R
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	MEMCLK_UP_L[0]	VSS	MEMADD[1]	VDDIO	MEMCHECK[11]	VDDIO	MEMCHECK[14]	VSS	MEMDQS[8]	T
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	VDDIO	MEMCLK_LO_L[0]	MEMCLK_LO_H[0]	MEMDATA[100]	MEMDATA[96]	MEMCHECK[15]	MEMCHECK[6]	MEMCHECK[2]	MEMDQS[17]	U
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	NC_V23	MEMADD[10]	MEMADD[0]	MEMDQS[22]	MEMDATA[97]	MEMDATA[101]	MEMDATA[32]	MEMCHECK[7]	MEMCHECK[3]	V
VSS	VDD	VSS	VDD	VSS	VDDIO	VSS	MEMBANK[0]	VSS	MEMBANK[1]	VDDIO	MEMDATA[98]	VDDIO	MEMDQS[31]	VSS	MEMDATA[36]	W
VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	MEMCLK_LO_H[1]	MEMWE_L	MEMRAS_L	MEMDATA[99]	MEMDATA[103]	MEMDATA[102]	MEMDQS[4]	MEMDATA[33]	MEMDATA[37]	Y
VSS	VDD	VSS	VDDIO	VSS	VDDIO	VSS	MEMCLK_LO_L[1]	MEMCS_L[0]	MEMCAS_L	MEMDATA[109]	MEMDATA[104]	MEMDATA[108]	MEMDATA[38]	MEMDATA[34]	MEMDQS[13]	AA
VLDT_2	VSS	VDD	VSS	VDDIO	VSS	VDDIO	VDDIOFB_H	VSS	MEMCS_L[1]	VDDIO	MEMDQS[32]	VDDIO	MEMDATA[105]	VSS	MEMDATA[39]	AB
VLDT_2	VSS	VTT	VTT	VSS	VDDIO	VSS	VDDIOFB_L	MEMCS_L[3]	MEMCS_L[2]	MEMDATA[110]	MEMDATA[106]	MEMDQS[23]	MEMDATA[40]	MEMDATA[44]	MEMDATA[35]	AC
VDD	VSS			MEMCLK_LO_L[2]	MEMCLK_LO_H[2]	VDDIO	MEMCS_L[7]	MEMCS_L[5]	MEMCS_L[4]	MEMDATA[112]	MEMDATA[111]	MEMDATA[107]	MEMDQS[14]	MEMDATA[41]	MEMDATA[45]	AD
MEMZP	VSS	VTT	VTT	MEMCLK_UP_L[2]	MEMCLK_UP_H[2]	VSS	MEMADD[13]	VSS	MEMCS_L[6]	VDDIO	MEMDATA[113]	VDDIO	MEMDATA[116]	VSS	MEMDQS[5]	AE
VSS	MEMZN	VTT	VTT_SENSE	VDDIO_SENSE	VSS	MEMVREF1	MEMDATA[123]	MEMDQS[25]	MEMDATA[121]	MEMDATA[118]	MEMDQS[33]	MEMDATA[117]	MEMDATA[43]	MEMDATA[46]	MEMDATA[42]	AF
L2_CADOUT_H[14]	L2_CADOUT_L[12]	L2_CADOUT_H[12]	L2_CADOUT_L[11]	L2_CADOUT_H[11]	L2_CADOUT_L[9]	L2_CADOUT_H[9]	VDDIO	MEMDATA[127]	MEMDQS[34]	MEMDATA[125]	MEMDATA[119]	MEMDQS[24]	MEMDATA[52]	MEMDATA[48]	MEMDATA[47]	AG
L2_CADOUT_H[13]	VDD	L2_CLKOUT_H[1]	VSS	L2_CADOUT_H[10]	VDD	L2_CADOUT_H[8]	VSS	MEMDATA[122]	MEMDATA[126]	VDDIO	MEMDATA[124]	VDDIO	MEMDATA[114]	VSS	MEMDATA[49]	AH
L2_CADOUT_L[13]	L2_CADOUT_L[4]	L2_CLKOUT_L[1]	L2_CADOUT_L[3]	L2_CADOUT_L[10]	L2_CADOUT_L[1]	L2_CADOUT_L[8]	VDDIO	MEMDATA[63]	MEMDQS[16]	MEMDATA[120]	MEMDATA[60]	MEMDATA[55]	MEMDATA[115]	MEMDQS[15]	MEMDATA[53]	AJ
VDD	L2_CADOUT_H[4]	VSS	L2_CADOUT_H[3]	VDD	L2_CADOUT_H[1]	VSS	VSS	MEMDATA[58]	MEMDATA[62]	VSS	MEMDATA[61]	MEMDATA[50]	VSS	MEMDATA[54]		AK
L2_CADOUT_H[5]	L2_CLKOUT_L[0]	L2_CLKOUT_H[0]	L2_CADOUT_L[2]	L2_CADOUT_H[2]	L2_CADOUT_L[0]	L2_CADOUT_H[0]	VDDIO	MEMDATA[59]	MEMDQS[7]	MEMDATA[57]	MEMDATA[56]	MEMDATA[51]	MEMDQS[6]			AL
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 3. AMD Opteron™ Processor Micro PGA—Top View, Right Side

5 Pin Designations

Table 4, beginning on page 26, lists the pins alphabetically by pin name.

Table 4. Pin List by Name

CLKIN_H	G16	L0_CADIN_L[11]	K4	L0_CADOUT_H[9]	AF5
CLKIN_L	H16	L0_CADIN_L[12]	M4	L0_CADOUT_L[0]	AE1
COREFB_H	L7	L0_CADIN_L[13]	P5	L0_CADOUT_L[1]	AE3
COREFB_L	L6	L0_CADIN_L[14]	P4	L0_CADOUT_L[10]	AD3
CORESENSE_H	K7	L0_CADIN_L[15]	T5	L0_CADOUT_L[11]	AC5
DBRDY	G8	L0_CADIN_L[2]	J2	L0_CADOUT_L[12]	AA5
DBREQ_L	J7	L0_CADIN_L[3]	K1	L0_CADOUT_L[13]	Y3
FBCLKOUT_H	G18	L0_CADIN_L[4]	M1	L0_CADOUT_L[14]	W5
FBCLKOUT_L	H18	L0_CADIN_L[5]	N2	L0_CADOUT_L[15]	V3
L0_CADIN_H[0]	G3	L0_CADIN_L[6]	P1	L0_CADOUT_L[2]	AC1
L0_CADIN_H[1]	G1	L0_CADIN_L[7]	R2	L0_CADOUT_L[3]	AC3
L0_CADIN_H[10]	J5	L0_CADIN_L[8]	H5	L0_CADOUT_L[4]	AA3
L0_CADIN_H[11]	K3	L0_CADIN_L[9]	H4	L0_CADOUT_L[5]	W1
L0_CADIN_H[12]	M3	L0_CADOUT_H[0]	AF1	L0_CADOUT_L[6]	W3
L0_CADIN_H[13]	N5	L0_CADOUT_H[1]	AE2	L0_CADOUT_L[7]	U1
L0_CADIN_H[14]	P3	L0_CADOUT_H[10]	AD4	L0_CADOUT_L[8]	AF3
L0_CADIN_H[15]	R5	L0_CADOUT_H[11]	AD5	L0_CADOUT_L[9]	AE5
L0_CADIN_H[2]	J3	L0_CADOUT_H[12]	AB5	L0_CLKIN_H[0]	L3
L0_CADIN_H[3]	J1	L0_CADOUT_H[13]	Y4	L0_CLKIN_H[1]	L5
L0_CADIN_H[4]	L1	L0_CADOUT_H[14]	Y5	L0_CLKIN_L[0]	L2
L0_CADIN_H[5]	N3	L0_CADOUT_H[15]	V4	L0_CLKIN_L[1]	M5
L0_CADIN_H[6]	N1	L0_CADOUT_H[2]	AD1	L0_CLKOUT_H[0]	AB1
L0_CADIN_H[7]	R3	L0_CADOUT_H[3]	AC2	L0_CLKOUT_H[1]	AB4
L0_CADIN_H[8]	G5	L0_CADOUT_H[4]	AA2	L0_CLKOUT_L[0]	AA1
L0_CADIN_H[9]	H3	L0_CADOUT_H[5]	Y1	L0_CLKOUT_L[1]	AB3
L0_CADIN_L[0]	G2	L0_CADOUT_H[6]	W2	L0_CTLIN_H[0]	R1
L0_CADIN_L[1]	H1	L0_CADOUT_H[7]	V1	L0_CTLIN_L[0]	T1
L0_CADIN_L[10]	K5	L0_CADOUT_H[8]	AF4	L0_CTLOUT_H[0]	U2

Table 4. Pin List by Name (Continued)

L0_CTLOUT_L[0]	U3	L1_CADIN_L[3]	A19	L1_CADOUT_L[13]	C9
L0_REF0	D1	L1_CADIN_L[4]	A17	L1_CADOUT_L[14]	E10
L0_REF1	E1	L1_CADIN_L[5]	B16	L1_CADOUT_L[15]	C11
L1_CADIN_H[0]	C22	L1_CADIN_L[6]	A15	L1_CADOUT_L[2]	A6
L1_CADIN_H[1]	A22	L1_CADIN_L[7]	B14	L1_CADOUT_L[3]	C6
L1_CADIN_H[10]	E20	L1_CADIN_L[8]	E21	L1_CADOUT_L[4]	C8
L1_CADIN_H[11]	C19	L1_CADIN_L[9]	D21	L1_CADOUT_L[5]	A10
L1_CADIN_H[12]	C17	L1_CADOUT_H[0]	A3	L1_CADOUT_L[6]	C10
L1_CADIN_H[13]	E16	L1_CADOUT_H[1]	B4	L1_CADOUT_L[7]	A12
L1_CADIN_H[14]	C15	L1_CADOUT_H[10]	D5	L1_CADOUT_L[8]	C3
L1_CADIN_H[15]	E14	L1_CADOUT_H[11]	E5	L1_CADOUT_L[9]	E4
L1_CADIN_H[2]	C20	L1_CADOUT_H[12]	E7	L1_CLKIN_H[0]	C18
L1_CADIN_H[3]	A20	L1_CADOUT_H[13]	D9	L1_CLKIN_H[1]	E18
L1_CADIN_H[4]	A18	L1_CADOUT_H[14]	E9	L1_CLKIN_L[0]	B18
L1_CADIN_H[5]	C16	L1_CADOUT_H[15]	D11	L1_CLKIN_L[1]	E17
L1_CADIN_H[6]	A16	L1_CADOUT_H[2]	A5	L1_CLKOUT_H[0]	A7
L1_CADIN_H[7]	C14	L1_CADOUT_H[3]	B6	L1_CLKOUT_H[1]	D7
L1_CADIN_H[8]	E22	L1_CADOUT_H[4]	B8	L1_CLKOUT_L[0]	A8
L1_CADIN_H[9]	C21	L1_CADOUT_H[5]	A9	L1_CLKOUT_L[1]	C7
L1_CADIN_L[0]	B22	L1_CADOUT_H[6]	B10	L1_CTLIN_H[0]	A14
L1_CADIN_L[1]	A21	L1_CADOUT_H[7]	A11	L1_CTLIN_L[0]	A13
L1_CADIN_L[10]	E19	L1_CADOUT_H[8]	D3	L1_CTLOUT_H[0]	B12
L1_CADIN_L[11]	D19	L1_CADOUT_H[9]	E3	L1_CTLOUT_L[0]	C12
L1_CADIN_L[12]	D17	L1_CADOUT_L[0]	A4	L2_CADIN_H[0]	AJ3
L1_CADIN_L[13]	E15	L1_CADOUT_L[1]	C4	L2_CADIN_H[1]	AL3
L1_CADIN_L[14]	D15	L1_CADOUT_L[10]	C5	L2_CADIN_H[10]	AG5
L1_CADIN_L[15]	E13	L1_CADOUT_L[11]	E6	L2_CADIN_H[11]	AJ6
L1_CADIN_L[2]	B20	L1_CADOUT_L[12]	E8	L2_CADIN_H[12]	AJ8

Table 4. Pin List by Name (Continued)

L2_CADIN_H[13]	AG9	L2_CADOUT_H[1]	AK21	L2_CADOUT_L[7]	AL13
L2_CADIN_H[14]	AJ10	L2_CADOUT_H[10]	AH20	L2_CADOUT_L[8]	AJ22
L2_CADIN_H[15]	AG11	L2_CADOUT_H[11]	AG20	L2_CADOUT_L[9]	AG21
L2_CADIN_H[2]	AJ5	L2_CADOUT_H[12]	AG18	L2_CLKIN_H[0]	AJ7
L2_CADIN_H[3]	AL5	L2_CADOUT_H[13]	AH16	L2_CLKIN_H[1]	AG7
L2_CADIN_H[4]	AL7	L2_CADOUT_H[14]	AG16	L2_CLKIN_L[0]	AK7
L2_CADIN_H[5]	AJ9	L2_CADOUT_H[15]	AH14	L2_CLKIN_L[1]	AG8
L2_CADIN_H[6]	AL9	L2_CADOUT_H[2]	AL20	L2_CLKOUT_H[0]	AL18
L2_CADIN_H[7]	AJ11	L2_CADOUT_H[3]	AK19	L2_CLKOUT_H[1]	AH18
L2_CADIN_H[8]	AG3	L2_CADOUT_H[4]	AK17	L2_CLKOUT_L[0]	AL17
L2_CADIN_H[9]	AJ4	L2_CADOUT_H[5]	AL16	L2_CLKOUT_L[1]	AJ18
L2_CADIN_L[0]	AK3	L2_CADOUT_H[6]	AK15	L2_CTLIN_H[0]	AL11
L2_CADIN_L[1]	AL4	L2_CADOUT_H[7]	AL14	L2_CTLIN_L[0]	AL12
L2_CADIN_L[10]	AG6	L2_CADOUT_H[8]	AH22	L2_CTLOUT_H[0]	AK13
L2_CADIN_L[11]	AH6	L2_CADOUT_H[9]	AG22	L2_CTLOUT_L[0]	AJ13
L2_CADIN_L[12]	AH8	L2_CADOUT_L[0]	AL21	LDTSTOP_L	J6
L2_CADIN_L[13]	AG10	L2_CADOUT_L[1]	AJ21	MEMADD[0]	V25
L2_CADIN_L[14]	AH10	L2_CADOUT_L[10]	AJ20	MEMADD[1]	T25
L2_CADIN_L[15]	AG12	L2_CADOUT_L[11]	AG19	MEMADD[10]	V24
L2_CADIN_L[2]	AK5	L2_CADOUT_L[12]	AG17	MEMADD[11]	J25
L2_CADIN_L[3]	AL6	L2_CADOUT_L[13]	AJ16	MEMADD[12]	J24
L2_CADIN_L[4]	AL8	L2_CADOUT_L[14]	AG15	MEMADD[13]	AE23
L2_CADIN_L[5]	AK9	L2_CADOUT_L[15]	AJ14	MEMADD[2]	P23
L2_CADIN_L[6]	AL10	L2_CADOUT_L[2]	AL19	MEMADD[3]	N23
L2_CADIN_L[7]	AK11	L2_CADOUT_L[3]	AJ19	MEMADD[4]	N25
L2_CADIN_L[8]	AG4	L2_CADOUT_L[4]	AJ17	MEMADD[5]	M24
L2_CADIN_L[9]	AH4	L2_CADOUT_L[5]	AL15	MEMADD[6]	M25
L2_CADOUT_H[0]	AL22	L2_CADOUT_L[6]	AJ15	MEMADD[7]	K25

Table 4. Pin List by Name (Continued)

MEMADD[8]	L23	MEMCLK_LO_L[1]	AA23	MEMDATA[106]	AC27
MEMADD[9]	K23	MEMCLK_LO_L[2]	AD20	MEMDATA[107]	AD28
MEMBANK[0]	W23	MEMCLK_LO_L[3]	J23	MEMDATA[108]	AA28
MEMBANK[1]	W25	MEMCLK_UP_H[0]	R23	MEMDATA[109]	AA26
MEMCAS_L	AA25	MEMCLK_UP_H[1]	L24	MEMDATA[11]	E31
MEMCHECK[0]	R31	MEMCLK_UP_H[2]	AE21	MEMDATA[110]	AC26
MEMCHECK[1]	R29	MEMCLK_UP_H[3]	G20	MEMDATA[111]	AD27
MEMCHECK[10]	R26	MEMCLK_UP_L[0]	T23	MEMDATA[112]	AD26
MEMCHECK[11]	T27	MEMCLK_UP_L[1]	L25	MEMDATA[113]	AE27
MEMCHECK[12]	P25	MEMCLK_UP_L[2]	AE20	MEMDATA[114]	AH29
MEMCHECK[13]	P24	MEMCLK_UP_L[3]	G21	MEMDATA[115]	AJ29
MEMCHECK[14]	T29	MEMCS_L[0]	AA24	MEMDATA[116]	AE29
MEMCHECK[15]	U28	MEMCS_L[1]	AB25	MEMDATA[117]	AF28
MEMCHECK[2]	U30	MEMCS_L[2]	AC25	MEMDATA[118]	AF26
MEMCHECK[3]	V31	MEMCS_L[3]	AC24	MEMDATA[119]	AG27
MEMCHECK[4]	P30	MEMCS_L[4]	AD25	MEMDATA[12]	C28
MEMCHECK[5]	R30	MEMCS_L[5]	AD24	MEMDATA[120]	AJ26
MEMCHECK[6]	U29	MEMCS_L[6]	AE25	MEMDATA[121]	AF25
MEMCHECK[7]	V30	MEMCS_L[7]	AD23	MEMDATA[122]	AH24
MEMCHECK[8]	R24	MEMDATA[0]	B24	MEMDATA[123]	AF23
MEMCHECK[9]	R25	MEMDATA[1]	A25	MEMDATA[124]	AH27
MEMCKE_LO	H25	MEMDATA[10]	E30	MEMDATA[125]	AG26
MEMCKE_UP	H24	MEMDATA[100]	U26	MEMDATA[126]	AH25
MEMCLK_LO_H[0]	U25	MEMDATA[101]	V28	MEMDATA[127]	AG24
MEMCLK_LO_H[1]	Y23	MEMDATA[102]	Y28	MEMDATA[13]	B30
MEMCLK_LO_H[2]	AD21	MEMDATA[103]	Y27	MEMDATA[14]	C31
MEMCLK_LO_H[3]	H23	MEMDATA[104]	AA27	MEMDATA[15]	D31
MEMCLK_LO_L[0]	U24	MEMDATA[105]	AB29	MEMDATA[16]	F30

Table 4. Pin List by Name (Continued)

MEMDATA[17]	F31	MEMDATA[42]	AF31	MEMDATA[68]	F23
MEMDATA[18]	H31	MEMDATA[43]	AF29	MEMDATA[69]	D24
MEMDATA[19]	J31	MEMDATA[44]	AC30	MEMDATA[7]	B27
MEMDATA[2]	A27	MEMDATA[45]	AD31	MEMDATA[70]	E25
MEMDATA[20]	F29	MEMDATA[46]	AF30	MEMDATA[71]	C26
MEMDATA[21]	G31	MEMDATA[47]	AG31	MEMDATA[72]	C27
MEMDATA[22]	J29	MEMDATA[48]	AG30	MEMDATA[73]	E27
MEMDATA[23]	J30	MEMDATA[49]	AH31	MEMDATA[74]	F28
MEMDATA[24]	K31	MEMDATA[5]	C24	MEMDATA[75]	G27
MEMDATA[25]	L31	MEMDATA[50]	AK28	MEMDATA[76]	D27
MEMDATA[26]	N31	MEMDATA[51]	AL28	MEMDATA[77]	D29
MEMDATA[27]	P29	MEMDATA[52]	AG29	MEMDATA[78]	F26
MEMDATA[28]	L29	MEMDATA[53]	AJ31	MEMDATA[79]	F27
MEMDATA[29]	L30	MEMDATA[54]	AK30	MEMDATA[8]	B28
MEMDATA[3]	A28	MEMDATA[55]	AJ28	MEMDATA[80]	H26
MEMDATA[30]	M31	MEMDATA[56]	AL27	MEMDATA[81]	H27
MEMDATA[31]	P31	MEMDATA[57]	AL26	MEMDATA[82]	J28
MEMDATA[32]	V29	MEMDATA[58]	AK24	MEMDATA[83]	L26
MEMDATA[33]	Y30	MEMDATA[59]	AL24	MEMDATA[84]	G29
MEMDATA[34]	AA30	MEMDATA[6]	A26	MEMDATA[85]	H28
MEMDATA[35]	AC31	MEMDATA[60]	AJ27	MEMDATA[86]	K27
MEMDATA[36]	W31	MEMDATA[61]	AK27	MEMDATA[87]	K29
MEMDATA[37]	Y31	MEMDATA[62]	AK25	MEMDATA[88]	L27
MEMDATA[38]	AA29	MEMDATA[63]	AJ24	MEMDATA[89]	M27
MEMDATA[39]	AB31	MEMDATA[64]	G23	MEMDATA[9]	A29
MEMDATA[4]	A24	MEMDATA[65]	E24	MEMDATA[90]	P26
MEMDATA[40]	AC29	MEMDATA[66]	F25	MEMDATA[91]	P27
MEMDATA[41]	AD30	MEMDATA[67]	E26	MEMDATA[92]	L28

Table 4. Pin List by Name (Continued)

MEMDATA[93]	M26	MEMDQS[28]	E29	NC_AE14	AE14
MEMDATA[94]	N29	MEMDQS[29]	J27	NC_AE9	AE9
MEMDATA[95]	P28	MEMDQS[3]	M29	NC_AF11	AF11
MEMDATA[96]	U27	MEMDQS[30]	N27	NC_AF13	AF13
MEMDATA[97]	V27	MEMDQS[31]	W29	NC_AF15	AF15
MEMDATA[98]	W27	MEMDQS[32]	AB27	NC_AF9	AF9
MEMDATA[99]	Y26	MEMDQS[33]	AF27	NC_AG1	AG1
MEMDQS[0]	C25	MEMDQS[34]	AG25	NC_AG13	AG13
MEMDQS[1]	C29	MEMDQS[35]	R27	NC_AG14	AG14
MEMDQS[10]	C30	MEMDQS[4]	Y29	NC_AH12	AH12
MEMDQS[11]	H30	MEMDQS[5]	AE31	NC_AH2	AH2
MEMDQS[12]	M30	MEMDQS[6]	AL29	NC_AJ12	AJ12
MEMDQS[13]	AA31	MEMDQS[7]	AL25	NC_AJ2	AJ2
MEMDQS[14]	AD29	MEMDQS[8]	T31	NC_C13	C13
MEMDQS[15]	AJ30	MEMDQS[9]	B25	NC_D13	D13
MEMDQS[16]	AJ25	MEMRAS_L	Y25	NC_E11	E11
MEMDQS[17]	U31	MEMRESET_L	G25	NC_E12	E12
MEMDQS[18]	D25	MEMVREF0	F22	NC_F7	F7
MEMDQS[19]	E28	MEMVREF1	AF22	NC_G14	G14
MEMDQS[2]	H29	MEMWE_L	Y24	NC_G6	G6
MEMDQS[20]	J26	MEMZN	AF17	NC_H12	H12
MEMDQS[21]	M28	MEMZP	AE16	NC_H13	H13
MEMDQS[22]	V26	NC_AA6	AA6	NC_H14	H14
MEMDQS[23]	AC28	NC_AC6	AC6	NC_H7	H7
MEMDQS[24]	AG28	NC_AE10	AE10	NC_H9	H9
MEMDQS[25]	AF24	NC_AE11	AE11	NC_K8	K8
MEMDQS[26]	R28	NC_AE12	AE12	NC_L8	L8
MEMDQS[27]	F24	NC_AE13	AE13	NC_M23	M23

Table 4. Pin List by Name (Continued)

NC_N6	N6	VDD	D12	VDD	N9
NC_R6	R6	VDD	D16	VDD	N11
NC_T3	T3	VDD	D20	VDD	N13
NC_T4	T4	VDD	F6	VDD	N15
NC_T7	T7	VDD	F11	VDD	N17
NC_U5	U5	VDD	F15	VDD	N19
NC_U6	U6	VDD	F18	VDD	P6
NC_V23	V23	VDD	F19	VDD	P10
NC_V5	V5	VDD	G7	VDD	P12
NC_W6	W6	VDD	H2	VDD	P14
PRESENCE_DET	AK2	VDD	J4	VDD	P16
PWROK	F12	VDD	J13	VDD	P18
RESET_L	G12	VDD	K6	VDD	P20
TCK	AE7	VDD	K12	VDD	R9
TDI	AF7	VDD	K18	VDD	R11
TDO	AE8	VDD	L9	VDD	R13
THERMDA	AJ1	VDD	L11	VDD	R15
THERMDC	AH1	VDD	L13	VDD	R17
THERMTRIP_L	AE15	VDD	L15	VDD	R19
TMS	AE6	VDD	L17	VDD	T2
TRST_L	AD7	VDD	M2	VDD	T8
VDD	B5	VDD	M10	VDD	T10
VDD	B9	VDD	M12	VDD	T12
VDD	B13	VDD	M14	VDD	T14
VDD	B17	VDD	M16	VDD	T16
VDD	B21	VDD	M18	VDD	T18
VDD	D4	VDD	M20	VDD	T20
VDD	D8	VDD	N4	VDD	U4

Table 4. Pin List by Name (Continued)

VDD	U9	VDD	AA11	VDDA2	D2
VDD	U11	VDD	AA13	VDDA3	C2
VDD	U13	VDD	AA15	VDDIO	A23
VDD	U15	VDD	AA17	VDDIO	C23
VDD	U17	VDD	AB6	VDDIO	D26
VDD	U19	VDD	AB8	VDDIO	D28
VDD	V6	VDD	AB12	VDDIO	E23
VDD	V10	VDD	AB18	VDDIO	G26
VDD	V12	VDD	AC13	VDDIO	G28
VDD	V14	VDD	AD2	VDDIO	H22
VDD	V16	VDD	AD12	VDDIO	J21
VDD	V18	VDD	AD14	VDDIO	K20
VDD	V20	VDD	AD16	VDDIO	K22
VDD	W9	VDD	AE4	VDDIO	K26
VDD	W11	VDD	AF6	VDDIO	K28
VDD	W13	VDD	AF10	VDDIO	L19
VDD	W15	VDD	AF14	VDDIO	L21
VDD	W17	VDD	AH5	VDDIO	M22
VDD	W19	VDD	AH9	VDDIO	N21
VDD	Y2	VDD	AH13	VDDIO	N26
VDD	Y10	VDD	AH17	VDDIO	N28
VDD	Y12	VDD	AH21	VDDIO	P22
VDD	Y14	VDD	AK4	VDDIO	R21
VDD	Y16	VDD	AK8	VDDIO	T22
VDD	Y18	VDD	AK12	VDDIO	T26
VDD	Y20	VDD	AK16	VDDIO	T28
VDD	AA4	VDD	AK20	VDDIO	U21
VDD	AA9	VDDA1	C1	VDDIO	U23

Table 4. Pin List by Name (Continued)

VDDIO	V22	VLDT_0	M8	VSS	B7
VDDIO	W21	VLDT_0	N7	VSS	B11
VDDIO	W26	VLDT_0	P8	VSS	B15
VDDIO	W28	VLDT_0	R7	VSS	B19
VDDIO	Y22	VLDT_0	U7	VSS	B23
VDDIO	AA19	VLDT_0	V8	VSS	B26
VDDIO	AA21	VLDT_0	W7	VSS	B29
VDDIO	AB20	VLDT_0	Y8	VSS	D6
VDDIO	AB22	VLDT_0	AA7	VSS	D10
VDDIO	AB26	VLDT_1	H8	VSS	D14
VDDIO	AB28	VLDT_1	H10	VSS	D18
VDDIO	AC21	VLDT_1	J9	VSS	D22
VDDIO	AD22	VLDT_1	J11	VSS	D23
VDDIO	AE26	VLDT_1	J15	VSS	D30
VDDIO	AE28	VLDT_1	J16	VSS	E2
VDDIO	AG23	VLDT_1	K10	VSS	F1
VDDIO	AH26	VLDT_1	K14	VSS	F2
VDDIO	AH28	VLDT_1	K16	VSS	F5
VDDIO	AJ23	VLDT_2	AB10	VSS	F8
VDDIO	AL23	VLDT_2	AB14	VSS	F10
VDDIO_SENSE	AF20	VLDT_2	AB16	VSS	F13
VDDIOFB_H	AB23	VLDT_2	AC9	VSS	F14
VDDIOFB_L	AC23	VLDT_2	AC11	VSS	F16
VID[0]	G11	VLDT_2	AC15	VSS	F17
VID[1]	H11	VLDT_2	AC16	VSS	G4
VID[2]	G10	VLDT_2	AD8	VSS	G13
VID[3]	F9	VLDT_2	AD10	VSS	G15
VID[4]	G9	VSS	B3	VSS	G17

Table 4. Pin List by Name (Continued)

VSS	G22	VSS	L16	VSS	P15
VSS	G24	VSS	L18	VSS	P17
VSS	G30	VSS	L20	VSS	P19
VSS	H6	VSS	L22	VSS	P21
VSS	H15	VSS	M6	VSS	R4
VSS	H17	VSS	M7	VSS	R8
VSS	J8	VSS	M9	VSS	R10
VSS	J10	VSS	M11	VSS	R12
VSS	J12	VSS	M13	VSS	R14
VSS	J14	VSS	M15	VSS	R16
VSS	J17	VSS	M17	VSS	R18
VSS	J18	VSS	M19	VSS	R20
VSS	J20	VSS	M21	VSS	R22
VSS	J22	VSS	N8	VSS	T6
VSS	K2	VSS	N10	VSS	T9
VSS	K9	VSS	N12	VSS	T11
VSS	K11	VSS	N14	VSS	T13
VSS	K13	VSS	N16	VSS	T15
VSS	K15	VSS	N18	VSS	T17
VSS	K17	VSS	N20	VSS	T19
VSS	K19	VSS	N22	VSS	T21
VSS	K21	VSS	N24	VSS	T24
VSS	K24	VSS	N30	VSS	T30
VSS	K30	VSS	P2	VSS	U8
VSS	L4	VSS	P7	VSS	U10
VSS	L10	VSS	P9	VSS	U12
VSS	L12	VSS	P11	VSS	U14
VSS	L14	VSS	P13	VSS	U16

Table 4. Pin List by Name (Continued)

VSS	U18	VSS	Y15	VSS	AC20
VSS	U20	VSS	Y17	VSS	AC22
VSS	U22	VSS	Y19	VSS	AD6
VSS	V2	VSS	Y21	VSS	AD9
VSS	V7	VSS	AA8	VSS	AD11
VSS	V9	VSS	AA10	VSS	AD13
VSS	V11	VSS	AA12	VSS	AD15
VSS	V13	VSS	AA14	VSS	AD17
VSS	V15	VSS	AA16	VSS	AE17
VSS	V17	VSS	AA18	VSS	AE22
VSS	V19	VSS	AA20	VSS	AE24
VSS	V21	VSS	AA22	VSS	AE30
VSS	W4	VSS	AB2	VSS	AF2
VSS	W8	VSS	AB7	VSS	AF8
VSS	W10	VSS	AB9	VSS	AF12
VSS	W12	VSS	AB11	VSS	AF16
VSS	W14	VSS	AB13	VSS	AF21
VSS	W16	VSS	AB15	VSS	AG2
VSS	W18	VSS	AB17	VSS	AH3
VSS	W20	VSS	AB19	VSS	AH7
VSS	W22	VSS	AB21	VSS	AH11
VSS	W24	VSS	AB24	VSS	AH15
VSS	W30	VSS	AB30	VSS	AH19
VSS	Y6	VSS	AC4	VSS	AH23
VSS	Y7	VSS	AC10	VSS	AH30
VSS	Y9	VSS	AC12	VSS	AK6
VSS	Y11	VSS	AC14	VSS	AK10
VSS	Y13	VSS	AC17	VSS	AK14

Table 4. Pin List by Name (Continued)

VSS	AK18
VSS	AK22
VSS	AK23
VSS	AK26
VSS	AK29
VTT	AF18
VTT	F20
VTT	F21
VTT	G19
VTT	H19
VTT	J19
VTT	AC18
VTT	AC19
VTT	AE18
VTT	AE19
VTT_SENSE	AF19

6 Pin Descriptions

Table 5 describes the terms used in the pin description tables found in this chapter. The pins are organized within the following functional groups:

- HyperTransport™ technology interface
- DDR SDRAM memory interface
- Miscellaneous pins, including clock, JTAG, and debug pins

All pins are described in the tables beginning on page 40.

Table 5. Pin Description Table Definitions

Pin Types		Applicable Section in Electrical Chapter
I-HT	Input, HyperTransport™ technology, Differential	"HyperTransport™ Technology Interface" on page 48
O-HT	Output, HyperTransport technology, Differential	"HyperTransport™ Technology Interface" on page 48
B-IOS	Bidirectional, VDDIO[1] Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 51
I-IOS	Input, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 51
I-IOD	Input, VDDIO[1], Differential	"Clock Pins" on page 63
O-IOD	Output, VDDIO[1], Differential	"Clock Pins" on page 63
O-IOS	Output, VDDIO[1], Single-Ended	"DDR SDRAM and Miscellaneous Pins" on page 51
O-IO-OD	Output, VDDIO[1], Open Drain	"DDR SDRAM and Miscellaneous Pins" on page 51
A	Analog	"Power Supplies" on page 72
S	Supply Voltage	"Power Supplies" on page 72
VREF	Voltage Reference	"DDR SDRAM and Miscellaneous Pins" on page 51

Notes:
1. *Refer to Table 33, "Combined AC and DC Operating Conditions for Power Supplies," on page 72 for VDDIO voltage specifications.*

6.1 HyperTransport™ Technology Pins

Table 6. HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[0]	I-HT	Link 0 Control Input
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L1_CLKIN_H/L[1:0]	I-HT	Link 1 Clock Input
L1_CTLIN_H/L[0]	I-HT	Link 1 Control Input
L1_CADIN_H/L[15:0]	I-HT	Link 1 Command/Address/Data Input
L1_CLKOUT_H/L[1:0]	O-HT	Link 1 Clock Outputs
L1_CTLOUT_H/L[0]	O-HT	Link 1 Control Output
L1_CADOUT_H/L[15:0]	O-HT	Link 1 Command/Address/Data Outputs
L2_CLKIN_H/L[1:0]	I-HT	Link 2 Clock Input
L2_CTLIN_H/L[0]	I-HT	Link 2 Control Input
L2_CADIN[15:0]	I-HT	Link 2 Command/Address/Data Input
L2_CLKOUT_H/L[1:0]	O-HT	Link 2 Clock Outputs
L2_CTLOUT_H/L[0]	O-HT	Link 2 Control Output
L2_CADOUT_H/L[15:0]	O-HT	Link 2 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT[1]
L0_REF0	A	Compensation Resistor to VSS[1]

Notes:

1. *These pins are used in an alternating fashion to compensate* R_{TT} *by internal comparison to 3/4 VLDT and 1/4 VLDT and compensate* R_{ON} *by comparison to each other around 1/2 VLDT. For proper resistor value, see the* AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180.*

6.2 DDR SDRAM Memory Interface Pins

Table 7. DDR SDRAM Memory Interface Pin Descriptions

Signal Name	Type	Description
MEMCLK_UP_H/L[3]	O-IOD	DRAM Clock connected to DIMM3 for the upper half of the data bus
MEMCLK_UP_H/L[2]	O-IOD	DRAM Clock connected to DIMM2 for the upper half of the data bus
MEMCLK_UP_H/L[1]	O-IOD	DRAM Clock connected to DIMM1 for the upper half of the data bus
MEMCLK_UP_H/L[0]	O-IOD	DRAM Clock connected to DIMM0 for the upper half of the data bus
MEMCLK_LO_H/L[3]	O-IOD	DRAM Clock connected to DIMM3 for the lower half of the data bus
MEMCLK_LO_H/L[2]	O-IOD	DRAM Clock connected to DIMM2 for the lower half of the data bus
MEMCLK_LO_H/L[1]	O-IOD	DRAM Clock connected to DIMM1 for the lower half of the data bus
MEMCLK_LO_H/L[0]	O-IOD	DRAM Clock connected to DIMM0 for the lower half of the data bus
MEMCKE_UP	O-IOS	DRAM Clock Enable
MEMCKE_LO	O-IOS	DRAM Clock Enable
MEMDQS[35]	B-IOS	DRAM Data Strobe synchronous with MEMCHECK[15:12] for x4 DIMMs.
MEMDQS[34:27]	B-IOS	DRAM Data Strobe synchronous with the high-order nibbles of MEMDATA[127:64] for x4 DIMMs
MEMDQS[26]	B-IOS	DRAM data strobe synchronous with MEMCHECK[11:8] for x4 DIMMs and MEMCHECK[15:8] for x8/x16 DIMMs.
MEMDQS[25:18]	B-IOS	DRAM Data Strobe synchronous with the low-order nibbles of MEMDATA[127:64] for x4 DIMMs and all nibbles for x8/x16 DIMMs
MEMDQS[17]	B-IOS	DRAM Data Strobe synchronous with MEMCHECK[7:4] for x4 DIMMs
MEMDQS[16:9]	B-IOS	DRAM Data Strobe synchronous with high-order nibbles of MEMDATA[63:0] for x4 DIMMs
MEMDQS[8]	B-IOS	DRAM Data Strobe synchronous with MEMCHECK[3:0] for x4 DIMMs and MEMCHECK[7:0] for x8/x16 DIMMs
MEMDQS[7:0]	B-IOS	DRAM Data Strobe synchronous with low-order nibbles of MEMDATA[127:64] for x4 DIMMs and all nibbles for x8/x16 DIMMs
MEMDATA[127:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[15:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects[1]
MEMRAS_L	O-IOS	DRAM Row Address Select
MEMCAS_L	O-IOS	DRAM Column Address Select

Table 7. DDR SDRAM Memory Interface Pin Descriptions (Continued)

Signal Name	Type	Description
MEMWE_L	O-IOS	DRAM Write Enable
MEMADD[13:0]	O-IOS	DRAM Column/Row Address
MEMBANK[1:0]	O-IOS	DRAM Bank Address
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference[1]
MEMZP	A	Compensation Resistor tied to VSS[1]
MEMZN	A	Compensation Resistor tied to 2.5 V[1]

Notes:
1. *For connection details and proper resistor values, see the* AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide, *order# 25180.*

6.3 Miscellaneous Pins

Table 8. Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

Table 9. Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125^{o}C.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_0 VLDT_1 VLDT_2	S	HyperTransport™ I/O ring power supply
VTT	S	VTT regulator voltage

Table 9. Miscellaneous Pin Descriptions (Continued)

Signal Name	Type	Description
PRESENCE_DET	S	This pin can be connected to VSS or used for detection of the processor in multiprocessor configurations. When used as a presence detection bit it should be pulled up and sensed via the circuitry that is used to detect installed processors on the motherboard. This pin is connected to VSS internally.
VSS	S	Ground

Table 10. VID[4:0] Encoding

VID[4:0]	VDD	VID[4:0]	VDD	VID[4:0]	VDD	VID[4:0]	VDD
0x00000	1.550 V	0x01000	1.350 V	0x10000	1.150 V	0x11000	0.950 V
0x00001	1.525 V	0x01001	1.325 V	0x10001	1.125 V	0x11001	0.925 V
0x00010	1.500 V	0x01010	1.300 V	0x10010	1.100 V	0x11010	0.900 V
0x00011	1.475 V	0x01011	1.275 V	0x10011	1.075 V	0x11011	0.875 V
0x00100	1.450 V	0x01100	1.250 V	0x10100	1.050 V	0x11100	0.850 V
0x00101	1.425 V	0x01101	1.225 V	0x10101	1.025 V	0x11101	0.825 V
0x00110	1.400 V	0x01110	1.200 V	0x10110	1.000 V	0x11110	0.800 V
0x00111	1.375 V	0x01111	1.175 V	0x10111	0.975 V	0x11111	Off

Table 11. JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Table 12. Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

6.4 Pin States at Reset

The default pin states are listed below. These are listed for all output and bidirectional pins in the power-on reset state (reset) as well as the ACPI S1 and S3 power management states.

Table 13. Reset Pin State

Pin Name	Reset State	S1 State	S3 State	Comments
L*_CLKOUT*	T	Z	Z	Tristated in S1 only if programmed to do so.
L*_CTLOUT*	0	Z	Z	Tristated in S1 only if programmed to do so.
L*_CADOUT*	1	Z	Z	Tristated in S1 only if programmed to do so.
MEMCLK*	Z	Z	Z	
MEMDQS*	Z	Z	Z	
MEMCKE*	0	0	0	In S3, MEMCKE* is forced to a logic Low.
MEMDATA*	Z	Z	Z	
MEMCHECK*	Z	Z	Z	
MEMCS_L*	1	Z	Z	
MEMRAS_L	1	Z	Z	
MEMCAS_L	1	Z	Z	
MEMWE_L	1	Z	Z	
MEMADD*	0	Z	Z	
MEMBANK*	0	Z	Z	
MEMRESET_L	0	0	0	In S3, MEMRESET_L is forced to logic 0.
MEMZN	1	1	1	
MEMZP	0	0	0	
FBCLKOUT*	T	T	Z	
TDO	X	X	Z	
DBRDY	0	0	Z	
VID[4:0]	X	X	X	
THERMTRIP_L	Z	X	Z	

For differential inputs, “0” and “1” refer to the high-end differential output. Low-end differential outputs are inverted. Definitions of pin states: X: Either logic 1 or 0, Z: Tristated, T: Toggling between 0 and 1

7 Electrical Data

7.1 Absolute Maximum Ratings

Stresses greater than those listed in Table 14 may cause permanent damage to the device and motherboard. Systems using this device must be designed to ensure that these parameters are not violated. Violation of these ratings will void the product warranty. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Absolute Maximum Ratings for AMD Opteron™ Processor

Characteristic	Range
Storage Temperature	–55°C to 85°C
VLDT supply voltage relative to VSS	–0.3 V to 1.5 V
VDD supply voltage relative to VSS	–0.3 V to 1.65 V
VTT supply voltage relative to VSS	–0.3 V to 1.65 V
VDDIO supply voltage relative to VSS	–1 V to 2.9 V
VDDA supply voltage relative to VSS	–0.3 V to 3.0 V
MEMVREF input voltage relative to VSS	–1 V to 2.9 V
Input voltage relative to VSS for HyperTransport™ technology interface	–0.3 V to 1.5 V
Differential input voltage for HyperTransport™ technology interface	–1.5 V to 1.5 V
Input voltage relative to VSS for DDR SDRAM memory interface and Miscellaneous pins	–1 V to 2.9V

Refer to *AMD Opteron™ Processor Power and Thermal Data Sheet*, order# 30417, for maximum case temperature specifications.

7.2 HyperTransport™ Technology Interface

7.2.1 Operating Conditions

Table 15. DC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output Differential Voltage	mV	495	600	715	1, 2
V_{OCM}	Output Common Mode Voltage	mV	495	600	715	1, 2
V_{ID}	Input Differential Voltage	mV	200	600	1000	1, 2
V_{ICM}	Input Common Mode Voltage	mV	440	600	780	1, 2
DeltaV_{OD}	Change in V_{OD} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{ID}	Change in V_{ID} from 0 to 1 State	mV	–15	0	15	1
DeltaV_{ICM}	Change in V_{ICM} from 0 to 1 State	mV	–15	0	15	1
I_l	Input Leakage Current	mA	–1		1	
I_{OZ}	Output Tristate Leakage Current	mA	–1		1	
R_{ON}	Output Driver Impedance	ohm	45	50	55	
DeltaR_{ON}	Change in R_{ON} Driving 0=>1 or 1=>0	%	–2.5	0	2.5	
R_{TT}	Input Differential Impedance	ohm	90	100	110	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured at <100 MHz, considered slow enough to attain both 0 and 1 logic state voltage levels without AC transients on signals and supplies.*

Table 16. AC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output Differential Voltage	mV	400		820	1
V_{OCM}	Output Common Mode Voltage	mV	440		780	1
V_{ID}	Input Differential Voltage	mV	300		900	1
V_{ICM}	Input Common Mode Voltage	mV	385		845	1
$DeltaV_{OD}$	Change in V_{OD} from 0 to 1 State	mV	–75		75	1
$DeltaV_{OCM}$	Change in V_{OCM} from 0 to 1 State	mV	–50		50	1
$DeltaV_{ID}$	Change in V_{ID} from 0 to 1 State	mV	–125		125	1
$DeltaV_{ICM}$	Change in V_{ICM} from 0 to 1 State	mV	–100		100	1
T_{RISE}	Input Rising Edge Rate	V/ns	1		4	1, 2
T_{FALL}	Input Falling Edge Rate	V/ns	1		4	1, 2
C_{IN}	Input Pad Capacitance	pF			2	
C_{OUT}	Output Pad Capacitance	pF			3	
C_{DELTA}	C_{IN} Pad Capacitance Range Across Group	pF			0.5	
T_{CADV}	Output CAD Valid	pS	166		459	3
TPHERR	Accumulated Phase Error, CLKIN_H/L to L*_CLKOUT_H/L[1:0]	pS	0		5000	
T_{SU}	Device Setup Time	pS			110	3, 4
T_{HLD}	Device Hold Time	pS			110	3, 4
R_{TT}	Input Differential Impedance	ohm	90	100	110	
R_{ON}	Output Impedance	ohm	45	50	55	
$DeltaR_{ON}$	Change in R_{ON} Driving 0=>1 or 1=>0	%	–2.5		2.5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured in a differential fashion relative to the complement signal.*
3. *Measured from crossing points of differential pairs.*
4. *Input setup and hold times are measured from the crossing point of CAD versus the crossing point of CLK, effectively including the edge time to achieve VID min AC.*

7.2.2 Reference Information

Table 17. Internal Termination for HyperTransport™ Technology Interface

Pin	Internal Termination	Value	Tolerance
L*_CADIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L*_CTLIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%
L*_CLKIN*	Differential R_{TT}	100 ohm (PVT-compensated)	±10%

7.3 DDR SDRAM and Miscellaneous Pins

This section includes electrical specifications for all DDR SDRAM pins described in "DDR SDRAM Memory Interface Pins" on page 41, and the **THERMTRIP_L**, **RESET_L**, **LDTSTOP_L**, **PWROK**, **VID[4:0]**, **TCK**, **TMS**, **TRST_L**, **TDI**, **TDO**, **DBREQ_L**, and **DBRDY** pins described in "Miscellaneous Pins" on page 43.

7.3.1 Operating Conditions

Table 18. DC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	$0.49*V_{DDIO\_dc}$ Min	$0.5*V_{DDIO\_dc}$	$0.51*V_{DDIO\_dc}$ Max	1, 12
I_l	Input leakage current Any input: $0 \leq V_{IN} \leq V_{DDIO}$ V (All other pins not under test = 0V)	mA	-1		1	
I_{oz}	Output leakage current Any output: $0 \leq V_{OUT} \leq V_{DDIO}$ V	mA	-1		1	
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.15	-	-	2
V_{IL}	Input low voltage (logic 0)	V	-	-	V_{ref} - 0.15	2
V_{OH}	Output high voltage (logic 1) (for VID[4:0])	V	2.0			
	Output high voltage (logic 1) (for all other pins)	V	1.8			
V_{OL}	Output low voltage (logic 0)	V			0.65	
I_{OH}	Output levels -Output high current ($V_{OUT}= V_{DDIO}/2$)	mA	-25	-28	-33	3
I_{OL}	Output levels - Output low current ($V_{OUT}=V_{DDIO}/2$)	mA	25	28	32	3
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.2	1.3	1.4	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-100	-	100	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	1.1	1.25	1.4	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-100	-	100	7

Notes:

The notes for Table 18 through Table 21 appear on page 54.

Table 19. AC Operating Conditions

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ref}	Reference voltage (for I/O), MEMVREF pin	V	V_{ref}(DC) - 2%		V_{ref}(DC) + 2%	1
V_{IH}	Input high voltage (logic 1)	V	V_{ref} + 0.35	-		2
V_{IL}	Input low voltage (logic 0)	V		-	V_{ref} - 0.35	2
V_{OD}	Differential output voltage (for CK & $\overline{CK}$)	V	1.0	1.3	1.6	4
ΔV_{OD}	Change in V_{OD} magnitude	mV	-150	-	150	5
V_{OCM}	Output common mode voltage (for CK & $\overline{CK}$)	V	0.9	1.25	1.6	6
ΔV_{OCM}	Change in V_{OCM} magnitude	mV	-200	-	200	7

Table 20. Input Capacitance

Symbol	Parameters	Unit	Min	Typ	Max	Notes
C_{in}	Input capacitance (DQ & DQS)	pF	3.0	3.5	4.0	
ΔC	Delta Input capacitance	pF	-	-	0.4	8

Table 21. Slew Rate of DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
S_{OUT}	Output slew rate (pullup and pull-down)	V/ns	2	3	4	9
S_{OUT_Ratio}	Output slew rate ratio between pullup and pulldown		0.75	1	1.25	10
S_{in}	Input slew rate	V/ns	0.5		4	11

1. *V_{ref} is expected to be equal to $0.5*V_{DDIO}$ and to track variations in the DC level of the same. Peak to peak noise on V_{ref} may not exceed $\pm$ 2% of the DC value.*
2. *The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. The receiver effectively switches to the new logic state when receiver input crosses the AC level. The new logic state is maintained as long as the input stays beyond the DC threshold.*
3. *With compensation the granularity between NMOS current and PMOS current cannot exceed 3mA. The range is 6mA due to 10% variation.*
4. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
5. *ΔV_{OD} is the change in magnitude between the differential output voltage while driving a logic 0 and while driving a logic 1.*
6. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage magnitude relative to ground under DC or AC conditions.*
7. *ΔV_{OCM} is the change in magnitude between the output common mode voltage while driving a logic 0 and while driving a logic 1.*
8. *ΔC means the difference in capacitance between any MEMDATA/MEMDQS pin to any other MEMDATA/MEMDQS pin.*
9. *Pullup and pulldown slew rate is measured into R_{TT} (50 Ohms) to V_{TT} as shown in Figure 4. The slew rate is measured between $V_{ref} \pm$ 300 mV. It is designed for any pattern of data, including all outputs switching and only one output switching.*
10. *The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.*
11. *The slew rate is measured at the CPU pin between $V_{ref} \pm$ 150 mV. Minimum and maximum input slew rate specification is set based on DRAM output slew rate specification.*
12. *VDDIO_dc is defined in Table 33 on page 72.*

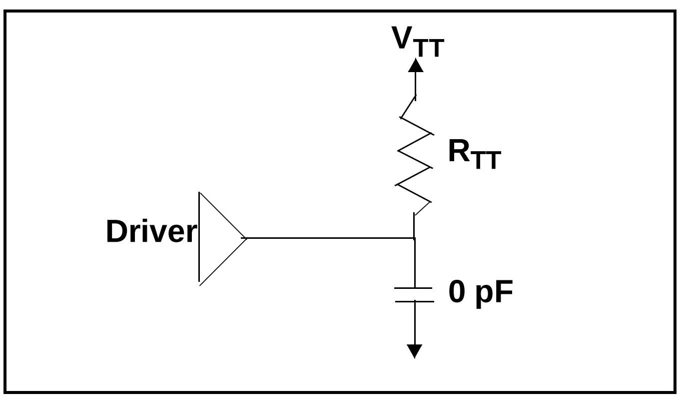


Figure 4. Slew Rate Measurement Example

Table 22. Package Routing Skew

Routing Measurement	Skew (ps)
Any MEMCLK clock pair to any other MEMCLK clock pair	± 100
Any MEMCLK pair to any MEMDQS pair	± 100
Any MEMDQS pair to any MEMDATA associated within pair	± 75
Any MEMCLK pair to any MEMADD/CMD	± 100
Pad skew	± 250

7.3.2 AC Operating Characteristics

Table 23. Electrical AC Timing Characteristics for DDR SDRAM Signals

Symbol	Parameters	Unit	Min	Typ	Max	Notes
tCK	MEMCLK cycle time	ps	5000	-	10000	15
tCH	MEMCLK high pulse width	ps	0.45*tCK	-	0.55*tCK	
tCL	MEMCLK low pulse width	ps	0.45*tCK	-	0.55*tCK	
tCKS	MEMCLK output skew	ps	-350	-	350	1,2,3
tDQSH	MEMDQS high pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQSL	MEMDQS low pulse width	ps	0.45*tCK	-	0.55*tCK	1
tDQS	MEMCLK to MEMDQS	ps	-350	-	350	1,4,5
tDSS	MEMDQS falling edge to MEMCLK rising edge	ps	0.45*tCK - 350	-	-	1,6,7
tDSH	MEMCLK rising edge to MEMDQS falling edge	ps	0.45*tCK - 350	-	-	1,6,7
tDQSQV	MEMDQS to MEMDATA shift (when data becomes valid)	ps	-{0.5* tDQSHmax - [638]}	-	-{0.5* tDQSHmin + [638]}	1,8,9
tDQSQIV	MEMDQS to MEMDATA shift (when data becomes invalid)	ps	{0.5*tDQSHmin - [638]}	-	{0.5* tDQSHmax + [638]}	1,8,9
t2	MEMADD/CMD to MEMCLK (Registered DIMM environment - MEMADD/CMD are launched 1/2 clock early)	ps	- 350	-	350	1,10,11
t3	MEMDATA edge arrival relative to MEMDQS	ps	-{tCK/4 - [350+0.2* (tCK/4)]}	-	tCK/4 - [350+0.2* (tCK/4)]	12,13,14

1. *Write cycle timing parameter*
2. *The skew consists of pad output skew (± 250ps) and package routing skew between any two clock pairs (± 100ps).*
3. *tCKS Timing Parameter, refer to Figure 5 on page 58.*
4. *The timing consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps).*
5. *tDQS Timing parameter, refer to Figure 6 on page 58.*
6. *The skew consists of pad output skew (± 250ps) and package routing skew between any MEMCLK to any MEMDQS (± 100ps). Minimum DQS pulse width is 45% of MEMCLK.*
7. *tDSS, tDSH timing parameters, refer to Figure 7 on page 59.*
8. *During write, DQ signals are driven quarter clock earlier such that DQS is placed in the center of data eye window. The skew consists of pad output skew (± 250ps), package routing skew between any DQS signals and it's associated DQ signals (± 75ps) and maximum clock granularity (± 312.5 ps).*

9. *tDQSQV and tDQSQIV timing parameters apply only within DQS and its associated DQ signals. Refer to Figure 8 on page 60.*
10. *The skew consists of pad output skew (± 250 ps) and package routing skew (± 100 ps) between any MEMCLK pair to any MEMADD/CMD signal. Maximum clock granularity skew is 312.5 ps.*
11. *t2 Timing parameter, applies to registered DIMM Environment Only - MEMADD/CMD signals are launched 1/2 clock cycle early. The granularity term does not apply here. Refer to Figure 9 on page 61.*
12. *Read cycle timing parameter.*
13. *The PDL placement uncertainty is 20%. Package skew between DQS and its associated DQs is 75ps. The sum of setup/hold time & receiver uncertainty is 275ps.*
14. *t3 timing parameter, refer to Figure 10 on page 62.*
15. *The slow operation of 10ns cycle time is specifically included for functional test purpose only. All electrical characterization will be performed at full speed however all functional tests will be performed at 10ns cycle time.*

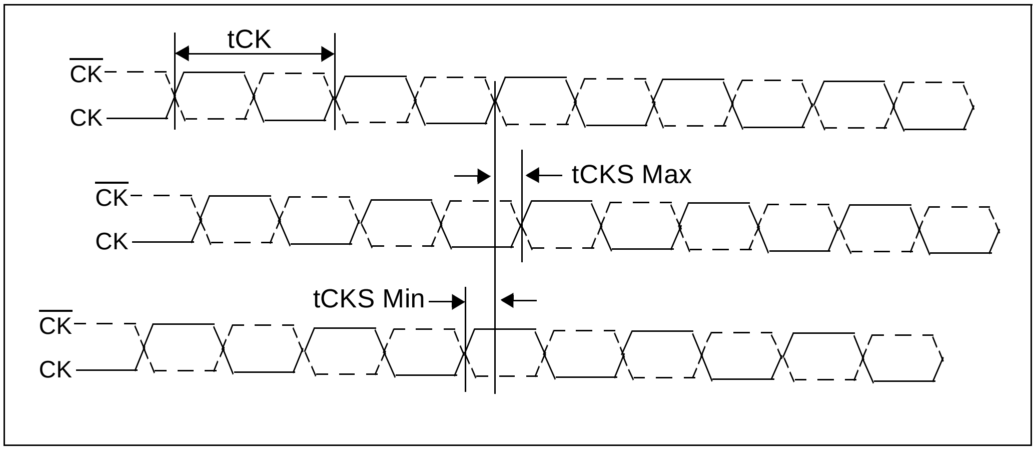


Figure 5. MEMCLK Output Skew

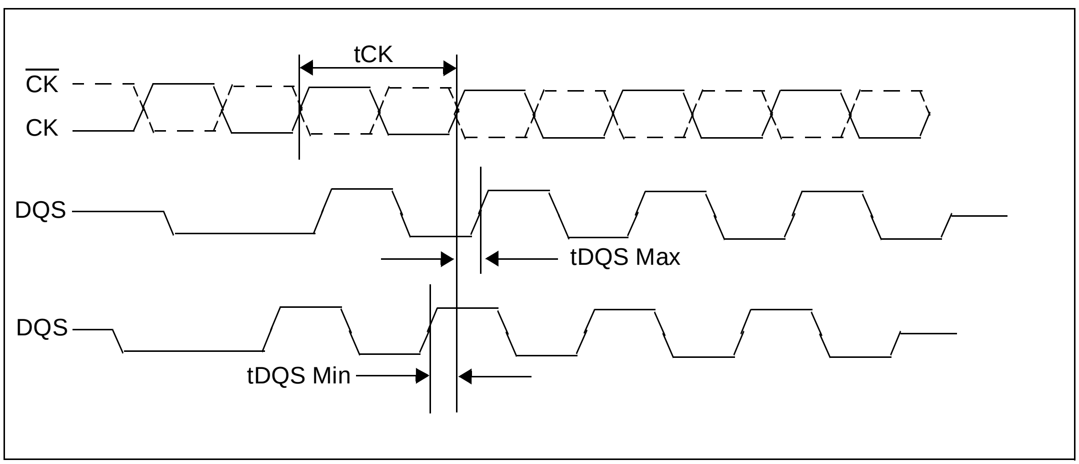


Figure 6. MEMDQS Timing Parameter

t

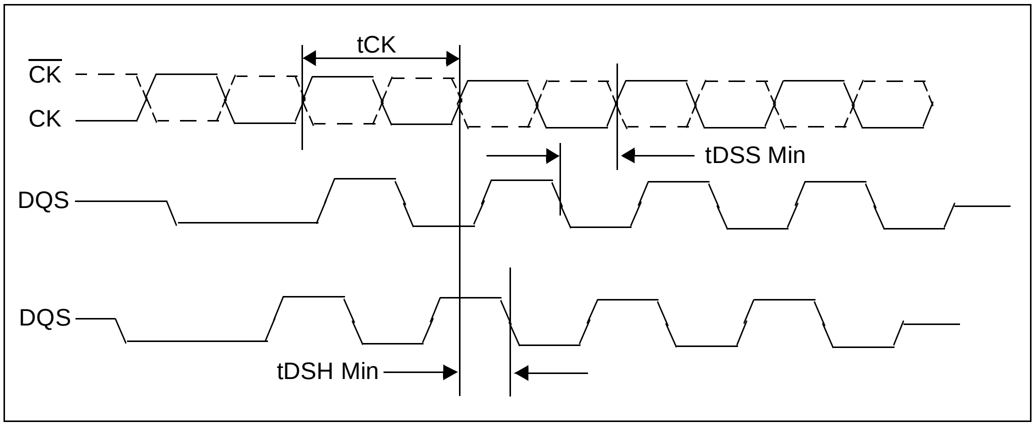


Figure 7. DSS/tDSH Timing Parameters

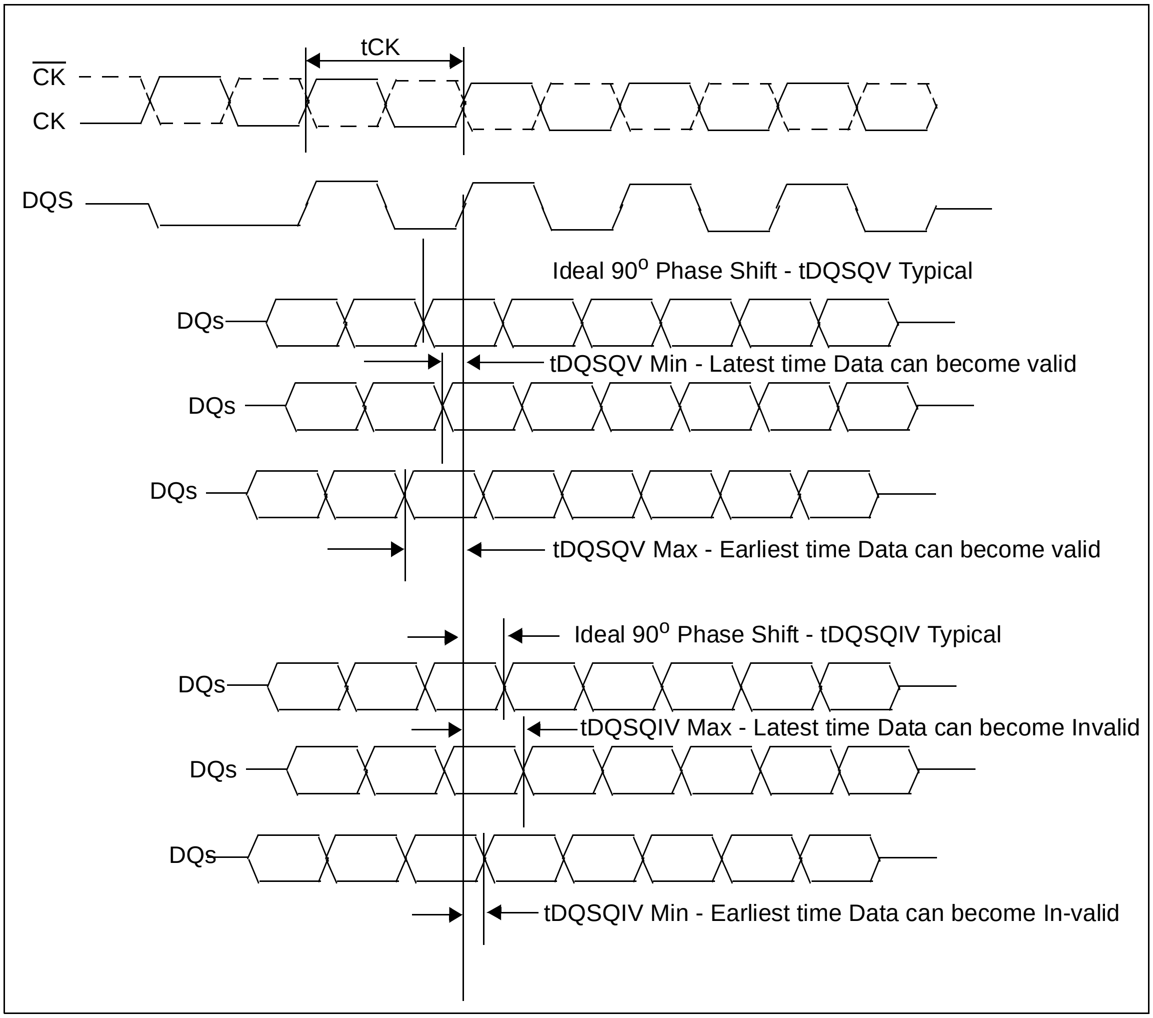


Figure 8. tDQSQV/tDQSQIV Timing Parameters

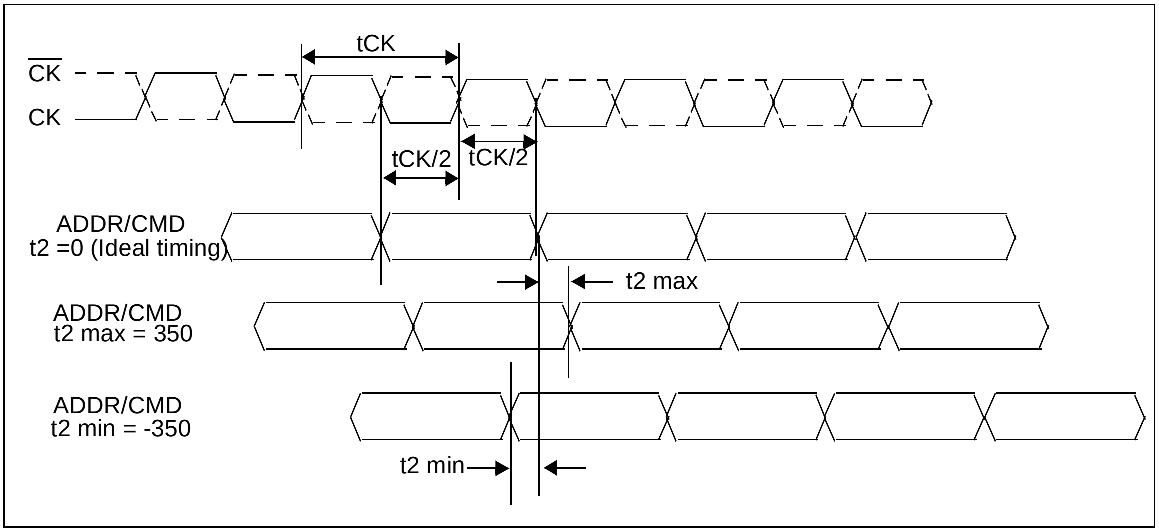


Figure 9. MEMADD/CMD to MEMCLK Timing Parameter (Registered DIMMs)

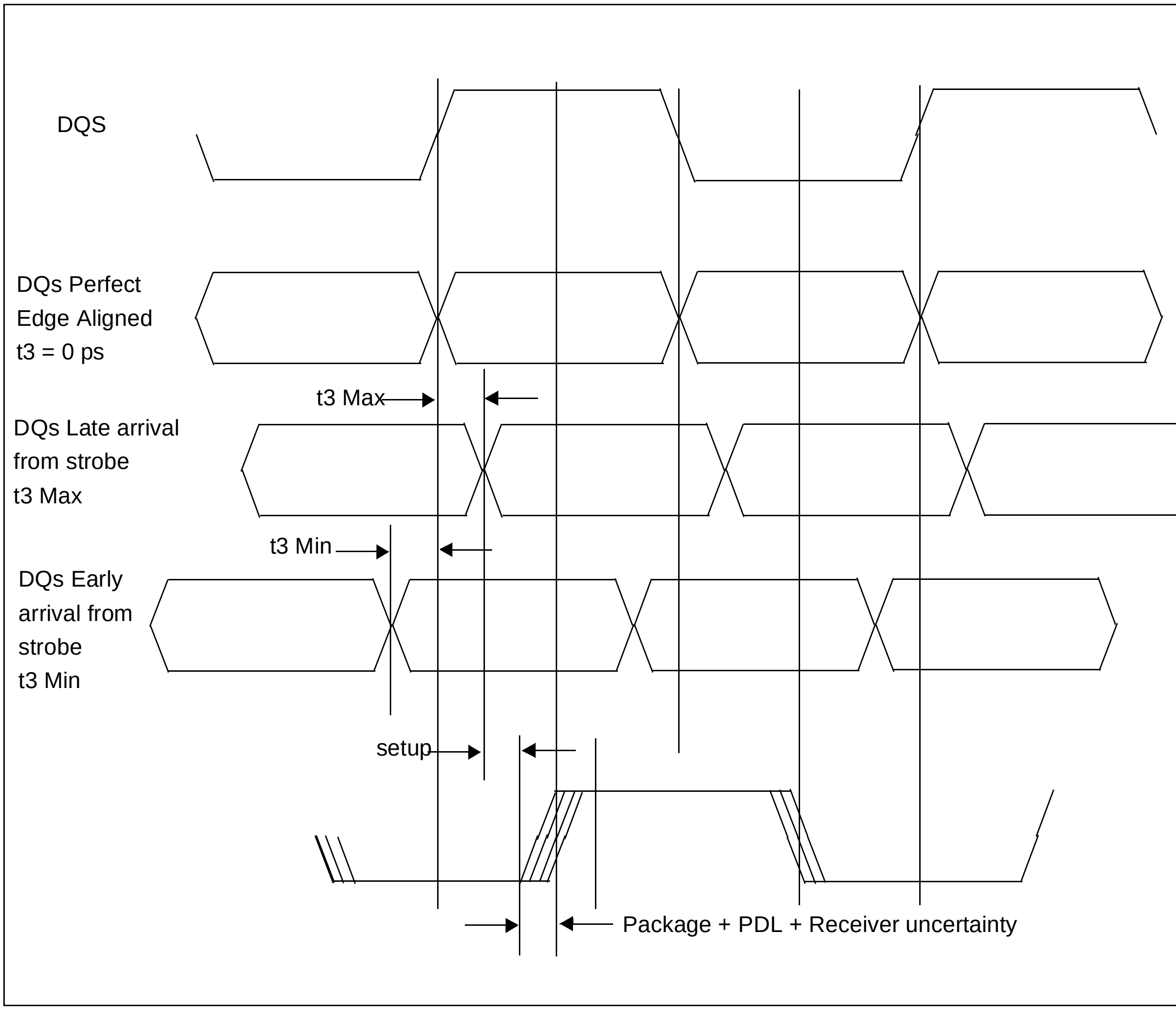


Figure 10. MEMDQS Edge Arrival Relative to DQs

7.4 Clock Pins

7.4.1 Operating Conditions

Table 24. DC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameters	Unit	Min	Typ	Max	Notes
V_{ID}	Differential Input Voltage	mV	300		2400	
$DeltaV_{ID}$	Change in V_{ID} Magnitude	mV	–50		50	
V_{ICM}	Input Common Mode Voltage	mV	VTT–100	VTT	VTT+100	
$DeltaV_{ICM}$	Change in V_{ICM} Magnitude	mV	–50		50	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
$DeltaV_{OD}$	Change in V_{OD} Magnitude	mV	–50		50	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
$DeltaV_{OCM}$	Change in V_{OCM} Magnitude	mV	–50		50	4

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *$DeltaV_{OD}$ is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *$DeltaV_{OCM}$ is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*

Table 25. AC Operating Conditions for CLKIN_H/L and FBCLKOUT_H/L Pins

Symbol	Parameter	Unit	Min	Typ	Max	Notes
F (PLL mode, VDDA=2.5 V)	Input Frequency Range (SSC)	MHz	198.8		200	6
T_{JC}	Jitter, Cycle-to-Cycle	pS	0		200	7
DC	Input Duty Cycle (CLKIN_H/L)	%	30		70	
V_{BIAS}	Input BIAS Voltage Node	mV	VTT	VTT	VTT	
V_{ID}	Differential Input Voltage	mV	400		2300	
DeltaV_{ID}	Change in V_{ID} Magnitude	mV	–150		150	
V_{ICM}	Input Common Mode Voltage	mV	V_{BIAS}–200		V_{BIAS}+200	
DeltaV_{ICM}	Change in V_{ICM} Magnitude	mV	–200		200	
V_{OD}	Differential Output Voltage	V	1.2	1.3	1.4	1
DeltaV_{OD}	Change in V_{OD} Magnitude	mV	–100		100	2
V_{OCM}	Output Common Mode Voltage	V	1.1	1.25	1.4	3
DeltaV_{OCM}	Change in V_{OCM} Magnitude	mV	–100		100	4
I_F	Input Falling Edge Rate	V/ns	1.2		10	5
I_R	Input Rising Edge Rate	V/ns	1.2		10	5
C_{IN}	Input Capacitance	pF	0		5	

Notes:

1. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
2. *Delta V_{OD} is the change in magnitude between the differential output voltage while driving logic 0 and while driving logic 1.*
3. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage relative to ground under DC or AC conditions.*
4. *Delta V_{OCM} is the change in magnitude between the output common mode voltage while driving logic 0 and while driving logic 1 under DC or AC conditions.*
5. *Measured differentially through the range of VICM – 400 mV to VICM + 400 mV.*
6. *Spread spectrum clocking is limited to –0.5% downspread under normal operation.*
7. *Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.*

7.5 Power-Up Signal Sequencing

Figure 12 on page 67 illustrates the signal sequencing requirements during a cold reset (power-up conditions). The HyperTransport™ link reset sequencing is defined in the *HyperTransport™ I/O Link Specification*.

The following list describes the power-up signal sequencing illustrated in Figure 12. Note that the numbered items correspond to the numbers in Figure 12.

1. RESET_L must be asserted a minimum of 1ms prior to the assertion of PWROK, as defined in the *HyperTransport™ I/O Link Specification*. The TMS pin must be asserted a minimum of 10ns before PWROK assertion and must be held in the High state a minimum of 10ns after the assertion of PWROK.
2. CLKIN_H/L must be within specification at the time the VDD power supply begins to ramp.
3. PWROK remains deasserted at least 1ms after CLKIN_H/L is stable and voltages to the processor are within specification. The processor determines if there are devices attached to its HyperTransport links 10µs after the assertion of PWROK.
4. After PWROK assertion, the VID[4:0] signals change from the default code (01110b = 1.2 V) to the value programmed during device manufacturing. The PLL begins locking to the frequency programmed during device manufacturing 160µs after PWROK is asserted.
5. LDTSTOP_L must be deasserted a minimum of 1µs before the deassertion of RESET_L, as defined by the *HyperTransport™ I/O Link Specification*.
6. The RESET_L signal remains asserted a minimum of 1mS after PWROK assertion, as defined in the *HyperTransport™ I/O Link Specification*. The clocks from the transmitters of all HyperTransport technology devices must be stable before RESET_L is deasserted.
7. The MEMCLK_LO_H/L[3:0] and MEMCLK_UP_H/L[3:0] signals are stable after BIOS sets the Memory Clock Ratio Valid (MCR) bit in the processor's DRAM Config Upper register. The MEMCLK* period is defined by the MEMCLK[2:0] field in the DRAM Config Upper register.
8. MEMRESET_L is deasserted after BIOS sets the Dram_Init bit in the DRAM Config Lower register. This allows time for the PLL on registered DIMMs to stabilize before the deassertion of the DIMM's reset signal. The delay between these events depends on the silicon revision and the DRAM operating speed as described in Figure 11 and Table 26 on page 66.
9. The MEMCKE_LO/UP signals are asserted following the deassertion of MEMRESET_L. The delay between these events depends on the silicon revision and the DRAM operating speed as described in Figure 11 and Table 26 on page 66. Note that the MEMCKE_LO/UP delay from MEMRESET_L is different when exiting self-refresh as listed in Table 27 on page 66.

Figure 11. MEMRESET_L and MEMCKE_LO/UP Sequencing

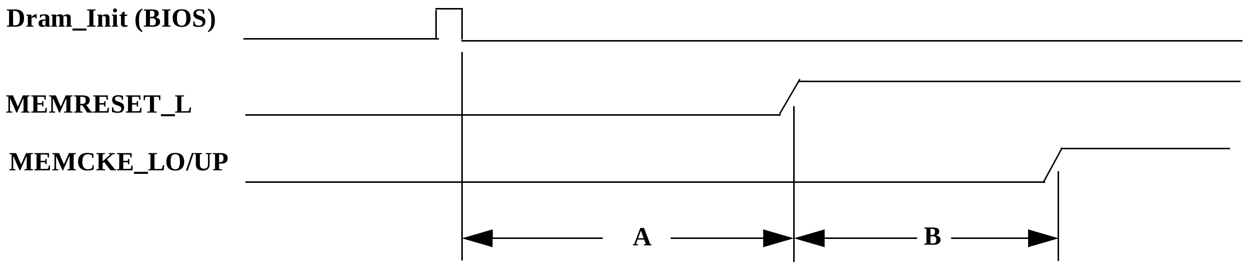


Table 26. MEMRESET_L and MEMCKE_LO/UP Initialization Timing

Silicon Revision	DRAM Speed	Timing Parameter A	Timing Parameter B
Rev B	DDR200	655µS	120nS
	DDR266	492.8µS	90.2nS
	DDR333	394.8µS	72.3nS
Rev C	DDR200	163.8µS	491.5µS
	DDR266	123.2µS	369.6µS
	DDR333	98.7µS	296.1µS
	DDR400	81.9µS	245.8µS

Table 27. MEMCKE_LO/UP Delay from MEMRESET_L During Exit from Self-Refresh

Silicon Revision	DRAM Speed	Registered DIMMs
Rev B	DDR200	120nS
	DDR266	90.2nS
	DDR333	72.2nS
Rev C	DDR200	10.24µS
	DDR266	7.6µS
	DDR333	6.1µS
	DDR400	5.1µS

Note: *Refer to the* AMD Opteron™ Processor Power and Thermal Data Sheet, *order# 30417 for silicon revision determination.*

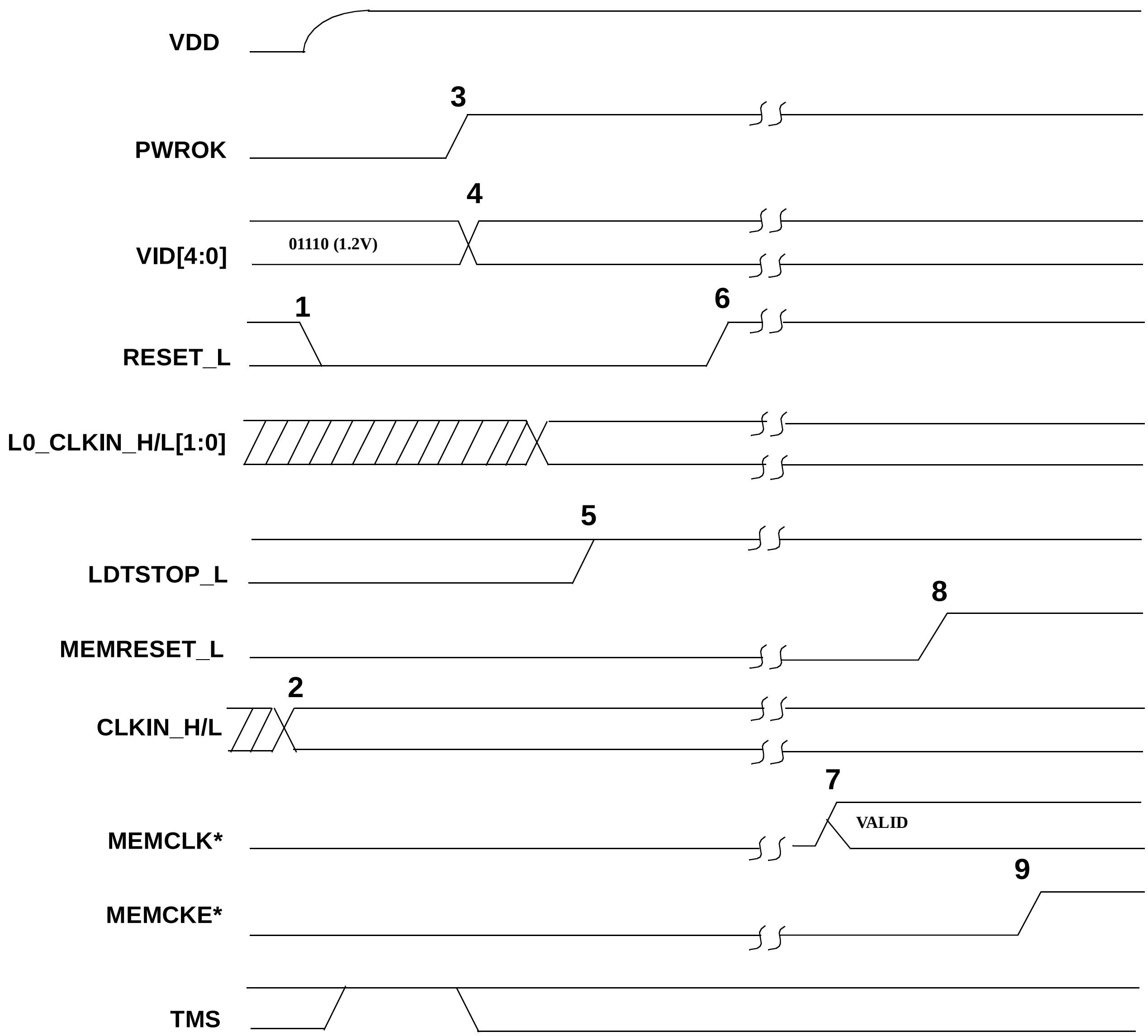


Figure 12. Power-Up Signal Sequencing

7.6 Reference Information

Table 28. Internal Termination for Miscellaneous Pins Interface

Pin	Type[2]	Internal Termination	Value	Tolerance
CLKIN_H/L	I-IOD	None[1]		
FBCLKOUT_H/L	O-IOD	80-ohm differential termination		±50%
RESET_L	I-IOS	None		
PWROK	I-IOS	None		
VID[4:0]	O-IOS	None		
LDTSTOP_L	I-IOS	None		
THERMDA	A	None		
THERMDC	A	None		
THERMTRIP_L	O-IO-OD	None		
COREFB_H/L	A	None		
TCK	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TMS	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TRST_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDI	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
TDO	O-IOS	Pullup to VDDIO	533 ohms	±50%
DBREQ_L	I-IOS	Pullup to VDDIO[3]	533 ohms	±50%
DBRDY	O-IOS	Pullup to VDDIO	533 ohms	±50%

Notes:

1. *CLKIN_H/L inputs have DC voltage BIAS generating circuits on the inputs. These consist of both a ~250-ohm pullup resistor to VTT on each input and a ~250-ohm series input resistor.*
2. *Refer to Table 5 on page 39 for definitions in pin Type column.*
3. *Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used they must not be driven with open-drain outputs or additional termination is required.*

Table 29. External Required Circuits (Pins Not Normally Used in System)

Pin	External Circuit (Non-Operating)[1]
NC_G14	Tied to VDDIO_SUS through resistor
NC_H14	Tied to VSS through resistor
NC_AE14	Tied to VDDIO_RUN through resistor
NC_AF13	Tied to VDDIO_RUN through resistor
NC_AE10	Tied to VSS through resistor
NC_AE11	Tied to VSS through resistor
NC_AF11	Tied to VSS through resistor
NC_AE13	Tied to VSS through resistor
NC_AE12	Tied to VSS through resistor
NC_T3	Tied to VSS through resistor
NC_T4	Tied to VLDT through resistor

Notes:
1. *See the* AMD Athlon™ 64 FX and AMD Opteron™ Processor Motherboard Design Guide*, order# 25180, for proper resistor values.*
2. *Input pins of the same type may be pulled high or low through a shared resistor provided that VIL Max and VIH Min specifications are not exceeded for those pin types.*

7.7 Thermal Diode Specifications

An on-die thermal diode is provided as a tool for thermal management. An external sensor is necessary to measure the temperature of the thermal diode.

Thermal solutions should be not designed and validated using the thermal diode. Thermal solutions should be designed and validated against the case temperature specification per the methodology specified in *AMD Athlon™ 64 and AMD Opteron™ Processor Thermal Guide*, order# 26633.

Table 30. Thermal Diode Specification Revision and Frequency Guide

Rev/Freq	< 2.2GHz	>= 2.2GHz
B3	Table 31	N/A
C0	Table 31	Table 32
CG and later	Table 32	Table 32

Note: *Refer to the* AMD Opteron™ Processor Power and Thermal Data Sheet, *order# 30417 for silicon revision determination.*

Table 31. Thermal Diode Specifications for AMD Opteron™ Processor (Revision and Frequency Dependent, see Table 30)

Symbol	**Parameter**	**Units**	**Min**	**Typ**	**Max**	**Notes**
I	Sourcing Currents	µA	5		500	1
n_f	Ideality Factor		1.008		1.096	2
T_{Offset}	Temperature Offset	°C	0		32	3, 4, 5
θ_{j-c}	Thermal resistance (junction to case)	°C/W			0.32	6

Notes:

1. *The sourcing current should always be used in forward bias.*
2. *Characterized at 95ºC with a forward bias current pair of 10 and 100 µA. The ideality factor limits correspond to the diode offset limits.*
3. *Temperature offset is unique for each processor. The diode offset value is found in the Thermtrip Status Register discussed in the* BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, *order# 26094. This diode offset supports temperature sensors using two or more sourcing currents only. Single-sourcing current implementations are not supported by AMD.*
4. *The temperature offset is set based on a sourcing current pair of 10 and 100 µA and an ideality factor of 1.008. The diode offset should be subtracted from the temperature sensor reading. If the temperature sensor has an ideality factor different from 1.008, an additional offset is needed. Contact your temperature sensor vendor about whether an additional offset is needed.*
5. *After correcting for the diode offset, the thermal diode has an accuracy of ±10°C. This accuracy is additive to the temperature sensor accuracy.*
6. *The temperature specification for the processor is based on the case temperature. The thermal resistance from the junction to the case is provided as a reference for implementing fan-speed control using the thermal diode.*

Table 32. Thermal Diode Specifications for AMD Opteron™ Processor (Revision and Frequency Dependent, see Table 30)

Symbol	Parameter	Units	Min	Typ	Max	Notes
I	Sourcing Currents	µA	5		500	1
T_{Offset}	Temperature Offset	°C	0		52	2, 3, 4, 5

Notes:

1. *The sourcing current should always be used in forward bias.*
2. *The temperature offset is used to normalize the thermal diode measurement to reflect case temperature at the worst case conditions for a part.*
3. *This diode offset supports temperature sensors using two or more sourcing currents only. Single sourcing current implementations are not supported by AMD.*
4. *The temperature offset is unique for each processor and is programmed at the factory. The diode offset value is found in the Thermtrip Status Register described in the* BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors, *order# 26094.*
5. T_{Offset} *should be subtracted from the temperature sensor reading. If the temperature sensor has an ideality factor different from 1.008, a small correction to this offset is required. Contact your temperature sensor vendor to determine if additional correction is required.*

7.8 Power Supplies

7.8.1 Operating Conditions

Table 33. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VID_VDD	VID Requested VDD Supply Level	V	See Note 11			6
VDD_dc	VDD Supply Voltage	V	VID_VDD –50 mV	VID_VDD	VID_VDD +50 mV	
VDD_ac	VDD Supply Voltage	V	VID_VDD –100 mV		VID_VDD +100 mV	13
VDD_PON	VDD Supply Voltage before PWROK assertion during power-on.	V	1.15	1.20	VDD_max	8
VDDIO_dc	VDDIO Supply Voltage for DDR333 and below	V	2.40	2.50	2.60	10
VDDIO_dc	VDDIO Supply Voltage for DDR400	V	2.50	2.60	2.65	10, 12
VDDIO_ac	VDDIO supply voltage	V	VDDIO_dc -150 mV		VDDIO_dc +150 mV	9
VLDT	VLDT Supply Voltage	V	1.14	1.20	1.26	
VTT_dc	VTT Supply Voltage	V	VDDIO_dc Min/2 - 50 mV	VDDIO_dc Typ/2	VDDIO_dc Max/2 + 50 mV	
VTT_ac	VTT Supply Voltage	V	VTT_dc - 150 mV		VTT_dc + 150 mV	9
VDDA	VDDA Supply Voltage	V	2.40	2.50	2.60	
IDD	VDD Power Supply Current	A	See Note 11			
IDDIO1	VDDIO Power Supply Current	A		2.8	2.9	4
IDDIO2	VDDIO Power Supply Current in S3 State	mA			850	
ITT1	VTT Power Supply Current	mA			200	2, 5
ITT2	VTT Power Supply Current in S3 State	mA			200	
ILDT	VLDT Power Supply Current	A			1.5	1
IDDA	VDDA Power Supply Current	mA			33	
IDDslew1	VDD Power Supply Current Change During Normal Operation	A/µs			$.0583*f^{MHz}$	3, 7
IDDslew2	VDD Power Supply Current Change Upon Reset Exit	A/µs			270	3
IDDslew3	VDD Power Supply Current Change Upon Stop Grant Entry	A/µs	–270			3
IDDslew4	VDD Power Supply Current Change Upon Stop Grant Exit	A/µs			270	3

Table 33. Combined AC and DC Operating Conditions for Power Supplies

Symbol	Parameter	Unit	Min	Typ	Max	Notes
IDDslew5	VDD Power Supply Current Change Upon Non-reset Power Failure	A/µs	–4.25			3

Notes:

1. *ILDT is specified for three 16x16-bit HyperTransport™ links operating at 1.6 GT/s.*
2. *VTT must both sink and source current.*
3. *Current slew rates are controlled by ramping up or down the core frequency in steps during these sequences to control in-rush currents.*
4. *VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).*
5. *VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).*
6. *The processor drives a VID code corresponding to this voltage.*
7. *For example, the IDDslew1 calculation for a 1.2-GHz part is (.0583 x 1200) = 69.96 A/µs.*
8. *The processor's VID[4:0] outputs select VID_PON nom before PWROK is asserted. Transients up to VDD_max are allowed.*
9. *VDDIO_ac and VTT_ac parameters are measured +/- 1ns of all data bus bits switching.*
10. *Systems designed to DDR400 power supply parameters will also operate correctly with DDR333 and below.*
11. *Refer to the* AMD Opteron™ Processor Power and Thermal Data Sheet, *order# 30417, for these specifications.*
12. *DDR400 (200MHz) supported by Rev C0 and later. Refer to the* AMD Opteron™ Processor Power and Thermal Data Sheet, *order# 30417 for silicon revision determination.*
13. *Transient duration below VDD_dc min is limited to < 5µs. Transient duration above VDD_dc max is limited to < 2% duty cycle. Test by probing differentially at COREFB_H and COREFB_L with 20MHz scope bandwidth limit. Test conditions are while running AMD's MAXPOWER64 utility using AMD thermal approved production grade heat sinks in normal room ambient conditions.*

7.8.2 Thermal Power

Refer to *AMD Opteron™ Processor Power and Thermal Data Sheet*, order# 30417, for thermal power specifications.

7.8.3 Power Supply Relationships

7.8.3.1 Sequencing Relationships

Power supply relationships during power-up, power-down, and entry and exit of any power management state must be controlled in order to avoid damage to the device and help ensure proper operation of the device. Figure 13 shows an example of how these relationships can be maintained by system power generation and distribution schemes. PWROK must be deasserted as VDD decays during power down. VTT and VDDIO are considered SUSPEND planes and are powered in the S0 (working) state and the S1 and S3 sleep states. VDDA, VDD, and VLDT are considered RUN planes and are powered in the S0 and S1 states only. All power supplies should be turned off during the S4 (SUSPEND to DISK) and S5 (SOFT-OFF) states. VDDIO (RUN) is a power rail used for pull-ups on some processor signals that connect to devices that are powered off during S3, such as THERMTRIP_L.

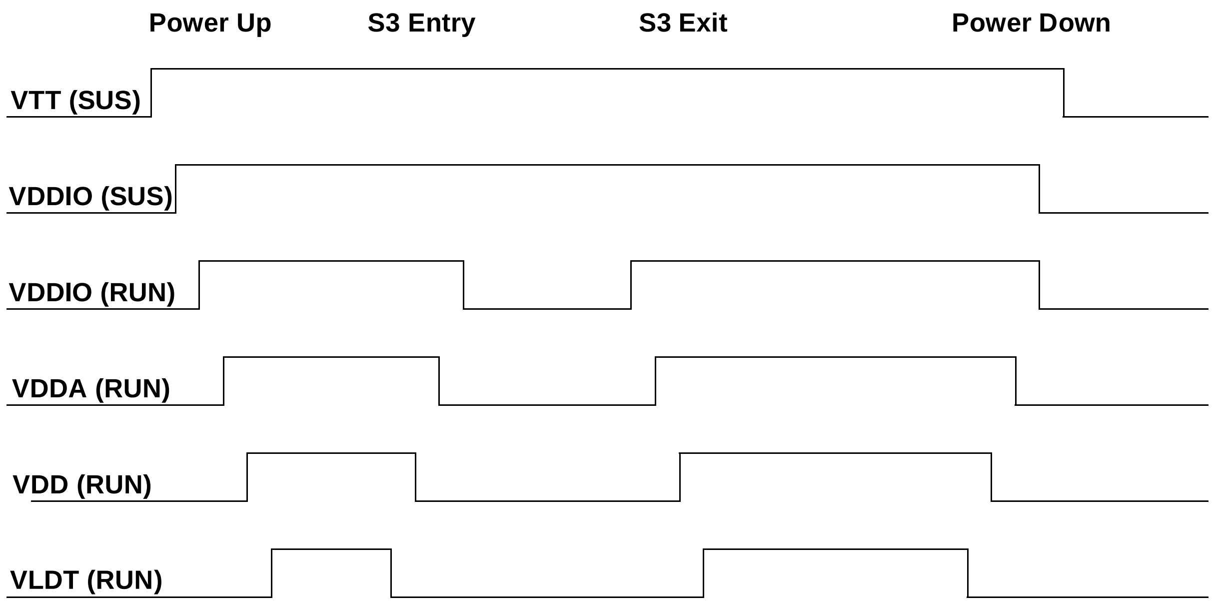


Figure 13. Sequencing Relationships for Power Supplies

Table 34. Sequencing Relationships for Power Supplies

Power Supply Relationship	Unit	Max	Notes
VTT to VDDIO	V	VTT_dc Max	1, 2
VDDIO to VTT	V	VDDIO_dc Max - VTT_dc Typ	1, 3
VDDIO to VDD	V	VDDIO_dc Max	1, 4
VDDA to VDD	V	VDDA Max	1, 5
VDD to VLDT	V	VDD Max	1, 6

1. *Sequencing relationships are measured from supply to supply and cover the DC voltage relationships between supplies that must be maintained under all operating conditions including power up, power down, power failure, and power state transitions in order to avoid device or system damage. These relationships can be maintained by propagation of PWRGD signals from one supply rail to the regulator enable of the next supply. The minimum requirements for a proper system implementation are that:*
   — VDDIO ramps such that VDDIO/2 <= VTT.
   — VDD ramps such that VDDIO and VDDA are within spec before VDD is enabled.
   — VLDT ramps such that VDD is within spec before VLDT is enabled.
2. *The VTT to VDDIO relationship allows for VTT to power-up before VDDIO.*
3. *The VDDIO to VTT relationship is critical to avoid overstress of the 2.5-V I/O structures that will occur when VDDIO exceeds VTT by 1.35 V during normal operation. VTT must track VDDIO/2 to maintain this specification. During power up and power down VDDIO may exceed VTT by up to 1.5V for no more than 100ms.*
4. *The VDDIO to VDD relationship allows for VDDIO to power-up before VDD.*

5. *The VDDA to VDD relationship allows for VDDA to power-up before VDD. VDDA must power-up before VDD to ensure that internal clock sources are valid before being used and that clock source multiplexors are properly controlled.*
6. *The VDD to VLDT relationship allows for VDD to power-up before VLDT and specifically allows for VDD=VDD_max with VLDT=0 V. VDD must power-up before VLDT to help ensure that PWROK is properly passed from the pins into the VDD power domain such that the deasserted state can be seen in the VLDT power domain.*

7.8.3.2 Sequencing Relationships: Signals to Power Supplies (Stress Conditions)

Once the powerup sequence has been completed and PWROK can be asserted, the sequencing of input signals to the CPU and output signals from the CPU can begin. The requirements from signals to power supplies are summarized by type as follows.

- VDDIO inputs and outputs are allowed to exceed VDDIO by 0.3V and are allowed to be 0.3V below VSS.
- VDDIO inputs are allowed to exceed VTT by VTT_dc Max + 0.3V and are allowed to be 0.3V below VSS.
- VLDT inputs and outputs are allowed to exceed VLDT by 0.3V and are allowed to be 0.3V below VSS.

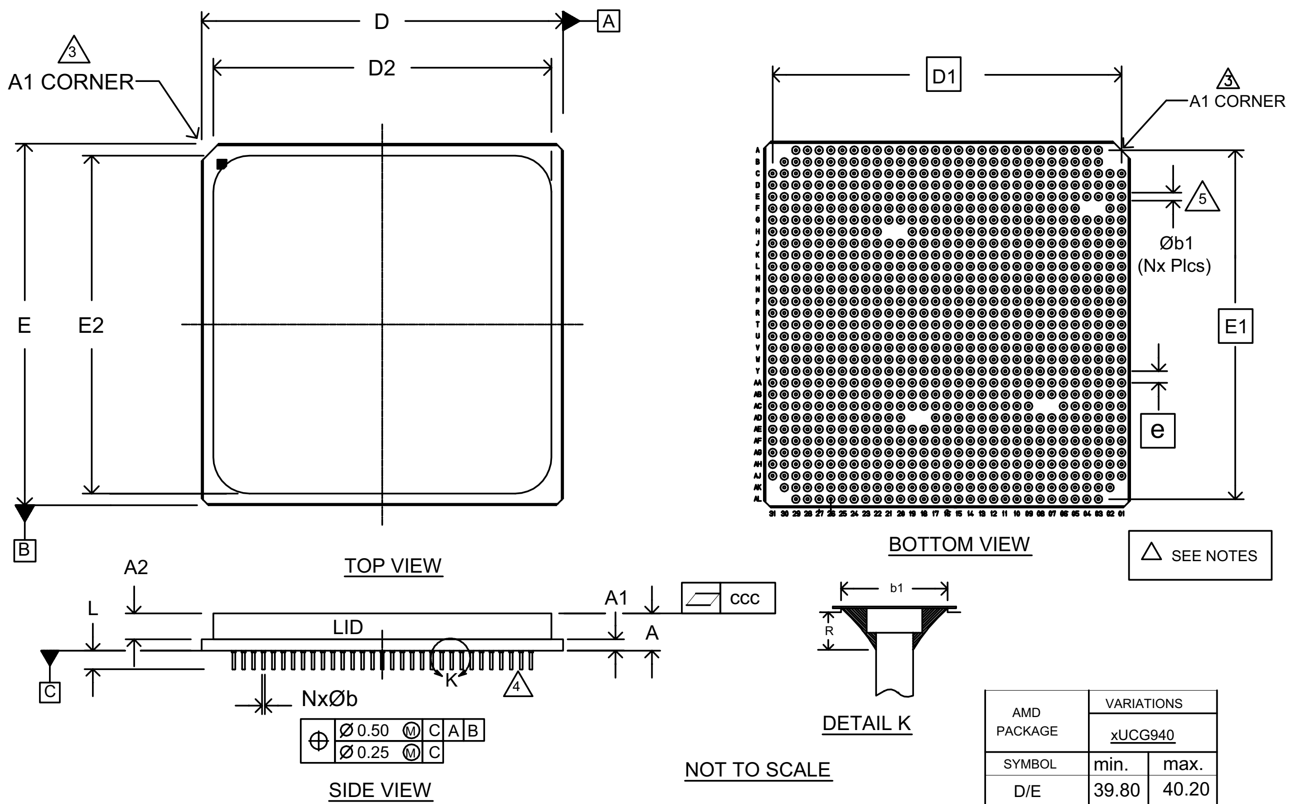
7.8.3.3 Power Failures

The power sequencing relationships defined in sections 7.8.3.1 and 7.8.3.2 must be guaranteed by the motherboard power supply subsystem in the event of a power failure.

7.8.3.4 Unused Links

Because the AMD Opteron processor has three independent HyperTransport links, some implementations will not connect one or more of these links. In this case, the VLDT of the link that is not connected to another device, should be connected to the VLDT of an operating link. Note that even if the link is not used, the VLDT for the link must be connected so that the internal link detection circuitry can successfully determine the connection status of the link.

8 Package Specifications



AMD PACKAGE	VARIATIONS xUCG940	
SYMBOL	min.	max.
D/E	39.80	40.20
D1/E1	38.10 BSC	
D2/E2	37.4	37.6
A	4.88 REF	
A1	1.556	1.796
A2	3.05	3.35
e	1.27 BSC	
b	0.275	0.35
b1	0.81	1.06
L	2.03	2.29
M	31	
N	940	
R	0.30 MAX	
ccc	0.125	
WT (gms)	45.17 REF	

GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner has a chamfer and a square on top of the package that identifies the pin A1 corner and can be used for handling and orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" defines the pin matrix size and "N" is number of pins.

Figure 14. Ceramic Micro Pin Grid Array Package: Top, Side, and Bottom Views