

□ MN103E01, MN103E04 Series

Type	MN103E010HRA	MN103E040HYB
Instruction Cashe (byte)	16K (4-way, set-associative)	
Data Cashe (byte)	16K (4-way, set-associative)	
SRAM Used by Both Instructions and Data(byte)	16K	
Package (Lead-free)	BGA292-P-2727	FLGA424-C-1717
Minimum Instruction Execution Time	7.5 ns (at 1.8 V tolerance = ±5%, 133 MHz)	

■ Interrupts

XIRQ × 8, NMI, Timer × 14, DMAC × 4, WDT, A/D, SIO × 6, I²C × 2, IrDA, Softmodem, Realtime clock, Asynchronous bus error

■ Timer Counter

8-bit timer × 4 (all down counters)

Cascade connection possible (usable as a 16/24/32-bit timer), Timer output possible (Duty = 1 : 1), Internal clock source or external clock source selectable, Selectable as a serial interface clock

16-bit timer × 7 (down counters)

Cascade connection possible (usable as a 32-bit timer), Timer output possible (Duty = 1 : 1), Internal clock source or external clock source selectable, Partially selectable as a serial interface clock

16-bit timer × 1 (up counter)

Internal clock source or external clock source selectable, Input capture function (rising edge, falling edges, or both selectable),

PWM generating function (compare/capture register × 2 contained)

Watchdog timer × 1

■ Serial interface

UART/synchronous (co-used) × 2-ch.

UART (with CTS control) × 1-ch.

■ DMA controller

Number of channels : 4

Transfer unit : 1/2/4/16 byte

Maximum number of bytes transferred : 1Mbyte

Start factor : External request, interrupt, software

Transfer mode : 2-bus cycle transfer

Transfer mode : Batch transfer, intermittent transfer

Addressing mode :

Source/destination each fixed, increment/decrement specification possible

Increment/decrement automatically executed according to the transfer unit

■ Expanded Calculation Functions

Multiply-and-accumulate; Multiply saturation; Floating point(Single precision)

■ I/O Pins

I/O 34 : Common use : 33

■ A/D converter

10-bit charge re-distribution mode (error : ±4LSB)

Number of channels : 8-channel

■ FPU (floating point unit)

- Data types complying with the IEEE754 standard supported

- Round to the nearest mode complying with the IEEE754 standard supported

- 32 single-precision floating point operation registers (FS0-FS31)

These can also be referenced as 16 double-precision floating point operation registers (FD0-FD30)

- Floating point operation exceptions (5 types) and floating point unload instruction exceptions complying with the IEEE754 standard supported

■ Memory Management Function

32-entry full-associative TLB loaded (instructions/data separated from each other)

Address conversion by paging (page size : 1 K-byte, 4 K-byte, 128 K-byte, 4 M-byte variable)

■ On-chip Bus Controller

Concurrent access from three types of master devices to four types of slave devices possible

■ System Bus Interface

External memory space allocation to 8 banks possible

The external interface can use the built-in memory, RAM, ROM, SDRAM interfaces

■ Memory Bus Interface

SDRAM directly connected interface contained

■ Soft Modem Interface

Interface with an external AFE (analog front end), Output data parallel-serial conversion, input data serial-parallel conversion

Send/receive FIFO contained (16-bit width, 16 steps), NCU control via the parallel IO port

■ Real-time Clock

Clock/calendar function, Interrupt : periodic, alarm, update ended

BCD/binary accommodated,

Leap year automatic correcting function, 24-hour/12-hour selectable, Daylight saving time mode accommodated

■ IrDA Interface

IrDA 1.0 SIR (-115.2 Kb/s, half-duplex)

IrDA 1.1 MIR (0.576, 1.152 Mb/s, half-duplex)

IrDA 1.1 FIR (4.0 Mbp/s, half-duplex)

UART (-1.5 Mbp/s, full-duplex)

48 MHz clock input (baud rate generating function contained)

■ I²C Interface

2 ports

Master-slave interface (multi-master supported)

3.3 V interface (open drain output)

■ Electrical Characteristics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD18A	VDD18 = 1.8 V ; VDD33, PVDD, AVDD, RVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1 : 0] = 0.0 ; Output open			460	mA
Supply current at stopping	IDD18D	VDD18 = 1.89 V VDD33, PVDD, AVDD, RVDD = 3.465 V fOSC = Stop ; FRQS[1 : 0] = 0.0 ; Output open ; Tj = 70°C			50	mA

(Ta = -20°C to +70°C)

■ Electrical Characteristics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bit
A/D conversion relative error		VREFH = 3.3 V			±4	LSB
A/D conversion differential non-linear error		Conversion reference clock = 4.166 MHz			±4	LSB
A/D conversion time			2.6			μs

(Ta = -20°C to +70°C , AVDD = 3.3 V±0.165V , AVSS = 0.0 V)

■ Development tools

ROM Emulator

PARTNER-ETII (KMC product)

On-board Development Tools

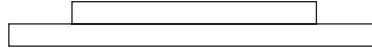
PX-ODB103E-J (On-board debug unit)

PX-ODB-AMT-20 (Trace unit)

PARTNER-J (KMC product)

■ Pin Assignment
BGA292-P-2727

Perspective



TRCD6	TRCD1	TDO	TRST MOD	PIO4[2]	PIO3[2]	SBI0	SBO1	SBT1	SBT2	XRST OUT	XIRQ1	XIRQ4	XIRQ5	PIO0[0]	PIO0[4]	AVDD	AN4	AVSS	VREFH	20						
TRCD3	EXTRG	TCK	PIO4[0]	PIO3[0]	PIO3[3]	SBO0	SBI1	SBI2	XIRQ0	XIRQ2	XNMI	XIRQ7	PIO0[2]	PIO0[6]	AN6	AN2	AN1	PIO1[2]	PIO5[0]	19						
TRCD7	TRCD4	TRCD0	TDI	TMS	PIO4[1]	PIO3[1]	PIO3[4]	SBT0	SBO2	XRESET	XIRQ3	XIRQ6	PIO0[1]	PIO0[5]	AN7	AN3	AN0	PIO1[1]	PIO5[2]	18						
MD0	TRCD2	TRCD5	VSS	VSS	PIO4[3]	VDD18	VDD33	VSS	VDD18	VDD33	VSS	PIO0[3]	VSS	PIO0[7]	AN5	PIO1[0]	PIO1[3]	PIO5[1]	CLK48	17						
MD13	TRC CLK	TRCST	VSS													VSS	PIO1[4]	SD3	SD0	16						
MD3	MD14	MD15	VSS													SD2	SD1	SD6	SD4	15						
sdcki	MD2	MD1	VD33													VDD33	SD5	SD9	SD7	14						
MD5	MD11	MD12	VD18	VSS VSS VSS VSS VSS VSS																		VSS	SD8	SD12	SD10	13
MD8	MD10	MD4	VDD33	VSS VSS VSS VSS VSS VSS																		VDD18	SD11	SD15	SD13	12
MD7	MD6	MD9	VSS	VSS VSS VSS VSS VSS VSS																		VDD33	SD14	SD17	SD16	11
MDK	XMCAS	XMBE0	VDD33	VSS VSS VSS VSS VSS VSS																		VSS	SD23	SD18	SD19	10
XMBE1	XMWE	MA12	VSS	VSS VSS VSS VSS VSS VSS																		VDD18	SD21	SD20	SD22	09
SDCLK	SDCKE	MA11	VDD18	VSS VSS VSS VSS VSS VSS																		VSS	SD25	SD24	SD26	08
XMRAS	XMCE1	MA13	VDD33													VDD33	SD29	SD27	SD28	07						
XMCS0	MA14	MA7	VDD33													XSCS2	XSAS	SD30	SD31	06						
MA9	MA8	MA1	VSS													VSS	XSCS3	XSCS0	XSCS1	05						
MA10	MA0	MA4	VSS	VSS	SA22	VDD18	VDD33	VSS	VDD33	SA0	XSBR	XSRE	VDD18	VDD33	VSS	VSS	XSCS6	XSCS4	XSCS5	04						
MA6	MA5	SA31	SA26	SA23	SA19	SA16	SA13	SA9	SA10	SA1	XSBG	PIO2[4]	PIO2[3]	PIO2[0]	VSS	XSWE3	XSWE0	XSCS7	RCLKI	03						
MA2	MA3	SA28	SA25	SA21	SA18	SA15	SA12	SA8	SA6	SA2	SSZ0	SRXW	PIO2[2]	PIO2[1]	TCP OUT	PWROK	XSWE2	XSWE1	RCLKO	02						
SA30	SA29	SA27	SA24	SA20	SA17	SA14	SA11	SA7	SA5	SA4	SA3	SSZ1	XSDK	SYS CLK	OSCO	OSCI	PVSS	PVDD	RVDD	01						
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y							

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