32 Segment Static LCD Driver

Features

- Drives up to 32 LCD segments in direct drive (versions 01/02) with an additional BP output
- Low power consumption
- Wide operating voltage range 3 to 15V
- Wide operating temperature range −40° to +85°C
- High noise immunity
- Few external components needed
- Serial data input/output
- 3 wire interface: CLOCK, DATA and STROBE
- N-way multiplex capability (versions 03/04)
- On-chip latches separate display and control sections
- Version 02/04 cross free cascadable
- Internal frequency control with on-chip oscillator
- Cascadable with on-chip wave shaping
- CMOS and NMOS compatible inputs
- Packages DIL40, PLCC44 and TAB

Description

The M 6003 is a CMOS integrated circuit that drives all LCD displays with either direct drive or multiplex voltage levels. The device accepts serial input data and requires only additional clock and strobe lines. Up to 32 segments may be driven by one device in direct drive. In the N-way multiplex version, 32N segments may be driven (N being limited by the display type in use). Versions 01 and 02 are for direct drive applications, versions 03 and 04 for multiplexed drive applications. Standard packaging for the M 6003 is 40 pin DIL plastic package, 44 pin PLCC and TAB on 35mm film.

Applications

- Instrumentation readouts
- Automotive dashboards
- Digital clocks, counters, etc.
- Large displays
- Telephones
- Balances and scales
- Portable battery operated products
- TAB for space limited, light weight products

Typical Operating Configuration

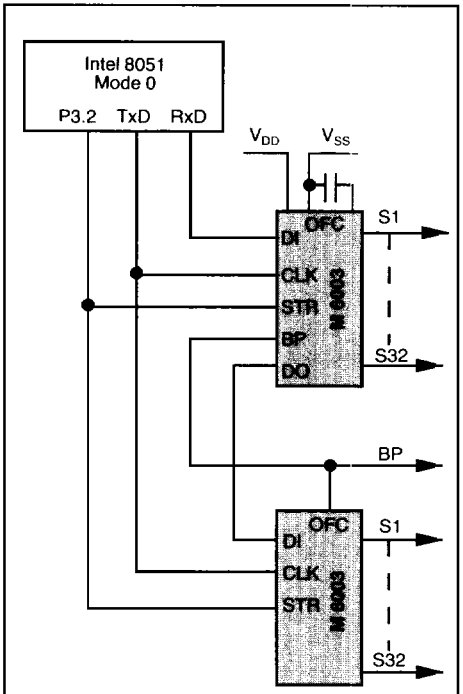


Fig. 1

Versions Available

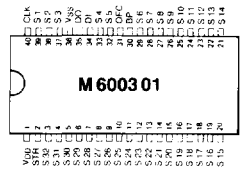
Version	Function	Packages
01	Direct drive	DIP40, PLCC44, TAB
02	Direct drive cascadable on single layer PCB	PLCC44, TAB
03	Multiplexed drive	DIP40, PLCC44, TAB
04	Multiplexed drive cascadable on single layer PCB	PLCC44, TAB

Table 1

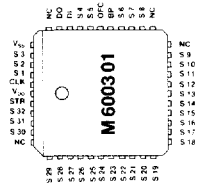
Pin Assignment

Version 01

a) DIP 40



b) PLCC 44



c) Film

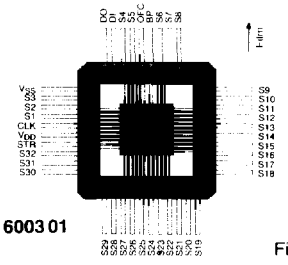
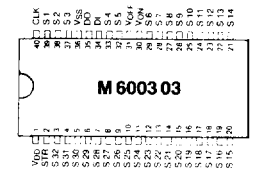


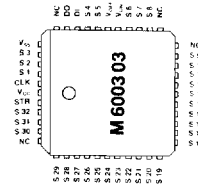
Fig. 2

Version 03

a) DIP 40



b) PLCC 44



c) Film

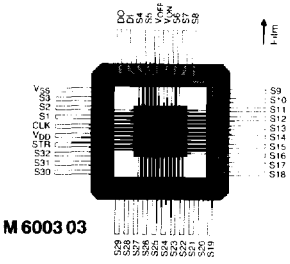
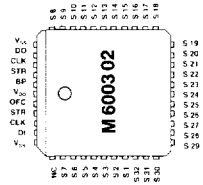


Fig. 3

Version 02

a) PLCC 44



b) Film

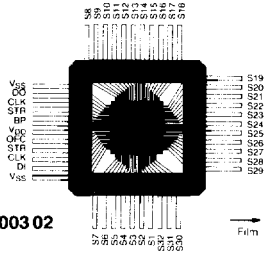
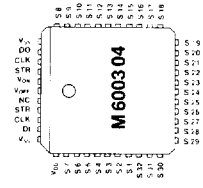


Fig. 4

Version 04

a) PLCC 44



b) Film

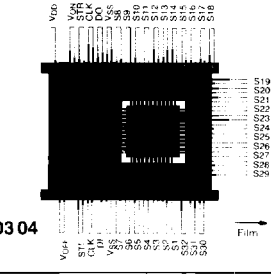


Fig. 5

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{MAX}	−0.3 to +17V
Voltage of any pin to V_{SS}	V_{MAX}	−0.3V
Voltage of any pin to V_{DD}	V_{MAX}	+0.3V
Storage temperature range	T_{STO}	−65 to +150°C

Table 2

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit. For proper operation it is recommended that all terminal voltages are constrained to the range $V_{SS} < V_{TERMINAL} < V_{DD}$, unless specially permitted. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

3

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	T_A	−40		+85	°C
Positive supply voltage	V_{DD}	3		15	V

Table 3

Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V, V_{SS} = 0, unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Supply current	I_{DD}	OFC at V_{DD}		1.5	3	μA
		C = 100pF, see Fig. 8		30	40	μA
		f<100Hz, oscillator driven		4	7	μA
I/O Lines						
Input high voltage	V_{IH}	V_{DD} = 3V	0.7 V_{DD}		V_{DD}	V
		$V_{DD} \geq$ 5V	0.5 V_{DD}		V_{DD}	V
Input low voltage	V_{IL}	$V_{DD} \leq$ 5V	0		0.2 V_{DD}	V
		V_{DD} = 15V	0		0.1 V_{DD}	V
Input voltages for OFC	V_{IH}		0.9 V_{DD}		V_{DD}	V
	V_{IL}		V_{SS}		0.1 V_{DD}	V
Input current	I_L	$V_{SS} < V_{IN} < V_{DD}$			10	μA
Input current for OFC	I_L	$V_{SS} < V_{IN} < V_{DD}$	1	3	10	μA
Input capacitance	C_{IN}			5		pF
Data output impedance	R_{ON}	I_L = 1mA		0.6	1	kΩ
Segment output impedance	R_{ON}	I_L = 10μA		15	40	kΩ
Backplane output impedance	R_{ON}	I_L = 150μA		1	2	kΩ

* Typical values are at 25°C and nominal voltages.

Table 4

Timing Characteristics at V_{DD} = 5V, V_{SS} = 0 and T_A = 25°C, unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock pulse width	t_{CL}, t_{CH}		250		∞	ns
Strobe pulse width	t_{PS}		200		t_{CL}	ns
Data set-up time	t_{DS}		250			ns
Data hold time	t_{DH}		100			ns
DO rise and fall time	t_R, t_F	C_L = 50pF, 10% to 90%			150	ns
DO propagation delay	t_{PD}	C_L = 15pF			500	ns
Strobe delay	t_{SD}		150			ns
Clock rise and fall time	t_{CR}, t_{CF}	10% to 90%			200	ns
Backplane frequency	f_{BP}	C = 33pF	40		90	Hz

Table 5

Timing Waveform

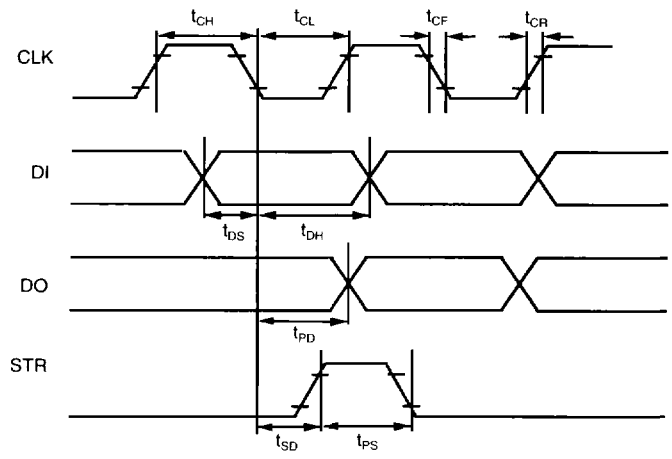


Fig. 6

Block Diagram

Direct drive versions shown:
Links I: direct drive
Links II: N-way mux

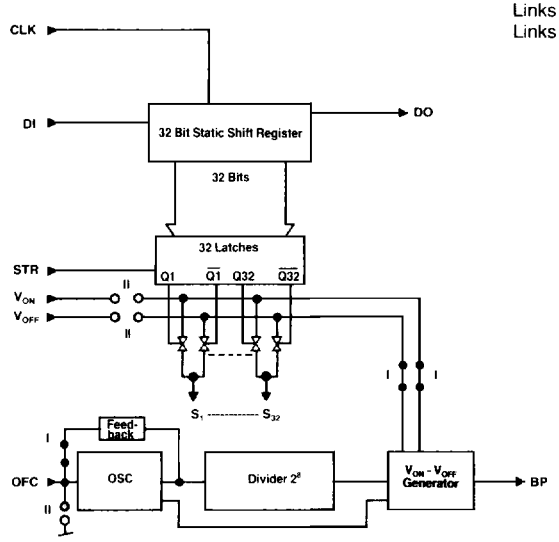


Fig. 7

Pin Description

Name	Function
V_{DD}	Positive supply terminal
V_{SS}	Ground terminal
V_{ON}	On-voltage waveform input (03/04)
V_{OFF}	Off-voltage waveform input (03/04)
OFC	Oscillator frequency control terminal (01/02)
DI	Serial data input
DO	Serial data output
CLK	Clock input
STR	Strobe input
S xx	Segment drive outputs
BP	Backplane drive output (01/02)

Table 6

Functional Description

General

Referring to the block diagram (Fig. 7), the M 6003 may be divided into two parts: the segment drivers and the waveform generator. The segment driver part consists of a 32 bit static shift register paralleled by 32 latches, which drive 64 analog switches. The waveform generator contains an RC oscillator, divider chain and the generator for the backplane and segment drive signals. The waveform generator is disconnected in the versions 03/04 for multiplexed drive, the corresponding waveforms being fed directly to the analog switches by the V_{ON}/V_{OFF} inputs.

V_{DD}, V_{SS}, V_{ON}, V_{OFF}

These pins constitute the supply lines. Only V_{DD} and V_{SS} are used in the direct drive mode (versions 01/02), but for multiplexing (versions 03/04) the extra voltages V_{ON} and V_{OFF} are needed. These two voltages depend upon the LCD and the multiplex scheme used. $V_{DD} - V_{SS}$ being the supply voltage for the logic part, care should be taken that the swing of the input signals does not go outside this range.

OFC Input

This input, present in the direct drive versions (versions 01/02) only, controls the frequency of the waveforms of the segment and backplane drivers. Two different modes are possible: free running or externally driven. In the free running mode, the frequency of the RC oscillator is inversely proportional to the capacitance connected between OFC and either V_{SS} or V_{DD}. With 33pF connected, the internal divider chain provides a basic LCD drive frequency. The temperature variation is approximately 0,6Hz/°C. When the OFC input is driven by a logic signal, an internal sense circuit switches off the oscillator and bypasses the divider chain thus generating a drive frequency in phase with the input signal.

BP Output

The backplane drive output, available only in the direct drive versions (versions 01/02), delivers a square wave signal with amplitude $V_{DD} - V_{SS}$ of a frequency determined by the OFC input (see "OFC Input").

Segment Outputs

The 32 segment-drive outputs S_1 to S_{32} have their display drive waveforms fed from the on-chip oscillator (versions 01/02) or from the V_{ON}/V_{OFF} inputs (versions 03/04). Each of the 32 corresponding data bits output by the latches selects for its segment the ON or the OFF waveform. The latches are loaded from the data input shift register by a positive pulse on the STR input, and the segment number of a data bit is the number of clock pulses used to shift it in from the data input pin DI.

Direct Drive Versions (versions 01/02)

The 32 segment-drive outputs deliver each a square wave of the amplitude $V_{DD} - V_{SS}$ at the frequency of the backplane output (see "BP Output"). This square wave is either in phase with the backplane signal (data 0) or in antiphase (data 1), resulting in a differential voltage across the corresponding LCD segment of either 0 or $[V_{DD} - V_{SS}]$.

Multiplexed versions (versions 03/04)

Depending on the data latched for the corresponding segment, the 32 segment drive outputs are either connected to the V_{ON} input (data 1) or the V_{OFF} input (data 0). The resulting voltage across the LCD segment is the difference between the V_{ON}/V_{OFF} output waveform and the segment's counter-electrode waveform from another driver. Details of different multiplex schemes are available on request.

DI Input

Data present on the DI pin is clocked in at the falling edge of the clock signal (see "CLK Input") and shifted through the 32 stages of the M 6003. A logic high level on the DI input causes a segment to be visible (direct drive) or connected to V_{ON} (multiplex drive). The timing and waveforms are shown in Fig. 6. The segment number corresponds to the number of clock pulses applied to shift in the data bit concerned.

DO Output

The data presented at the DI input will be shifted out at the DO output 32 clock periods later at the falling edge of the clock signal (see "CLK Input"). Exact timing and waveforms are shown in Fig. 6.

CLK Input

This input is used to clock the data present at the DI input through the shift register. Loading, shift and output of the data occur with the falling edge of the clock signal (Fig. 6). In order to avoid race conditions, data and strobe should be changed with the rising edge of the clock signal.

STR Input

The strobe signal is used to latch the data held in the shift register. A logic high level on the STR input causes a parallel loading of the shift register data into the output latches. If the STR input is held high, the latches are transparent. Timing and waveforms are shown in Fig. 6.

Cascading

Due to the on-chip wave shaper, the M 6003 is specially

suited for cascading. Just connect the DO pin of the previous device to the DI pin of the following and tie all CLK, STR and supply lines together. A few precautions should be taken with the OFC and BP pins (versions 01/02 only) in order to achieve best performances. When the waveforms are generated with the internal oscillator, connect the OFC input of the following device to the BP output of the previous one. Only one capacitor is then needed to provide frequency control. The same procedure may be used for driving OFC, or all OFC inputs may be connected to a common driving signal. The backplane of the LCD display should be connected to the free BP output thus minimizing the DC components of the driving signals.

Versions 02 and 04

Due to internal links, these two versions in either PLCC44 or TAB package allows the cascading of several M 6003 on a single layer PCB (Fig. 9 and 10). Version 02 is for direct driven LCD displays, version 04 for multiplexed displays.

Typical Applications

M 6003 01/02 Circuits Driving a 64 Segment Display in Direct Drive

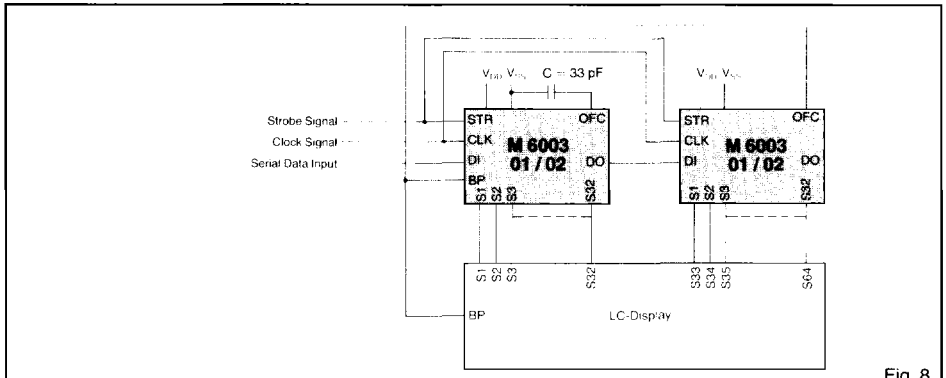


Fig. 8

M 6003 03/04 Circuits Driving an LCD at Low Mux Rate

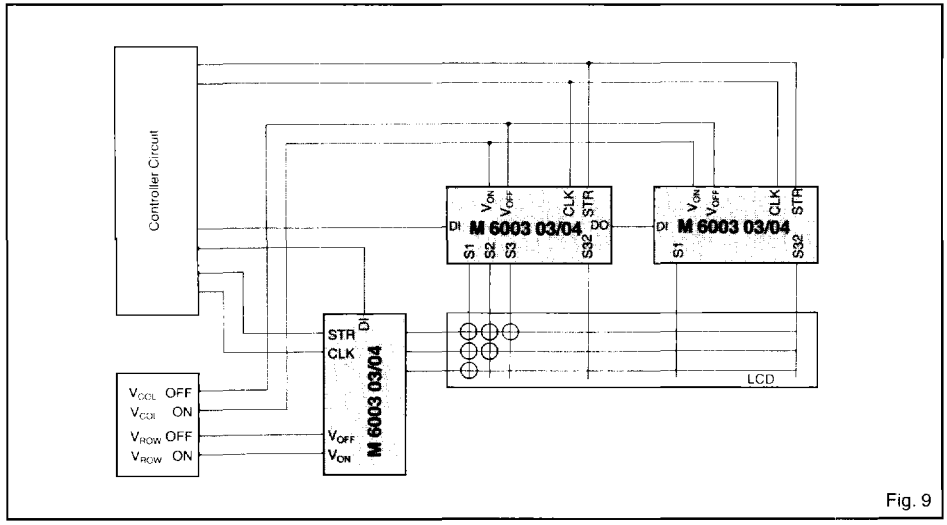


Fig. 9

Cascaded Version 02 for Direct Drive Application

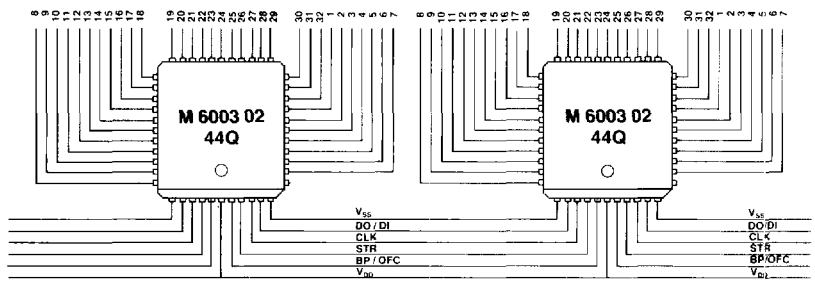


Fig. 10

Cascaded Version 04 on Film

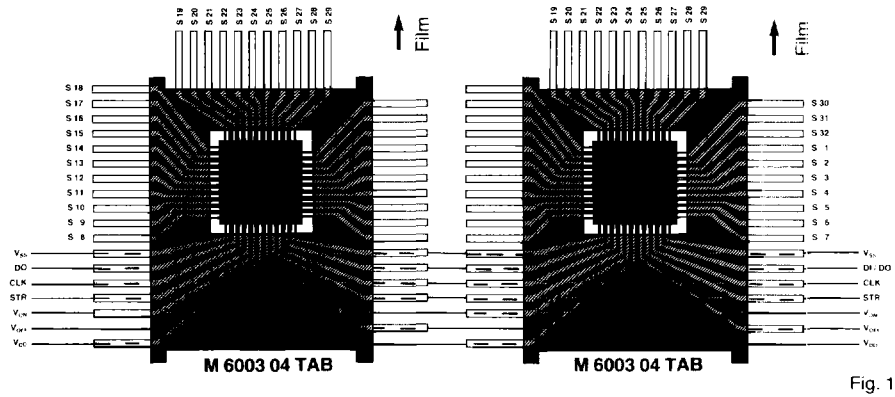
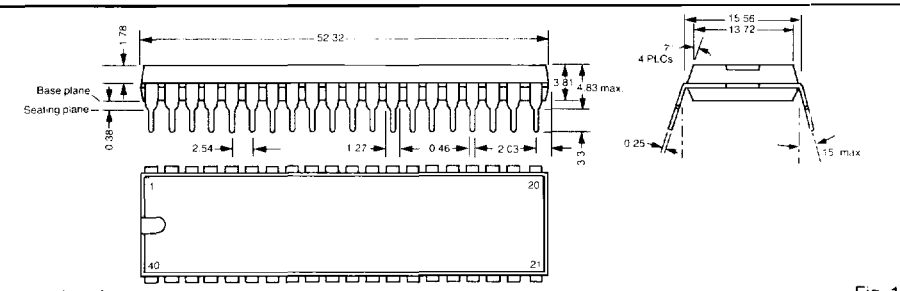


Fig. 11

Package and Ordering Information

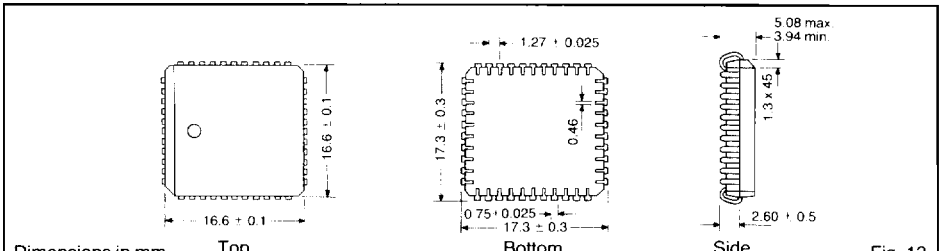
Dimensions of DIP40 Package



Dimensions in mm

Fig. 12

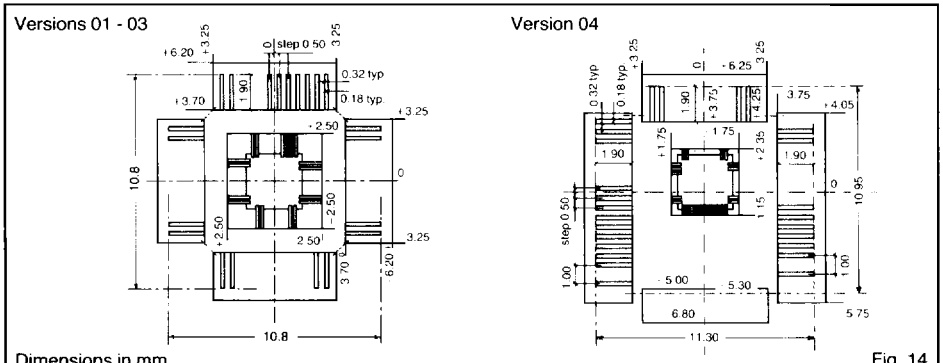
Dimensions of PLCC44 Package



Dimensions in mm

Fig. 13

Dimensions of TAB Packages



Dimensions in mm

Fig. 14

Recommended Solder Area (Top View)

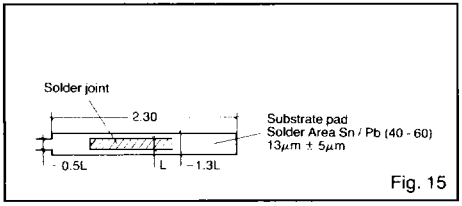


Fig. 15

Soldered Lead (Side View)

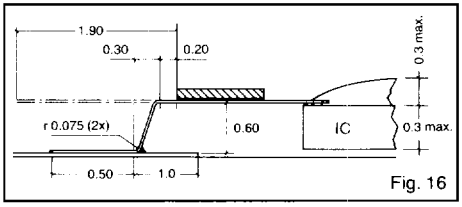


Fig. 16

Ordering Information

The M 6003 is available in the following versions and packages:

Version 01	DIP 40	M6003 01 40P
	PLCC 44	M6003 01 44Q
	Film*	M6003 01 TAB
Version 02	PLCC 44*	M6003 02 44Q
	Film*	M6003 02 TAB
Version 03	DIP 40*	M6003 03 40P
	PLCC 44*	M6003 03 44Q
	Film*	M6003 03 TAB
Version 04	PLCC 44*	M6003 04 44Q
	Film*	M6003 04 TAB

* and chip form, on request