Intel® PXA27x Processor Family

Memory Subsystem

Datasheet

Product Features

- **Device Architecture**
  - —Flash die density: 128-, 256-Mbit
  - —LPSDRAM die density: 256-Mbit
  - —Flash + LPDRAM Combo (x16)
  - —Flash + Flash Combo (x32)
- **Device Voltage**
  - —Core: V_{CC} = 1.8 V (Typ)
  - —I/O: V_{CCQ} = 1.8 V (Typ)
- **Device Packaging**
  - —Ball count: 336 balls
  - —Area: 14x14 mm
  - —Height: 1.55 mm
- **SDRAM Architecture and Performance**
  - —Clock rate: 104 MHz
  - —Four internal banks
  - —Burst Length: 1, 2, 4, 8, or full page
- **Quality and Reliability**
  - —Extended Temp: –25 °C to +85 °C
  - —Minimum 100 K flash block erase cycle
  - —0.13 µm ETOX™ VIII flash technology
- **Flash Architecture**
  - —Read-While-Write or Erase
  - —Asymmetrical blocking structure
  - —8-Mbit partition sizes (128-Mbit die)
  - —16-Mbit partition sizes (256-Mbit die)
  - —16-KWord parameter blocks (Bottom)
  - —64-KWord main blocks
  - —2-Kbit One-Time Programmable (OTP) Protection Register
  - —Zero-latency block locking
  - —Absolute write protection with block lock down using F-VPP and F-WP#
- **Flash Performance**
  - —85 ns initial access
  - —25 ns async page-mode read
  - —14 ns sync read (t_{CHQV})
  - —52 MHz CLK
  - —Buffered Enhanced Factory Programming (Buffered EFP): 5 µs/Byte (Typ)
  - —Buffered programming at 7 µs/Byte (Typ)
- **Flash Software**
  - —Intel® FDI, Intel® PSM, and Intel® VFM
  - —Common Flash Interface (CFI)
  - —Basic/Extended Command Set

The Intel® PXA27x Processor Family Memory Subsystem is a stacked device combining high-performance Intel StrataFlash® memory die with or without low-power SDRAM die in Intel® Stacked package. The flash memory features 1.8 V low-power operations with flexible multi-partitions, dual operation Read-While-Write or Read-While-Erase, asynchronous and synchronous reads up to 52 MHz on 0.13 µm ETOX™ VIII flash technology. The LPSDRAM memory features 1.8 V low-power operation up to 104 MHz. The PXA27x processor memory subsystem is stacked on top of Intel® PXA27x Processor for an optimized small form-factor package solution for cellular and PDA applications.

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Contents

Part 1: Electrical, Mechanical, and Thermal Specifications (EMTS) 7

1 Introduction 9
- 1.1 Nomenclature 9
- 1.2 Acronyms 10
- 1.3 Conventions 10

2 Device Overview 13
- 2.1 Intel StrataFlash® Memory Die 13
- 2.2 Device Description 14
- 2.3 Intel® PXA27x Processor Memory Subsystem Block Diagram 20

3 Package Information 23
- 3.1 Package Mechanical Information 23

4 Ballout and Signal Descriptions 27
- 4.1 Ballout Diagrams 27
- 4.2 Signal Descriptions 31

5 Maximum Ratings and Operating Conditions 35
- 5.1 Absolute Maximum Ratings 35
- 5.2 Operating Conditions 36

6 Electrical Specifications 37
- 6.1 Flash DC Current Characteristics 37
- 6.2 Flash DC Voltage Characteristics 38
- 6.3 LPSDRAM DC Characteristics 39

7 AC Characteristics 41
- 7.1 AC Test Conditions 41
- 7.2 Flash AC Read Specifications 42
- 7.3 Flash AC Write Specifications 47
- 7.4 Flash Program and Erase Characteristics 51
- 7.5 LPSDRAM Die Capacitance 51
- 7.6 LPSDRAM AC Characteristics 52

8 Power and Reset Specifications 55
- 8.1 Flash Power-Up and Power-Down 55
- 8.2 Flash Output Disable 55
- 8.3 Flash Standby 55
- 8.4 Flash Reset 55
- 8.5 Flash Power Supply Decoupling 56
- 8.6 Flash Automatic Power Saving 57
- 8.7 LPSDRAM Power-up Sequence and Initialization 57

Part 2: Flash Device Operations 59

9 Device Operations Overview 61

9.1 Flash and LPSDRAM Bus Operations 61
9.2 Flash Bus Operations 64
9.3 Flash Command Definitions 66

10 Flash Read Operations 69

10.1 Flash Asynchronous Page-Mode Read 69
10.2 Flash Synchronous Burst-Mode Read 70
10.2.1 Flash Burst Suspend 70
10.3 Flash Read Configuration Register 70
10.3.1 Flash Read Mode 71
10.3.2 Flash Latency Count 72
10.3.3 Flash Burst Sequence 73
10.3.4 Flash Clock Edge 74
10.3.5 Flash Burst Wrap 74
10.3.6 Flash Burst Length 74

11 Flash Programming Operations 75

11.1 Flash Word Programming 75
11.1.1 Flash Factory Word Programming 76
11.2 Flash Buffered Programming 76
11.3 Flash Buffered Enhanced Factory Programming 77
11.3.1 Flash Buffered EFP Requirements and Considerations 78
11.3.2 Flash Buffered EFP Setup Phase 78
11.3.3 Flash Buffered EFP Program/Verify Phase 78
11.3.4 Flash Buffered EFP Exit Phase 79
11.4 Flash Program Suspend 79
11.5 Flash Program Resume 80
11.6 Flash Program Protection 80

12 Flash Erase Operations 81

12.1 Flash Block Erase 81
12.2 Flash Erase Suspend 81
12.3 Flash Erase Resume 82
12.4 Flash Erase Protection 82

13 Flash Security Modes 83

13.1 Flash Block Locking 83
13.1.1 Flash Lock Block 83
13.1.2 Flash Unlock Block 83
13.1.3 Flash Lock-Down Block 83
13.1.4 Flash Block Lock Status 84
13.1.5 Flash Block Locking During Suspend 84
13.2 Flash One-Time Programmable Protection Registers 85
13.2.1 Flash Reading of the Protection Registers 86
13.2.2 Flash Programming of the Protection Registers 87
13.2.3 Flash Locking the Protection Registers 87

14 Flash Dual-Operation Considerations 89
14.1 Flash Partitioning 89
14.2 Flash Read-While-Write Command Sequences 89
14.2.1 Simultaneous Flash Operation Details 90
14.2.2 Flash Write to Flash Asynchronous Read Transition 90
14.2.3 Flash Write to Flash Synchronous Read Operation Transition 90
14.2.4 Flash Write with Clock Active 90
14.2.5 Flash Read During Flash Buffered Programming 91
14.3 Simultaneous Flash Operation Restrictions 91

15 Special Flash Read States 93
15.1 Flash Read Status Register 93
15.1.1 Flash Clear Status Register 94
15.2 Flash Read Device Identifier 95
15.3 CFI Query 96

Part 3: LPSDRAM Operations 97

16 LSDRAM Register Definition 99
16.1 Mode Register 99
16.2 LPSDRAM Extended Mode Register 100

17 LPSDRAM Command and Operation 101
17.1 LPSDRAM No Operation / LPSDRAM Deselect 101
17.2 LPSDRAM Active 101
17.3 LPSDRAM Read Command 101
17.4 LPSDRAM Write Command 102
17.5 LPSDRAM Power-Down 102
17.6 LPSDRAM Deep Power-Down 103
17.7 LPSDRAM Clock Suspend 103
17.8 LPSDRAM Precharge 103
17.9 LPSDRAM Auto Precharge 103
17.10 LPSDRAM Concurrent Auto Precharge 103
17.11 LPSDRAM Burst Terminate 110
17.12 LPSDRAM Auto Refresh 110
17.13 LPSDRAM Self Refresh 111

Appendix A Flash Flowcharts 113
Appendix B Common Flash Interface 121
Appendix C Intel® PXA27x Processor Memory Subsystem RAM Type ID 133
Appendix D Additional Information 135
Appendix E Ordering Introduction 137

Revision History

Date	Revision	Description
07/04	-001	Initial product document release.

Part 1: Electrical, Mechanical, and Thermal Specifications (EMTS)

Introduction 1

This document contains information pertaining to the PXA27x processor memory subsystem products in the Intel® PXA27x Processor Family. The Intel® PXA27x Processor Family memory subsystem is a stacked device combining high- performance Intel StrataFlash® memory die with or without low-power SDRAM die on Intel® Stacked package. The flash memory features 1.8 V low-power operations with flexible multi-partitions, dual operation Read-While-Write or Read-While-Erase, asynchronous and synchronous reads up to 52 MHz on 0.13 µm ETOX™ VIII flash technology. The LPSDRAM memory features 1.8 V low-power operation up to 104 MHz. The PXA27x processor memory subsystem is stacked on top of Intel® PXA27x Processor for an optimized small form-factor package solution for cellular and PDA applications.

1.1 Nomenclature

1.8 Volt Core	VCC (memory subsystem die core) voltage range of 1.7 V – 1.9 V.
1.8 Volt I/O	VCCQ (memory subsystem die I/O) voltage range of 1.7 V – 1.9 V.
Asserted	Signal with logical voltage level V_{IL}, or enabled.
Block	Group of cells, bits, bytes or words within the flash memory array that get erased with one erase instruction.
Bottom parameter	Previously referred to as a bottom-boot flash, a device with flash parameter partition located at the lowest physical address of its memory map for processor system boot up.
Deasserted	Signal with logical voltage level V_{IH}, or disabled.
Device	A specific memory type or stacked flash + LPSDRAM memory density configuration combination within a memory subsystem product family.
Die	Individual flash or LPSDRAM die used in a stacked package memory subsystem device.
High-Z	High Impedance
Low-Z	Signal is Driven on the bus.
Main block	Any 64-KWord flash array block.
Main partition	A flash partition containing only main blocks.
Non-Array Reads	Flash reads which return flash Device Identifier, CFI Query, Protection Register and Status Register information.
Parameter block	Any 16-KWord flash array block.
Parameter partition	A flash partition containing parameter and main blocks.

Partition	A group of flash blocks that shares common status register read state.
Program	An operation to Write data to the flash array or LPSDRAM.
Write	Bus cycle operation at the inputs of the flash or LPSDRAM die, in which a command or data are sent to the flash array or LPSDRAM.

1.2 Acronyms

APS	Automatic Power Savings
Buffered EFP	Buffered Enhanced Factory Programming
CFI	Common Flash Interface
CSP	Chip Scale Package
CUI	Command User Interface
MLC technology	Multi-Level Cell technology
OTP	One-Time Programmable
PLR	Protection Lock Register
PR	Protection Register
RCR	Read Configuration Register
RFU	Reserved for Future Use (Unused active signals in a package ballout)
RWW / RWE	Read-While-Write / Read-While-Erase
SR	Status Register
WSM	Write State Machine

1.3 Conventions

A5	Denotes one element of a signal group, in this case address bit 5.
Bit	Binary unit, valid range [0,1].
Byte	Eight bits, valid range [0x00 - 0xFF].
Clear	Logical zero (0).
DQ[15:0]	Denotes a group of similarly named signals, such as data bus.
F-CE#	Denotes Chip Enable of flash die, where “F” to denote flash specific signal suffix and “CE#” is the root signal name of the flash die. “D” to denote LPSDRAM type signal.

Gbit	1,073,741,824 bits.
Kbit	1024 bits.
KByte	1024 bytes (8,192 bits).
KWord	1024 words (16,384 bits).
Mbit	1,048,576 bits.
MByte	1,048,576 bytes (8,388,608 bits).
0x	Hexadecimal number prefix.
0b	Binary number prefix.
Set	Logical one (1).
SR.4	A flash status register bit, in this case status register bit 4 of SR[7:0].
VCC	Signal or voltage connection.
V_{CC}	Signal or voltage level.
VSS	Denotes a global power signal of the stacked device, VSS is common to all memory dies within a stacked memory device.
Word	Two bytes or sixteen bits, valid range [0x0000 - 0xFFFF].

Device Overview 2

The PXA27x processor memory subsystem device combines 128- or 256-Mbit Intel StrataFlash® memory die with or without 256-Mbit low-power SDRAM die on Intel stacked package. The following section describes the PXA27x processor memory subsystem features, operation, and characteristics of the flash and LPSDRAM devices.

2.1 Intel StrataFlash® Memory Die

The flash die provides read-while-write or read-while-erase capability with density upgrades of 256-Mbit increments. The flash die provides high-performance at low voltage on a 16-bit data bus and individually erasable memory blocks sized for optimum code and data storage.

The flash die contains one parameter partition and several main partitions. The flash memory arrays are grouped into multiple 8-Mbit partition for 128-Mbit flash die, or 16-Mbit partitions for 256-Mbit flash die. By dividing the flash memory into partitions, program or erase operations can take place simultaneously as read operation. Although each partition has write, erase, and burst read capabilities, simultaneous operations are limited to write or erase in one partition while reading in the another partition. Burst reads across partition boundaries are allow, but the burst reads are not allow to cross into a partition that is busy in programming or erasing mode, or across flash dies within the PXA27x processor memory subsystem. A new burst read operation must be initiated when crossing these bondaries.

Upon initial power up or return from reset, the flash defaults to asynchronous page-mode read. Configuring the Read Configuration Register (RCR) enables flash synchronous burst-mode reads. In synchronous burst-mode, output data are synchronized with the memory bus clock signal.

In addition to the enhanced architecture and interface, the flash die incorporates technology that enables fast factory program and erase operations. Designed for low-voltage systems, the flash supports read operations with F-VCC at 1.8 volt, and erase and program operations with F-VPP at 1.8 V or 9.0 V. Buffered Enhanced Factory Programming (Buffered EFP) provides the fastest flash array programming performance with F-VPP at 9.0 volt, which increases factory throughput. With F-VPP at 1.8 V, F-V_{CC} and F-VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated F-VPP connection provides complete data protection when F-VPP is less than V_{PPLK}.

A flash Command User Interface (CUI) is the interface between the PXA27x processor and all internal operations of each selected flash die. An internal flash Write State Machine (WSM) automatically executes, for example, the algorithms and timings necessary for block erase and program. A Status Register indicates erase or program completion and any errors that may have occurred.

An industry-standard flash command sequence invokes program and erase automation. Each erase operation erases one block at a time. The Erase Suspend feature allows system interrupt to pause an erase cycle to read or program data in another block in another partition. Program Suspend allows system interrupt to pause programming to read other locations. The flash array is programmed in 16-bits increments.

The flash offers power savings through Automatic Power Savings (APS) mode and standby mode. The individual flash die automatically enters APS mode following read-cycle completion. Standby is initiated when the PXA27x processor deselects the flash by deasserting F-CE# or by asserting F-RST#. Combined, these features can significantly reduce power consumption.

For security requirement, each flash die features 2048-bits of One-Time Protection (OTP) register allows unique flash identification that can be used to increase system security. In addition, the individual flexible Block Lock feature provides zero-latency block locking and unlocking.

2.2 Device Description

The PXA27x processor memory subsystem device combines high-performance Intel StrataFlash® memory die with low-power SDRAM die for 16-bit and Intel StrataFlash® memory only dies for 32-bit operations on Intel stacked package. Table 1, "PXA27x Processor Memory Subsystem Signals for 16-bit Interface" and Table 2, "PXA27x Processor Memory Subsystem Signals for 32-bit Interface" on page 17 provide the signal relationships between the Intel® PXA27x Processor device (bottom package) signal names with the PXA27x processor memory subsystem (top package) device respectively for x16 or x32 bit interfaces.

Table 1. Intel® PXA27x Processor Memory Subsystem Signals for 16-bit Interface (Sheet 1 of 4)

Ball#	Type	Ball Name	SDRAM	Flash	PXA27x
W18	Input	DQM<0>	D-DM[1]	—	DQM<0>
P17	Input	DQM<1>	D-DM[0]	—	DQM<1>
T17	Input	DQM<2>	—	—	DQM<2>
W17	Input	DQM<3>	—	—	DQM<3>
W1	Input	NCS<0>	—	F-CE#	nCS<0>
V18	Input	NSDCS<0>	D-CS#	—	nSDCS<0>
W20	Input	NWE	WE#	WE#	nWE
W19	Input	NOE	—	OE#	nOE
U20	Input	NSDCAS	D-CAS#	ADV#	nSDCAS
Y19	Input	NSDRAS	D-RAS#	—	nSDRAS
V19	Input	SDCLK<3>	—	F-CLK	SDCLK<3>
P19	Input	SDCLK<1>	R-CLK	—	SDCLK<1>
T18	Input	SDCKE	D-CKE	—	SDCKE
W15	Input	NF_WP<0>	—	F-WP#	—
N6	Bidirectional	MD<15>	DQ0	DQ15	MD<15>
M6	Bidirectional	MD<14>	DQ1	DQ14	MD<14>
R8	Bidirectional	MD<13>	DQ3	DQ13	MD<13>
R9	Bidirectional	MD<12>	DQ2	DQ12	MD<12>
R10	Bidirectional	MD<11>	DQ5	DQ11	MD<11>
T11	Bidirectional	MD<10>	DQ4	DQ10	MD<10>
T12	Bidirectional	MD<9>	DQ7	DQ9	MD<9>
R14	Bidirectional	MD<8>	DQ6	DQ8	MD<8>

Table 1. Intel® PXA27x Processor Memory Subsystem Signals for 16-bit Interface (Sheet 2 of 4)

Ball#	Type	Ball Name	SDRAM	Flash	PXA27x
V13	Bidirectional	MD<7>	DQ9	DQ7	MD<7>
T14	Bidirectional	MD<6>	DQ8	DQ6	MD<6>
M15	Bidirectional	MD<5>	DQ11	DQ5	MD<5>
M16	Bidirectional	MD<4>	DQ10	DQ4	MD<4>
V15	Bidirectional	MD<3>	DQ13	DQ3	MD<3>
P16	Bidirectional	MD<2>	DQ12	DQ2	MD<2>
M17	Bidirectional	MD<1>	DQ15	DQ1	MD<1>
U17	Bidirectional	MD<0>	DQ14	DQ0	MD<0>
V2	Input	MA<25>	—	—	MA<25>
W2	Input	MA<24>	D-BA1	A23	MA<24>
W4	Input	MA<23>	D-BA0	A22	MA<23>
Y4	Input	MA<22>	—	A21	MA<22>
W5	Input	MA<21>	—	A20	MA<21>
T4	Input	MA<20>	—	A19	MA<20>
R4	Input	MA<19>	—	A18	MA<19>
P2	Input	MA<18>	—	A17	MA<18>
W6	Input	MA<17>	—	A16	MA<17>
T5	Input	MA<16>	—	A15	MA<16>
R5	Input	MA<15>	—	A14	MA<15>
V6	Input	MA<14>	—	A13	MA<14>
U6	Input	MA<13>	A12	A12	MA<13>
T6	Input	MA<12>	A11	A11	MA<12>
W7	Input	MA<11>	A10	A10	MA<11>
P4	Input	MA<10>	A9	A9	MA<10>
P5	Input	MA<9>	A8	A8	MA<9>
T7	Input	MA<8>	A7	A7	MA<8>
R6	Input	MA<7>	A6	A6	MA<7>
N5	Input	MA<6>	A5	A5	MA<6>
W8	Input	MA<5>	A4	A4	MA<5>
R7	Input	MA<4>	A3	A3	MA<4>
P6	Input	MA<3>	A2	A2	MA<3>
T8	Input	MA<2>	A1	A1	MA<2>
Y3	Input	MA<1>	A0	A0[2]	MA<1>
W3	Input	MA<0>	—	—	MA<0>
Y8	Input	NF_RST	—	F-RST#	—
W10	Supply	F_VPP	—	F-VPP	—

Table 1. Intel® PXA27x Processor Memory Subsystem Signals for 16-bit Interface (Sheet 3 of 4)

Ball#	Type	Ball Name	SDRAM	Flash	PXA27x
N1/ T2/ V5/ V7/ V8/ V9/ V10/ V11/ V12/ V14/ V16/ V17/ R19/ N20/ P20/ R1/ Y6/ Y7/ Y10/ Y11/ Y12/ Y13/ Y16/ Y20/	PXA27x processor memory subsystem Core Supply	VCC_MEM	D-VCC	F-VCC	VCC_MEM
U19/ Y2/ N2/ N18/ P18/ T1/ U5/ U7/ U8/ U9/ U10/ U11/ U12/ U14/ U16/ W11/ Y5/ Y9/ Y17	PXA27x processor memory subsystem I/O Supply	VSS_MEM	VSSQ	VSSQ	VSS_MEM
A18/ A19/ A20/ B20/ C20/ C15/ D19	Supply	VSS	VSS	VSS	VSS

Table 1. Intel® PXA27x Processor Memory Subsystem Signals for 16-bit Interface (Sheet 4 of 4)

Ball#	Type	Ball Name	SDRAM	Flash	PXA27x
W9/ W12/ W13/ W16/ Y15/ Y18	RFU	RFU	—	—	—
Y14	Input	NF_WP<1>[1]	—	—	—

Notes:
1. NF_WP<1> is reserved for a stacked data-core flash memory write protect pin (not yet available in current PXA27x processor configurations), in the top package.
2. Address signals are shifted by one for 16-bit flash to align the PXA27x processor memory subsystem with the processor and system design requirements.

Table 2. Intel® PXA27x Processor Memory Subsystem Signals for 32-bit Interface (Sheet 1 of 4)

Ball#	Type	Ball Name	Flash Die #1	Flash Die #2	PXA27x
W1	Input	NCS<0>	F-CE#	F-CE#	nCS<0>
W20	Input	NWE	WE#	WE#	nWE
W19	Input	NOE	OE#	OE#	nOE
U20	Input	NSDCAS	ADV#	ADV#	nSDCAS
V19	Input	SDCLK<3>	F-CLK	F-CLK	SDCLK<3>
W15	Input	NF_WP<0>	F-WP#	F-WP#	—
M5	Bidirectional	MD<31>	—	DQ15	MD<31>
L5	Bidirectional	MD<30>	—	DQ14	MD<30>
L6	Bidirectional	MD<29>	—	DQ13	MD<29>
T9	Bidirectional	MD<28>	—	DQ12	MD<28>
T10	Bidirectional	MD<27>	—	DQ11	MD<27>
R11	Bidirectional	MD<26>	—	DQ10	MD<26>
R12	Bidirectional	MD<25>	—	DQ9	MD<25>
U13	Bidirectional	MD<24>	—	DQ8	MD<24>
P15	Bidirectional	MD<23>	—	DQ7	MD<23>
R15	Bidirectional	MD<22>	—	DQ6	MD<22>
N15	Bidirectional	MD<21>	—	DQ5	MD<21>
W14	Bidirectional	MD<20>	—	DQ4	MD<20>
U15	Bidirectional	MD<19>	—	DQ3	MD<19>
T16	Bidirectional	MD<18>	—	DQ2	MD<18>
N16	Bidirectional	MD<17>	—	DQ1	MD<17>
N17	Bidirectional	MD<16>	—	DQ0	MD<16>
N6	Bidirectional	MD<15>	DQ15	—	MD<15>
M6	Bidirectional	MD<14>	DQ14	—	MD<14>
R8	Bidirectional	MD<13>	DQ13	—	MD<13>
R9	Bidirectional	MD<12>	DQ12	—	MD<12>

Table 2. Intel® PXA27x Processor Memory Subsystem Signals for 32-bit Interface (Sheet 2 of 4)

Ball#	Type	Ball Name	Flash Die #1	Flash Die #2	PXA27x
R10	Bidirectional	MD<11>	DQ11	—	MD<11>
T11	Bidirectional	MD<10>	DQ10	—	MD<10>
T12	Bidirectional	MD<9>	DQ9	—	MD<9>
R14	Bidirectional	MD<8>	DQ8	—	MD<8>
V13	Bidirectional	MD<7>	DQ7	—	MD<7>
T14	Bidirectional	MD<6>	DQ6	—	MD<6>
M15	Bidirectional	MD<5>	DQ5	—	MD<5>
M16	Bidirectional	MD<4>	DQ4	—	MD<4>
V15	Bidirectional	MD<3>	DQ3	—	MD<3>
P16	Bidirectional	MD<2>	DQ2	—	MD<2>
M17	Bidirectional	MD<1>	DQ1	—	MD<1>
U17	Bidirectional	MD<0>	DQ0	—	MD<0>
V2	Input	MA<25>	A23	A23	MA<25>
W2	Input	MA<24>	A22	A22	MA<24>
W4	Input	MA<23>	A21	A21	MA<23>
Y4	Input	MA<22>	A20	A20	MA<22>
W5	Input	MA<21>	A19	A19	MA<21>
T4	Input	MA<20>	A18	A18	MA<20>
R4	Input	MA<19>	A17	A17	MA<19>
P2	Input	MA<18>	A16	A16	MA<18>
W6	Input	MA<17>	A15	A15	MA<17>
T5	Input	MA<16>	A14	A14	MA<16>
R5	Input	MA<15>	A13	A13	MA<15>
V6	Input	MA<14>	A12	A12	MA<14>
U6	Input	MA<13>	A11	A11	MA<13>
T6	Input	MA<12>	A10	A10	MA<12>
W7	Input	MA<11>	A9	A9	MA<11>
P4	Input	MA<10>	A8	A8	MA<10>
P5	Input	MA<9>	A7	A7	MA<9>
T7	Input	MA<8>	A6	A6	MA<8>
R6	Input	MA<7>	A5	A5	MA<7>
N5	Input	MA<6>	A4	A4	MA<6>
W8	Input	MA<5>	A3	A3	MA<5>
R7	Input	MA<4>	A2	A2	MA<4>
P6	Input	MA<3>	A1	A1	MA<3>
T8	Input	MA<2>	A0[2]	A0[2]	MA<2>
Y3	Input	MA<1>	—	—	MA<1>
W3	Input	MA<0>	—	—	MA<0>

Table 2. Intel® PXA27x Processor Memory Subsystem Signals for 32-bit Interface (Sheet 3 of 4)

Ball#	Type	Ball Name	Flash Die #1	Flash Die #2	PXA27x
Y8	Input	NF_RST	F-RST#	F-RST#	—
W10	Supply	F_VPP	F-VPP	F-VPP	—
N1/ T2/ V5/ V7/ V8/ V9/ V10/ V11/ V12/ V14/ V16/ V17/ R19/ N20/ P20/ R1/ Y6/ Y7/ Y10/ Y11/ Y12/ Y13/ Y16/ Y20/	PXA27x processor memory subsystem Core Supply	VCC_MEM	D-VCC	F-VCC	VCC_MEM
U19/ Y2/ N2/ N18/ P18/ T1/ U5/ U7/ U8/ U9/ U10/ U11/ U12/ U14/ U16/ W11/ Y5/ Y9/ Y17	PXA27x processor memory subsystem I/O Supply	VSS_MEM	VSSQ	VSSQ	VSS_MEM
A18/ A19/ A20/ B20/ C20/ C15/ D19	Supply	VSS	VSS	VSS	VSS

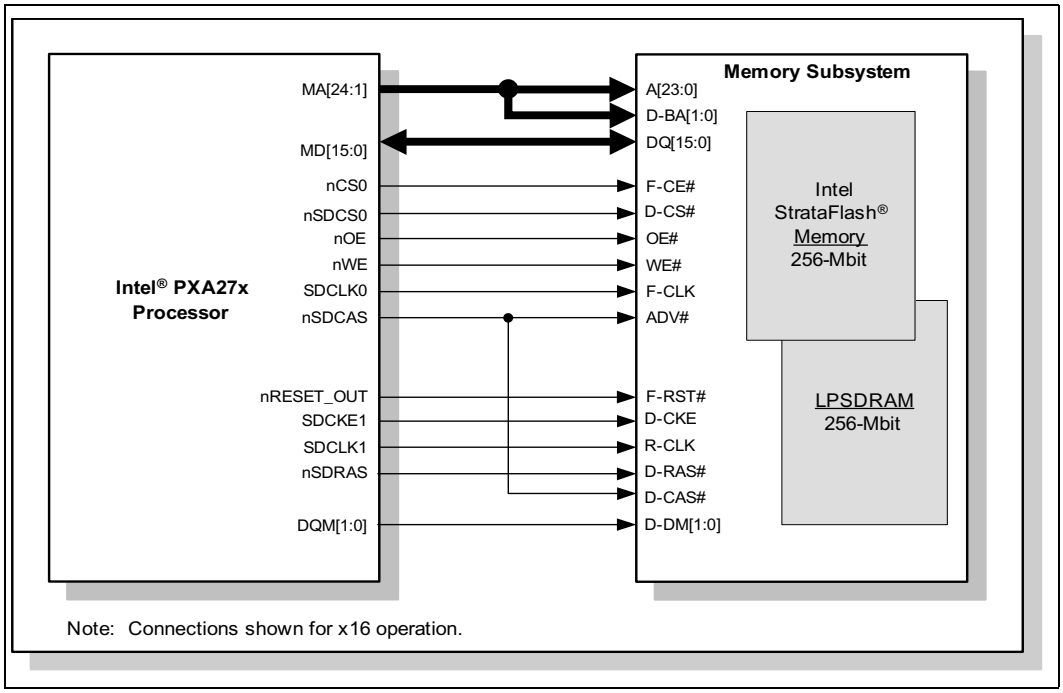
Table 2. Intel® PXA27x Processor Memory Subsystem Signals for 32-bit Interface (Sheet 4 of 4)

Ball#	Type	Ball Name	Flash Die #1	Flash Die #2	PXA27x
W9/ W12/ W13/ W16/ Y15/ Y18	RFU	RFU	—	—	—
Y14	Input	NF_WP<1>[1]	—	—	—

NOTES:
1. NF_WP<1> is reserved for a stacked data-core flash memory write protect pin (not yet available in current PXA27x processor configurations), in the top package.
2. Address signals in the stacked datasheet are shifted by two for 32-bit flash to align the PXA27x processor memory subsystem with the processor and system design requirements.

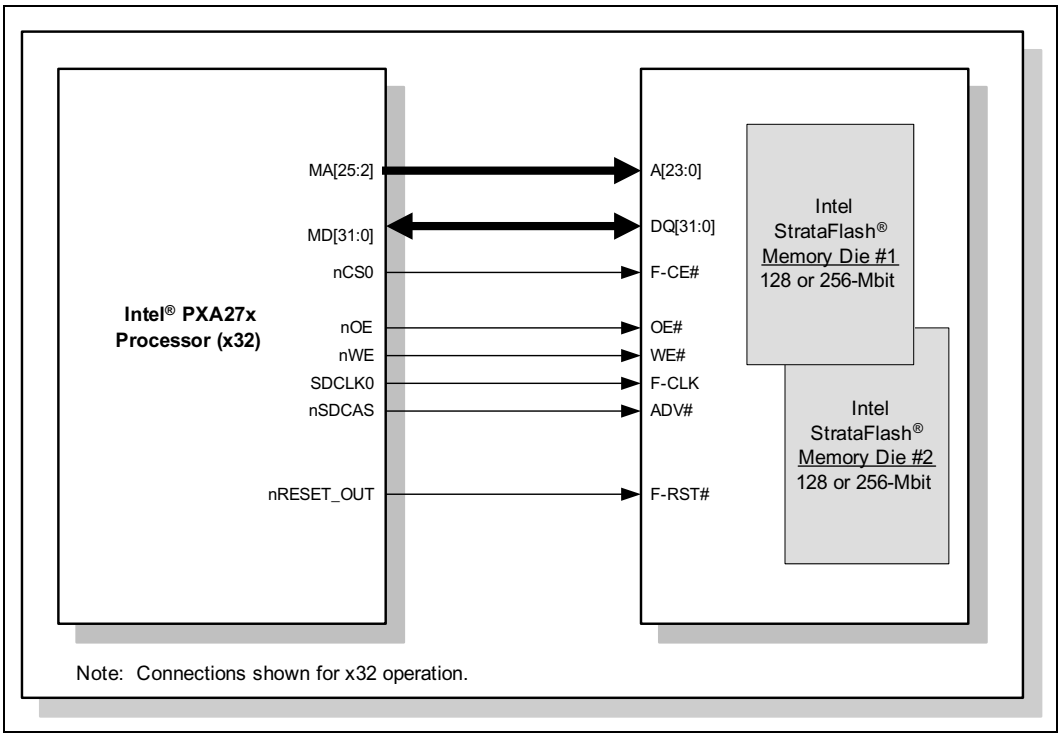
2.3 Intel® PXA27x Processor Memory Subsystem Block Diagram

Figure 1. Intel® PXA27x Processor Memory Subsystem (x16) Device Block Diagram[1]



Note: PXA271 = PXA27x CPU + 256-Mbit Flash + 256-Mbit LPSDRAM (x16 configuration) device

Figure 2. Intel® PXA27x Processor Memory Subsystem (x32) Device Block Diagram[1,2]



Notes:
1. PXA272 = PXA27x CPU + 128-Mbit Flash + 128-Mbit Flash (x32 configuration) device.
2. PXA273 = PXA27x CPU + 256-Mbit Flash + 256-Mbit Flash (x32 configuration) device.

Package Information 3

This section provides the package mechanical specifications for the Intel® PXA27x Processor with PXA27x processor memory subsystem device.

The Intel® PXA27x Processor with PXA27x processor memory subsystem device is provided in a 14 mm x 14 mm, 336-pin, 0.650 mm FS-CSP molded matrix array package, as shown in Figure 3, Figure 4, and Table 3, "Intel® PXA27x Processor with Memory Subsystem Dimensions" on page 24.

3.1 Package Mechanical Information

Figure 3. Intel® PXA27x Processor with Memory Subsystem Mechanical Details - Top View

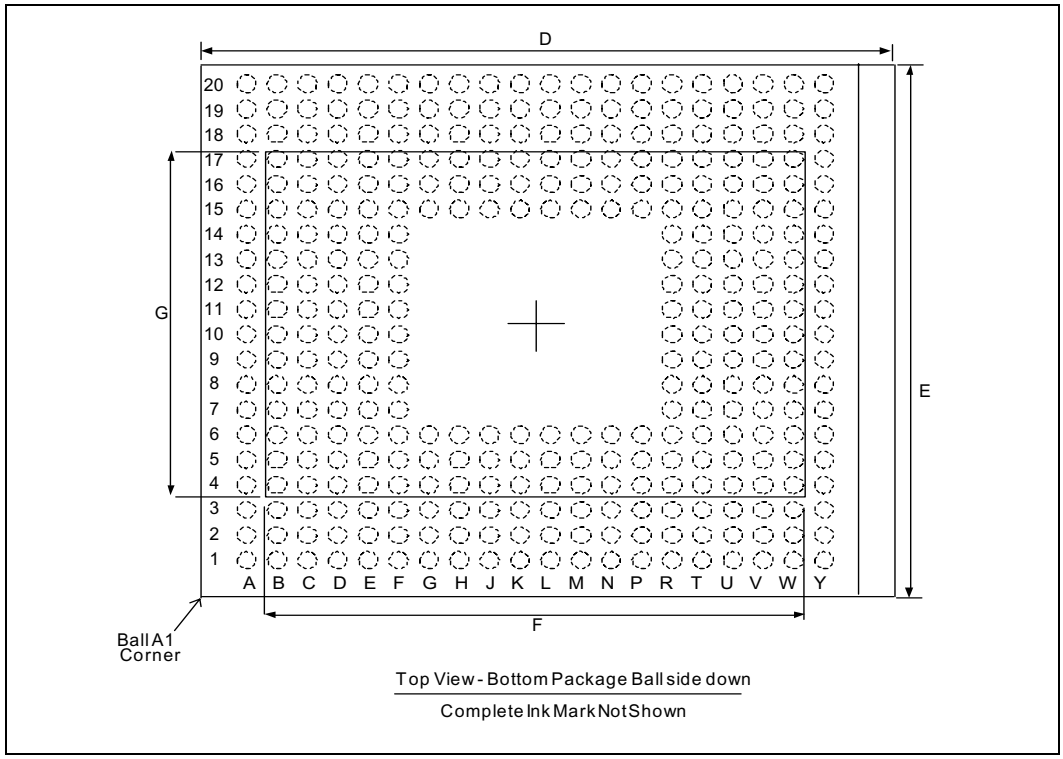


Figure 4. Intel® PXA27x Processor with Memory Subsystem Mechanical Details - Side View

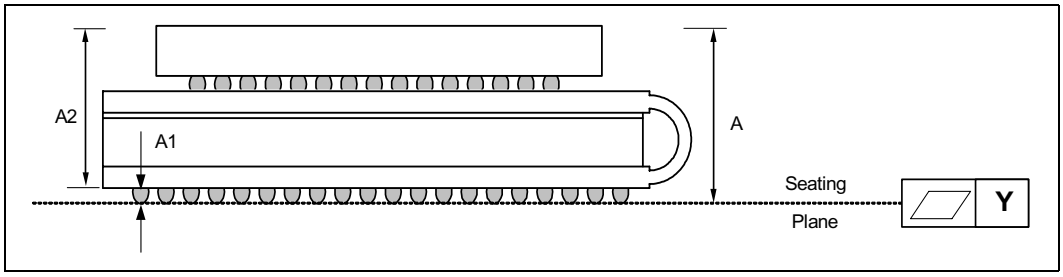
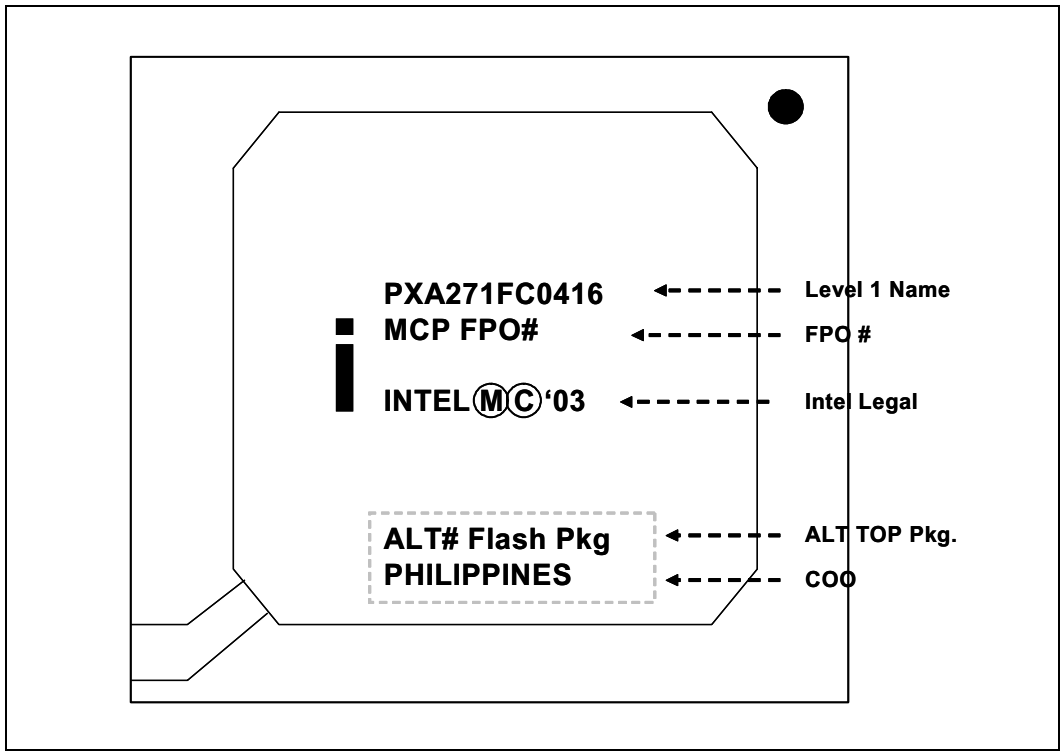


Table 3. Intel® PXA27x Processor with Memory Subsystem Dimensions

Dimension	Symbol	Min	Typical	Max
Pacakge Height	A			1.55
Ball Height	A1	0.180		
Package Body Thickness	A2	1.121		1.195
Ball (Lead) Width	b	0.350	0.4	0.450
Bottom Package Body Width	D	13.9	14	14.1
Bottom Package Body Length	E	13.9	14	14.1
Top Package Body Width	F	10.9	11	11.1
Top Package Body Length	G	12.9	13	13.1
Pitch	[e]		0.650	
Ball (Lead) Count	N		336	
Seating Plane Coplanarity	Y			0.150
Corner to Ball A1 Distance Along D	S1		0.825	
Corner to Ball A1 Distance Along E	S2		0.825	
NOTE: All mechanical dimensions are in milimeters (mm).				

Figure 5. Intel® PXA27x Processor with Memory Subsystem Package Marking



Ballout and Signal Descriptions 4

This section provides the ballout diagrams and signal descriptions for the Intel® PXA27x Processor with Memory Subsystem device.

4.1 Ballout Diagrams

Figure 6. Intel® PXA27x Processor with Memory Subsystem Ball Map, Top Left Quarter

	1	2	3	4	5	6	7	8	9	10
A	VCC_USB	VCC_USB	GPIO<89>	GPIO<42>	USBH_N<1>	USBH_P<1>	GPIO<90>	GPIO<61>	GPIO<65>	GPIO<71>
B	GPIO<118>	GPIO<119>	GPIO<88>	GPIO<43>	GPIO<115>	UIO	VCC_CORE	VCC_LCD	VCC_CORE	GPIO<70>
C	VSS_CORE	USBC_N	GPIO<120>	GPIO<116>	GPIO<114>	VCC_USIM	GPIO<91>	GPIO<63>	GPIO<64>	GPIO<69>
D	VCC_USB	USBC_P	GPIO<44>	GPIO<39>	GPIO<41>	VSS_IO	GPIO<58>	GPIO<59>	VSS_IO	GPIO<68>
E	VCC_CORE	GPIO<117>	GPIO<35>	VSS_IO	GPIO<109>	GPIO<16>	VSS_CORE	GPIO<62>	GPIO<66>	VSS_CORE
F	GPIO<45>	GPIO<34>	GPIO<32>	GPIO<110>	GPIO<111>	GPIO<25>	GPIO<22>	GPIO<60>	VSS_CORE	GPIO<67>
G	GPIO<112>	GPIO<92>	GPIO<17>	GPIO<36>	GPIO<37>	GPIO<30>				
H	GPIO<23>	GPIO<24>	GPIO<26>	GPIO<27>	GPIO<38>	GPIO<46>				
J	VCC_IO	VSS_IO	GPIO<40>	GPIO<31>	VSS_CORE	GPIO<11>				
K	GPIO<28>	GPIO<29>	VCC_CORE	GPIO<113>	GPIO<47>	VSS_CORE				

Figure 7. Intel® PXA27x Processor with Memory Subsystem Ball Map, Top Right Quarter

11	12	13	14	15	16	17	18	19	20	
VCC_LCD	VCC_CORE	TESTCLK	GPIO<9>	GPIO<0>	NRESET	TXTAL_OUT	VSS	VSS	VSS	**A**
VCC_CORE	GPIO<14>	VSS_IO	TDI	GPIO<4>	PWR_EN	TXTAL_IN	BOOT_SEL	NRESET_OUT	VSS	**B**
GPIO<86>	GPIO<75>	TMS	NTRST	VSS	GPIO<3>	NVDD_FAULT	NBATT_FAULT	PWR_CAP<0>	VSS	**C**
GPIO<87>	GPIO<76>	GPIO<77>	TDO	GPIO<10>	GPIO<1>	SYS_EN	PWR_CAP<1>	VSS	PWR_OUT	**D**
GPIO<72>	VSS_IO	GPIO<74>	TCK	CLK_REQ	PWR_CAP<3>	VCC_BATT	PWR_CAP<2>	PXTAL_IN	PXTAL_OUT	**E**
VSS_CORE	GPIO<73>	VSS_CORE	GPIO<19>	GPIO<97>	GPIO<94>	GPIO<96>	VCC_PLL	VSS_PLL	VSS_IO	**F**
				VSS_IO	GPIO<100>	GPIO<99>	GPIO<98>	GPIO<93>	GPIO<95>	**G**
				VSS_CORE	GPIO<106>	GPIO<104>	GPIO<101>	GPIO<102>	VCC_IO	**H**
				GPIO<51>	GPIO<108>	GPIO<107>	GPIO<105>	VCC_CORE	GPIO<103>	**J**
				GPIO<81>	VSS_BB	GPIO<50>	GPIO<52>	GPIO<53>	GPIO<54>	**K**

Figure 8. Intel® PXA27x Processor with Memory Subsystem Ball Map, Bottom Left Quarter

L	VCC_IO	VSS_IO	GPIO<12>	GPIO<13>	MD<30>	MD<29>				
M	GPIO<49>	GPIO<18>	VCC_SRAM	RDNWR	MD<31>	MD<14>				
N	VCC_MEM	VSS_MEM	VCC_SRAM	VSS_CORE	MA<6>	MD<15>				
P	GPIO<80>	MA<18>	GPIO<79>	MA<10>	MA<9>	MA<3>				
R	VCC_MEM	VCC_CORE	VCC_SRAM	MA<19>	MA<15>	MA<7>	MA<4>	MD<13>	MD<12>	MD<11>
T	VSS_MEM	VCC_MEM	GPIO<33>	MA<20>	MA<16>	MA<12>	MA<8>	MA<2>	MD<28>	MD<27>
U	VCC_CORE	VSS_CORE	VCC_SRAM	VSS_CORE	VSS_MEM	MA<13>	VSS_MEM	VSS_MEM	VSS_MEM	VSS_MEM
V	GPIO<15>	MA<25>	VSS_CORE	GPIO<78>	VCC_MEM	MA<14>	VCC_MEM	VCC_MEM	VCC_MEM	VCC_MEM
W	NCS<0>	MA<24>	MA<0>	MA<23>	MA<21>	MA<17>	MA<11>	MA<5>	RFU	F_VPP
Y	VSS_CORE	VSS_MEM	MA<1>	MA<22>	VSS_MEM	VCC_MEM	VCC_MEM	NF_RST	VSS_MEM	VCC_MEM
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**

Figure 9. Intel® PXA27x Processor with Memory Subsystem Ball Map, Bottom Right Quarter

				GPIO<85>	GPIO<55>	GPIO<57>	GPIO<48>	VCC_CORE	VCC_BB	**L**
				MD<5>	MD<4>	MD<1>	GPIO<56>	GPIO<83>	GPIO<84>	**M**
				MD<21>	MD<17>	MD<16>	VSS_MEM	GPIO<82>	VCC_MEM	**N**
				MD<23>	MD<2>	DQM<1>	VSS_MEM	SDCLK<1>	VCC_MEM	**P**
MD<26>	MD<25>	VSS_CORE	MD<8>	MD<22>	VSS_CORE	NSDCS<1>	GPIO<21>	VCC_MEM	VCC_CORE	**R**
MD<10>	MD<9>	VCC_CORE	MD<6>	VCC_CORE	MD<18>	DQM<2>	SDCKE	SDCLK<2>	GPIO<20>	**T**
VSS_MEM	VSS_MEM	MD<24>	VSS_MEM	MD<19>	VSS_MEM	MD<0>	VSS_CORE	VSS_MEM	NSDCAS	**U**
VCC_MEM	VCC_MEM	MD<7>	VCC_MEM	MD<3>	VCC_MEM	VCC_MEM	NSDCS<0>	SDCLK<3>	SDCLK<0>	**V**
VSS_MEM	RFU	RFU	MD<20>	NF_WP<0>	RFU	DQM<3>	DQM<0>	NOE	NWE	**W**
VCC_MEM	VCC_MEM	VCC_MEM	NF_WP<1>	RFU	VCC_MEM	VSS_MEM	RFU	NSDRAS	VCC_MEM	**Y**
11	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	

Note: "RFU" means "Reserved for Future Use." Please contact your local Intel representative for recommendations on what PCB designers can do with the RFUs.

4.2 Signal Descriptions

Table 4 describes the active signals for the PXA27x processor memory subsystem.

Table 4. Intel® PXA27x Processor Memory Subsystem Signal Descriptions (Sheet 1 of 3)

Symbol	Type	Name and Function
A[MAX:MIN]	Input	**ADDRESS:** Global device signals. Share inputs for all memory die addresses during read and write operations. For 16-bit bus operations, A[24:1] signal balls are used, while 32-bit bus operations, A[25:2] are used. This is due to the PXA27x processor addresses shift as compare to the flash and LPSDRAM die. Flash die addressability: A[23:0] for 256-Mbit die; A[22:0] for 128-Mbit die. For 256-Mbit LPSDRAM die: A[13:1] are the row and A[9:1] are the column addresses. • LPSDRAM Address inputs also provide the op-code during a Mode Register Set or Special Mode Register Set command. • A11 defines the Auto Precharge. During a LPSDRAM Precharge command, A11 is sampled to determine if all banks are to be precharged (A11 = HIGH).
DQ[MAX:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during write cycles, outputs data during read cycles. Data signals float when the device or its output are deselected. Data are internally latched during writes on the device. • DQ[15:0] are used for 16-bit bus operations. • DQ[31:0] are used for 32-bit bus operations.
ADV#	Input	**ADDRESS VALID:** Low-true input. During synchronous flash read operations, addresses are latched on the rising edge of ADV#, or on the next valid F-CLK edge, whichever occurs first. In asynchronous flash read operation, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.
F-CE#	Input	**FLASH CHIP ENABLE:** Low-true input. F-CE# low selects the associated flash memory die. F-CE# high deselects the associated flash die. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data outputs are placed in high-Z state.
F-CLK, R-CLK	Input	**CLOCK:** Synchronizes the selected memory die to the PXA27x memory bus clock in synchronous operations. • F-CLK is a flash signal. Synchronizes the flash die to the PXA27x memory bus frequency in synchronous operations. • R-CLK is a LPSDRAM input signal. Synchronizes the LPSDRAM die to the PXA27x memory bus clock. LPSDRAM is sampled on the positive edge of R-CLK. R-CLK also increments the internal burst counter and controls the output registers.
OE#	Input	**OUTPUT ENABLE:** Low-true input. OE# low enables the output drivers of the selected flash die. OE# high places the flash output drivers of the selected die in high-Z.
F-RST#	Input	**FLASH RESET:** Low-true input. F-RST# low resets internal operations and inhibits write operations. F-RST# high enables normal operation. Exit from reset places the flash device in asynchronous read array mode.
WAIT	Output	**DEVICE WAIT:** Flash die configurable Low-True or High-True output. Indicates data is valid in synchronous array or non-array sync flash reads. Configuration Register bit 10 (CR.10, WT) determines its polarity when asserted. With F-CE# and OE# at V_{IL}, WAIT's active output is V_{OL} or V_{OH}. WAIT is high-Z if F-CE# or OE# is V_{IH}. • In synchronous array or non-array flash read modes, WAIT indicates invalid data when asserted and valid data when deasserted. • In asynchronous flash page read, and all flash write modes, WAIT is deasserted.

Table 4. Intel® PXA27x Processor Memory Subsystem Signal Descriptions (Sheet 2 of 3)

Symbol	Type	Name and Function
WE#	Input	**WRITE ENABLE:** Global device signal. Low-true input. • For flash operation, WE# low selects the associated memory die for write operation. WE# high deselect the associated memory die, data are placed in high-Z state. • For LPSDRAM operation, WE# is latched on the positive clock edge in conjunction with the D-RAS# and D-CAS# signals. The WE# input is used to select the Bank Activate or Precharge command and Read or Write command.
F-WP#	Input	**FLASH WRITE PROTECT:** Low-true input. F-WP# low enables the Lock-Down flash mechanism. Blocks in a lock-down state cannot be unlocked with the Unlock command. F-WP# high overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command.
D-CKE	Input	**LPSDRAM Clock Enable:** High-true input • D-CKE low synchronously with clock, the internal clock is suspended from the next clock cycle. • The state of the outputs and the burst address is halted. When all banks are in the idle state, D-CKE is high, the LPDRAM enters into Power-Down and Self Refresh modes. • D-CKE is synchronous except after the device enters Power-Down and Self Refresh modes, where D-CKE becomes asynchronous until exiting the same mode. The input buffers, including R-CLK, are disabled during Power-Down and Self Refresh modes, providing low standby power.
D-BA[1:0]	Input	**LPSDRAM Bank Select:** Low-true input. D-BA0 and D-BA1 defines to which bank the Bank Activate, Read, Write, or Bank Pre-charge command is being applied. The bank address D-BA0 and D-BA1 are used to latched in mode register set.
D-RAS#	Input	**LPSDRAM Row Address Strobe:** Low-true input. • The D-RAS# signal defines the operation commands, with the D-CAS# and WE# signals. • The D-RAS# is latched at the rising edges of R-CLK. When D-RAS# and D-CS# are asserted and D-CAS# is deasserted, either the Bank Activate command or the Precharge command is selected by the WE# signal. • WE# is deasserted, the Bank Activate command is selected and the bank designated by D-BA[1:0] is turned on to the active state.
D-CAS#	Input	**LPSDRAM Column Address Strobe:** Low-true input. • D-CAS# signal defines the operation commands in conjunction with the D-RAS# and WE# signals and is latched at the rising edges of R-CLK. • D-RAS# is deasserted and D-CS# is asserted, the column access is started by asserting D-CAS#. Read or Write command then is selected by asserting WE# low or high.
D-CS#	Input	**LPSDRAM Chip Select:** Low-true input. D-CS# low selects the associated LPSDRAM memory die. All commands are masked when D-CS# high. D-CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
D-DM[1:0]	Input	**LPSDRAM Data Input/Output Mask:** Data Input Mask. • D-DM[1:0] are byte selects. Input data is masked when D-DM[1:0] are sampled HIGH during a write cycle. D-DM1 masks DQ[15-8], and D-DM0 masks DQ[7-0]. • The D-DM[1:0] latency for Read is 2 Clocks and for Write is 0 Clocks.
F-VPP	Power	**FLASH ERASE/ PROGRAM VOLTAGE:** Flash specific signal. Valid F-VPP voltage on this ball allows flash block erase or program functions. Flash memory array contents cannot be altered when F-VPP ≤ V_{PPLK}. Flash block erase and program at invalid F-VPP voltage should not be attempted.
F-VCC	Power	**FLASH CORE VOLTAGE LEVEL:** Flash specific signals. Flash core source voltage. • Flash operations are inhibited when F-V_{CC} ≤ V_{LKO}. Operations at invalid F-VCC voltage should not be attempted.

Table 4. Intel® PXA27x Processor Memory Subsystem Signal Descriptions (Sheet 3 of 3)

Symbol	Type	Name and Function
VCCQ	Power	**OUTPUT VOLTAGE LEVEL:** Global device signals. Device input/output-driver source voltage within its operatng voltage range.
D-VCC	Power	**LPSDRAM POWER SUPPLY:** Supplies power to the LPSDRAM die. • D-VCC supplies power for LPSDRAM operation.
F-VCC	Power	**FLASH POWER SUPPLY:** Supplies power to the Flash die. • F-VCC supplies power for Flash operation.
VSS[1]	Power	**GROUND:** Global ground reference for device memory core type voltages.
DU	-	**DO NOT USE:** This ball must be left floating. This ball should not be connected to any power supplies, signals, or other balls.
RFU[2]	-	**RESERVED for FUTURE USE:** Reserved by Intel for future device functionality and enhancements.

Notes:
1. Connect all VSS to system ground. Do not float any VSS connections.
2. Please contact your local Intel representative for details.

Maximum Ratings and Operating Conditions 5

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. See Table 5.

Table 5. Intel® PXA27x Processor Memory Subsystem Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Case Temperature under bias	–25	+85	°C	
Storage temperature	–55	+125		
Voltage on any flash signals (except F-V_{CC}, F-VPP) relative to VSS	–0.5	+3.8	V	1
Voltage on any LPSDRAM signals	–0.5	+2.6		1
F-VPP voltage	–0.2	+10		1,2
F-V_{CC} and D-VCC voltage	–0.2	+2.45		1
VCCQ voltage	–0.2	+2.45		1
Flash Output short circuit current	—	100	mA	3
LPSDRAM Output short circuit current	—	50		

Notes:
1. All specified voltages are relative to VSS. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on F-VCC, D-VCC, and F-VPP pins. During transitions, this level may undershoot to –2.5 V for periods < 5 ns which, during transitions, may overshoot to F-V_{CC} + 1.5 V and D-V_{CC} + 1.5 V for periods < 5 ns.
2. Maximum DC voltage on F-VPP may overshoot to +9.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may adversely affect device reliability.

Table 6. Memory Subsystem Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
T_C	Case Operating Temperature	—	–25	+85	°C
F-V_{CC}	Flash Supply Core Voltage	—	1.7	2.0	V
D-V_{CC}	LPSDRAM Supply Core Voltage	—	1.7	1.9	
V_{CCQ}	I/O Supply Voltage option	—	1.71	1.9	
V_{PPL}	Flash Progarmming Voltage Supply (Logic Level)	—	0.9	2.0	
V_{PPH}[1]	Flash Factory Programming (Elevated Voltage)	—	8.5	9.5	
t_{PPH}	Maximum Hours at Elevated Voltage	F-V_{PP} = V_{PPH}	—	80	Hours
Flash Block Erase Cycles	Flash Main and Parameter Blocks	F-V_{PP} = F-V_{CC}	100,000	—	Cycles
	Flash Main Blocks	F-V_{PP} = V_{PPH}	—	1000	
	Flash Parameter Blocks	F-V_{PP} =V_{PPH}	—	2500	

Note: F-V_{PP} program voltage is normally V_{PPL}. Maximum F-V_{PP} can be F-V_{PPH} ± 0.5 V for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during flash program or erase.

Electrical Specifications 6

Note: The PXA27x processor memory subsystem device power is the sum of all active and non-active die currents.

6.1 Flash DC Current Characteristics

The flash DC current characteristics shown in Table 7 are for the individual flash die within the PXA27x processor memory subsystem device.

Table 7. Flash DC Current Characteristics (Sheet 1 of 2)

Sym	Parameter	Typ	Max	Unit	Test Conditions		Notes
I_{LI}	Input Load Current	–	±1	µA	F-V_{CC} = F-$V_{CC\ MAX}$ V_{CCQ} = $V_{CCQ\ MAX}$ V_{IN} = V_{CCQ} or V_{SS}		1
I_{LO}	Output Leakage Current	–	±1	µA	F-V_{CC} = F-$V_{CC\ MAX}$ V_{CCQ} = $V_{CCQ\ MAX}$ V_{IN} = V_{IH} or V_{IL}		1
I_{CCS}	Standby	50	110	µA	F-V_{CC} = F-$V_{CC\ MAX}$ V_{CCQ} = $V_{CCQ\ MAX}$ F-CE# = V_{IH} F-RST# = V_{IH} F-WP# = V_{IH}		1,2
I_{CCAPS}	Automatic Power Saving (APS)	50	110	µA	F-V_{CC} = F-$V_{CC\ MAX}$ V_{CCQ} = $V_{CCQ\ MAX}$ F-CE# = V_{IH} F-RST# = V_{IH}		1,2
I_{CCR}	Asynchronous Single-Word • f = 5 MHz (1 F-CLK)	13	15	mA	1-Word Read	F-V_{CC} = F-$V_{CC\ MAX}$ F-CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1
	Page-Mode Read • f = 13 MHz (5 F-CLK)	8	9	mA	4-Word Read		1
I_{CCR}	Synchronous Burst Read • f = 52 MHz, LC = 4	18	22	mA	Burst length = 8	F-V_{CC} = F-$V_{CC\ MAX}$ F-CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1
		21	25	mA	Burst length = 16		
I_{CCW}, I_{CCE}	• F-VPP Program Current, • F-VPP Erase Current	35	50	mA	F-V_{PP} = V_{PPL}, program/erase in progress		1,3,4,7
		25	32	mA	F-V_{PP} = V_{PPH}, program/erase in progress		1,3,5,7
I_{CCWS}, I_{CCES}	• F-VPP Program Suspend Current, • F-VPP Erase Suspend Current	50	110	µA	F-CE# = V_{IL}, suspend in progress		1,6,3
I_{PPS}, I_{PPWS}, I_{PPES}	F-VPP Standby Current, F-VPP Program Suspend Current, F-VPP Erase Suspend Current	0.2	5	µA	F-V_{PP} = F-V_{PPL}, suspend in progress		1,3
I_{PPR}	F-VPP Read	2	15	µA	F-V_{PP} ≤ F-V_{CC}		1,3

Table 7. Flash DC Current Characteristics (Sheet 2 of 2)

Sym	Parameter	Typ	Max	Unit	Test Conditions	Notes
I_{PPW}	F-VPP Program Current	0.05	0.10	mA	F-V_{PP} = V_{PPL}, program in progress	1,3
		8	22		F-V_{PP} = V_{PPH}, program in progress	1,3
I_{PPE}	F-VPP Erase Current	0.05	0.10	mA	F-V_{PP} = V_{PPL}, erase in progress	1,3
		8	22		F-V_{PP} = V_{PPH}, erase in progress	1,3

NOTES:
1. All currents are RMS unless noted. Typical values are at typical F-VCC and T_C = +25 °C.
2. I_{CCS} is the average current measured over any 5 ms time interval 5 µs after F-CE# is deasserted.
3. Sampled, not 100% tested.
4. Flash read + program current is the sum of I_{CCR} + I_{CCW} currents.
5. Flash read + erase current is the sum of I_{CCR} + I_{CCE} currents.
6. I_{CCES} is specified with the flash deselected. If the flash is read-while-erase suspend, the flash current is I_{CCES} + I_{CCR}.
7. I_{CCW}, I_{CCE} are measured over typical or Max times specified in Section 7.4, “Flash Program and Erase Characteristics” on page 51.

6.2 Flash DC Voltage Characteristics

Table 8. Flash DC Voltage Characteristics

Sym	Parameter	Min	Max	Unit	Test Condition	Notes
V_{IL}	Input Low Voltage	0	0.4	V		1
V_{IH}	Input High Voltage	V_{CCQ} – 0.4	V_{CCQ}	V		
V_{OL}	Output Low Voltage	—	0.1	V	F-V_{CC} = F-$V_{CC\ MIN}$ V_{CCQ} = $V_{CCQ\ MIN}$ I_{OH} = 100 µA	
V_{OH}	Output High Voltage	V_{CCQ} – 0.1	—	V		
V_{PPLK}	F-V_{PP} Lock-Out Voltage	—	0.4	V		2
V_{LKO}	F-V_{CC} Lock Voltage	1.0	—	V		
V_{LKOQ}	V_{CCQ} Lock Voltage	0.9	—	V		

Notes:
1. V_{IL} can undershoot to –0.4 V and V_{IH} can overshoot to V_{CCQ} + 0.4 V for durations of ≤ 20 ns.
2. F-V_{PP} ≤ V_{PPLK} inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.

6.3 LPSDRAM DC Characteristics

NOTICE: DC Characteristics of *all die* in the PXA27x processor memory subsystem need to be considered accordingly, depending on the device operation.

Table 9. LPSDRAM DC Characteristics (Sheet 1 of 2)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit	Notes
D-V_{CC}	Voltage Range		1.7	—	1.9	V	—
I_{CC1} (One Bank Active)	Operating Current at min cycle time Burst Length = 1	I_{IO} = 0 mA $t_{CK} \geq t_{CK\_MIN}$	—	—	75	mA	—
I_{CC2P}	Precharge Standby Current: Power-Down Mode (All banks idle)	D-CKE = L, D-CS# = H $t_{CK} \geq t_{CK\_MIN}$	—	—	700	µA	—
I_{CC2N}	Precharge Standby Current: Non-Power-Down Mode (All banks idle)	D-CKE = H, D-CS# = H $t_{CK} \geq t_{CK\_MIN}$	—	—	15	mA	—
I_{CC3P}	Active Standby Current in Power-Down Mode (All banks active)	D-CKE = L, $t_{CK} \geq t_{CK\_MIN}$	—	—	5	mA	—
I_{CC3N}	Active Standby Current: Non-Power-Down Mode (All banks active)	D-CKE = H, $t_{CK} \geq t_{CK\_MIN}$	—	—	25	mA	3
I_{CC4} (4 Banks active)	Operating Current Page Burst Mode	I_{IO} = 0 mA $t_{CK} \geq t_{CK\_MIN}$	—	—	80	mA	—
I_{CC5}	Auto Refresh Current	$t_{RC} > t_{RC\_MIN}$	—	—	150	mA	2
I_{CC6}	Self Refresh Current	Address & Data toggling at min cycle time	—	—	600	µA	4
I_{CC7}	Deep Power-Down Current	Address & Data toggling at min cycle time	—	—	10	µA	—
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CCQ} – 0.15	—	–	V	—
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CCQmin}	–0.1	—	0.2	V	—
V_{IH}	Input High Voltage	—	V_{CCQ} – 0.3	—	V_{CCQ} + 0.2	V	—

Table 9. LPSDRAM DC Characteristics (Sheet 2 of 2)

V_{IL}	Input Low Voltage	—	-0.2	—	0.3	V	
I_{IL}	Input Leakage Current	–0.2 V < V_{IN} < V_{CCQ} + 0.2 V	–1.5	—	+1.5	µA	1

Notes:
1. Input leakage currents include High-Z output leakage for bi-directional buffers with tri-state outputs.
2. Input signals are toggled at max frequency to simulate PXA27x processor memory subsystem operating condition, where another device may be active.
3. No accesses in progress.
4. See below Table 10, “LPSDRAM Self Refresh Current”.

Table 10. LPSDRAM Self Refresh Current

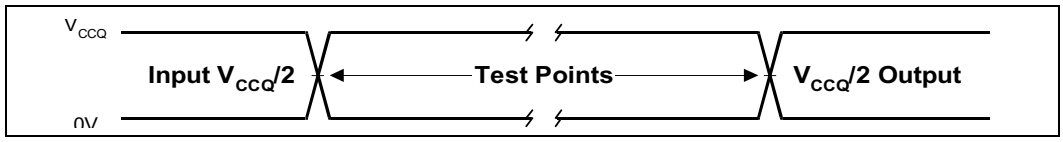
Parameter	Description	Test Condition	Set Temperature	# of Banks			Unit
				All Banks Refreshed	Bank 0 & 1 Refreshed	Bank 0 Refreshed	
I_{CC6}	Self Refresh Current (All Banks Refreshed)	D-CKE < 0.2 V t_{CK} = Infinity	85 °C max	600	450	315	µA
			70 °C max	525	375	295	
			45 °C max	450	300	270	
			15 °C max	375	250	250	

Note: Other than I_{CC6} for all Banks at 85°C, the Self Refresh currents are verified during device characterization and not 100% tested.

AC Characteristics 7

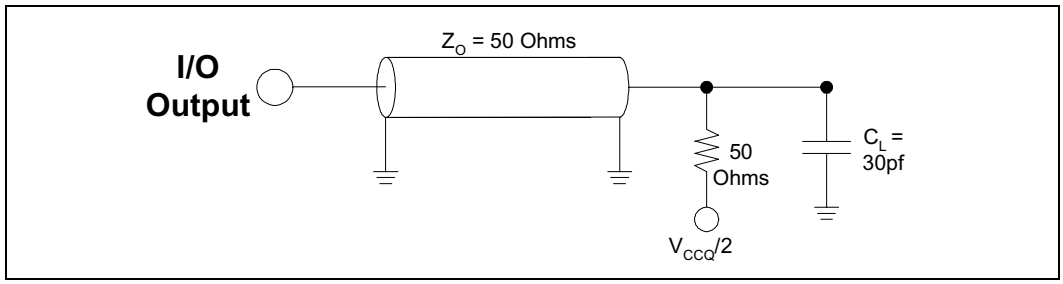
7.1 AC Test Conditions

Figure 10. Intel® PXA27x Processor Memory Subsystem AC Input/Output Reference Waveform



NOTE: AC test inputs are driven at V_{IH} for Logic "1" and V_{IL} for Logic "0." Input/output timing begins and ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed occurs at F-V_{CC} = F-$V_{CC\ MIN}$.

Figure 11. Intel® PXA27x Processor Memory Subsystem Transient Equivalent Testing Load Circuit



Notes:
1. Test configuration component value for worst case speed conditions.
2. C_L includes jig capacitance.

7.2 Flash AC Read Specifications

Table 11. Flash AC Read Specifications (Sheet 1 of 2)

Number	Symbol	parameter	V_{CC} Range	MIN	MAX	Units	Notes
Asynchronous Specifications							
R1	t_{AVAV}	Read cycle time	F-V_{CC} = 1.8 V to 2.0 V	85	—	ns	1
			F-V_{CC} = 1.7 V to 2.0 V	88	—	ns	
R2	t_{AVQV}	Address to output valid	F-V_{CC} = 1.8 V to 2.0 V	—	85	ns	
			F-V_{CC} = 1.7 V to 2.0 V	—	88	ns	
R3	t_{ELQV}	F-CE# low to output valid	F-V_{CC} = 1.8 V to 2.0 V	—	85	ns	
			F-V_{CC} = 1.7 V to 2.0 V	—	88	ns	
R4	t_{GLQV}	OE# low to output valid	—	—	20	ns	1,2
R5	t_{PHQV}	F-RST# high to output valid	—	—	150	ns	1
R6	t_{ELQX}	F-CE# low to output in low-Z	—	0	—	ns	1,3
R7	t_{GLQX}	OE# low to output in low-Z	—	0	—	ns	1,2,3
R8	t_{EHQZ}	F-CE# high to output in high-Z	—	—	17	ns	1,3
R9	t_{GHQZ}	OE# high to output in high-Z	—	—	17	ns	
R10	t_{OH}	Output hold from first occurring address, F-CE#, or OE# change	—	0	—	ns	
R11	t_{EHEL}	F-CE# pulse width high	—	14	—	ns	1
Latching Specifications							
R101	t_{AVVH}	Address setup to ADV# high	—	7	—	ns	1
R102	t_{ELVH}	F-CE# low to ADV# high	—	10	—	ns	
R103	t_{VLQV}	ADV# low to output valid	F-V_{CC} = 1.8 V to 2.0 V	—	85	ns	
			F-V_{CC} = 1.7 V to 2.0 V	—	88	ns	
R104	t_{VLVH}	ADV# pulse width low	—	7	—	ns	
R105	t_{VHVL}	ADV# pulse width high	—	7	—	ns	
R106	t_{VHAX}	Address hold from ADV# high	—	7	—	ns	1,4
R108	t_{APA}	Page address access	—	—	25	ns	1
R111	t_{PHVH}	F-RST# high to ADV# high	—	30	—	ns	1
Clock Specifications							
R200	$f_{F\text{-}CLK}$	F-CLK frequency	—	—	52	MHz	1,3
R201	$t_{F\text{-}CLK}$	F-CLK period	—	19.2	—	ns	
R202	$t_{CH/CL}$	F-CLK high and low time	—	3.5	—	ns	
R203	$t_{F\text{-}CLK}$	F-CLK fall and rise time	—	—	3	ns	
Synchronous Specifications							
R301	t_{AVCH}/t_{AVCL}	Address setup to F-CLK	—	7	—	ns	1
R302	t_{VLCH}/t_{VLCL}	ADV# low setup to F-CLK	—	7	—	ns	
R303	t_{ELCH}/t_{ELCL}	F-CE# low setup to F-CLK	—	7	—	ns	

Table 11. Flash AC Read Specifications (Sheet 2 of 2)

Number	Symbol	parameter	V_{CC} Range	MIN	MAX	Units	Notes
R304	t_{CHQV}/t_{CLQV}	F-CLK to output valid	—	–	14	ns	
R305	t_{CHQX}	Output hold from F-CLK	—	3	—	ns	1,5
R306	t_{CHAX}	Address hold from F-CLK	—	7	—	ns	1,4,5
R311	t_{CHVL}	F-CLK Valid to ADV# Setup	—	0	—	ns	1

NOTES:
1. See Figure 10, "PXA27x Processor Memory Subsystem AC Input/Output Reference Waveform" on page 41 for timing measurements and max allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after F-CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
5. Applies only to subsequent synchronous reads.

Figure 12. Flash Asynchronous Single-Word Read with ADV# Low

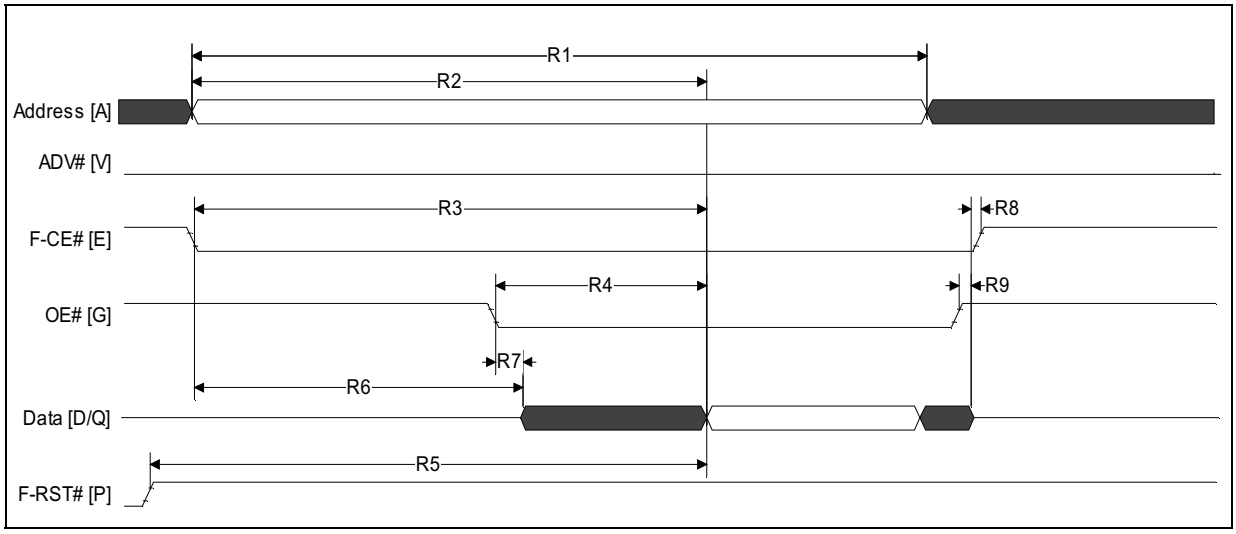
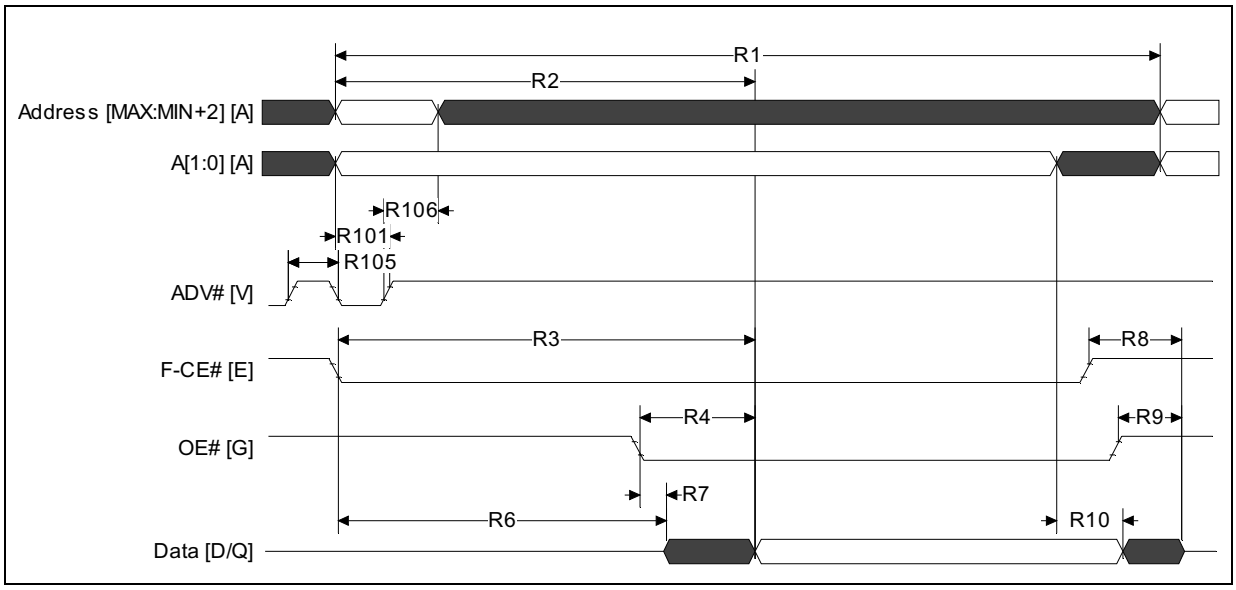


Figure 13. Flash Asynchronous Single-Word Read with ADV# Latch



NOTE: A[1:0] must be held constant.

Figure 14. Flash Asynchronous Page-Mode Read Timing

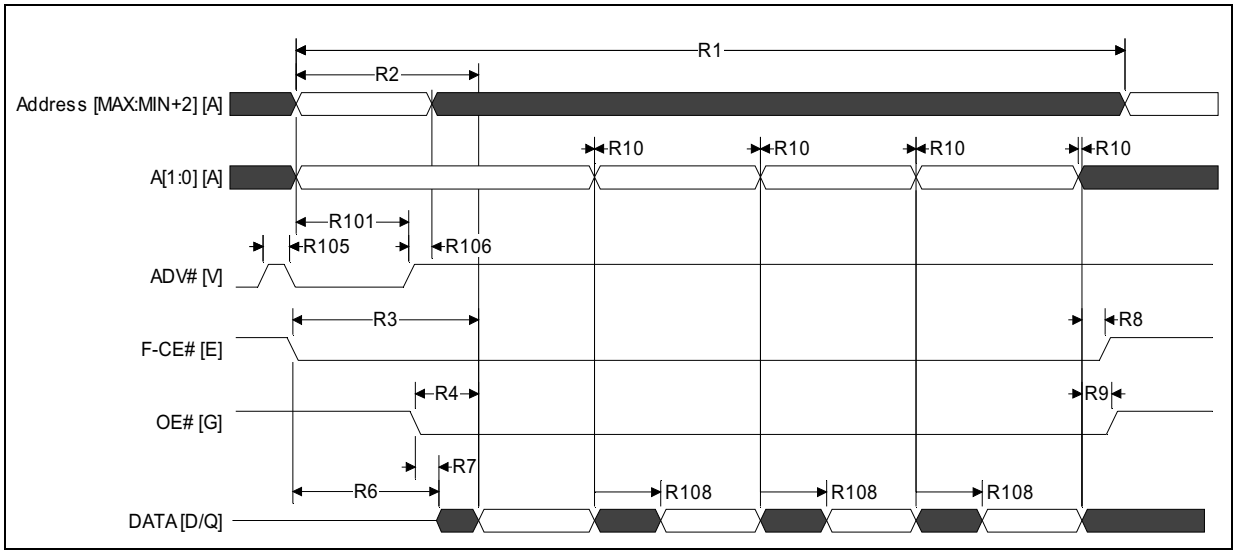
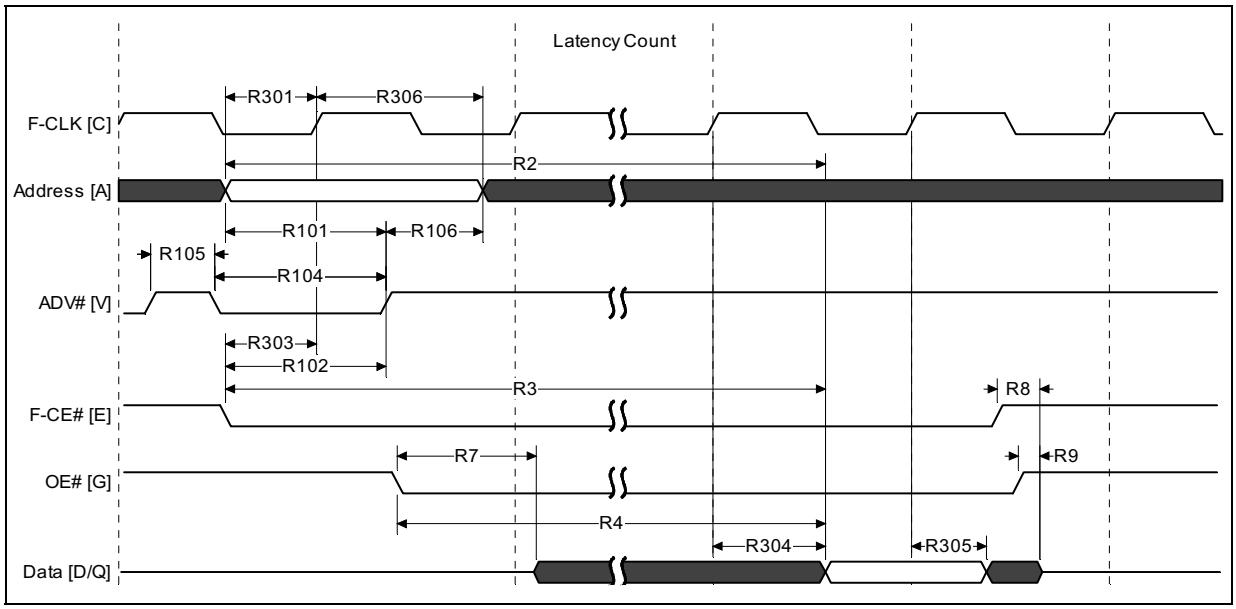


Figure 15. Flash Synchronous Single-Word Array or Non-array Read Timing



Note: This diagram illustrates the case where an n-word burst is initiated to the flash memory array and it is terminated by F-CE# deassertion after the first word in the burst.

Figure 16. Flash Synchronous Burst-Mode Eight-Word Read Timing

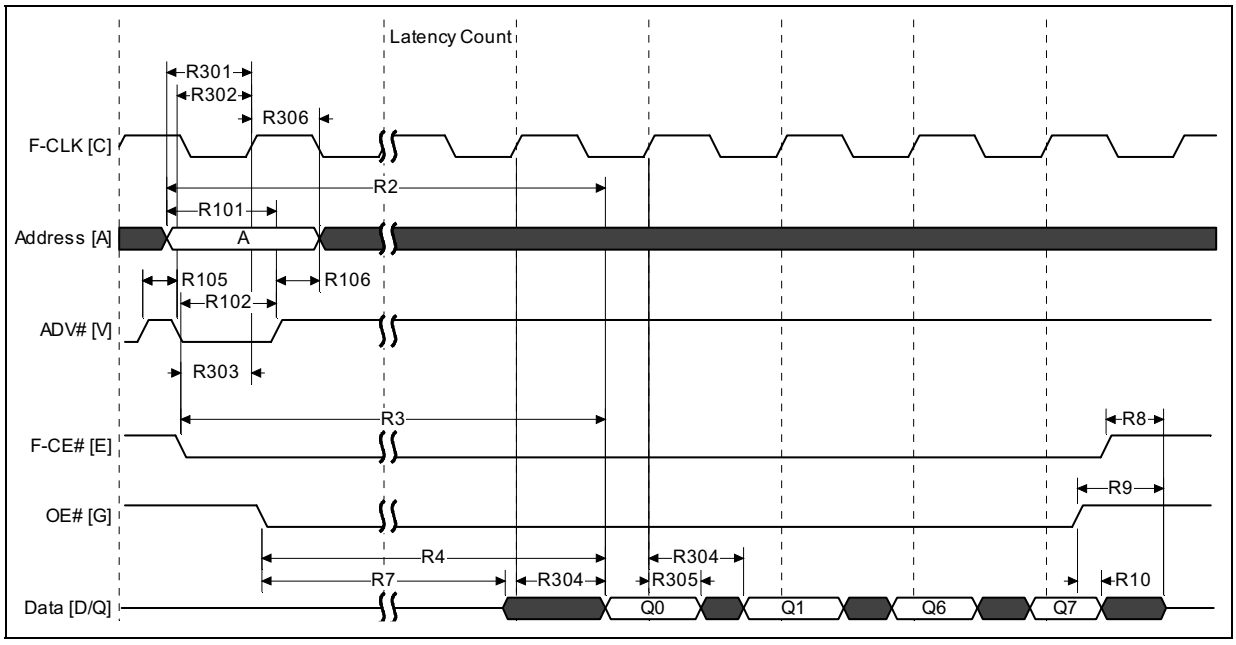
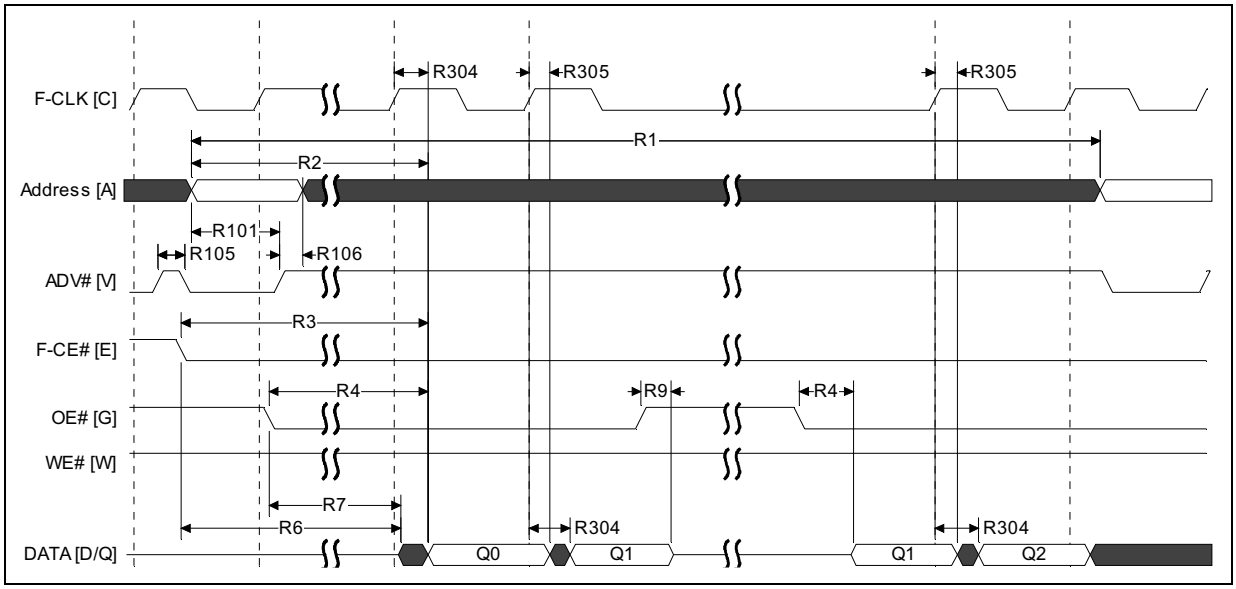


Figure 17. Flash Burst Suspend Timing



Note: F-CLK can be stopped in either high or low state.

7.3 Flash AC Write Specifications

Table 12. Intel® PXA27x Flash AC Write Specifications

Number	Symbol	Parameter	MIN	MAX	Unit	Notes
W1	t_{PHWL}	F-RST# high recovery to WE# low	150	—	ns	1,2,3
W2	t_{ELWL}	F-CE# setup to WE# low	0	—	ns	1,2,3
W3	t_{WLWH}	WE# write pulse width low	50	—	ns	1,2,4
W4	t_{DVWH}	Data setup to WE# high	50	—	ns	1,2
W5	t_{AVWH}	Address setup to WE# high	50	—	ns	1,2
W6	t_{WHEH}	F-CE# hold from WE# high	0	—	ns	1,2
W7	t_{WHDX}	Data hold from WE# high	0	—	ns	1,2
W8	t_{WHAX}	Address hold from WE# high	0	—	ns	1,2
W9	t_{WHWL}	WE# pulse width high	20	—	ns	1,2,5
W10	t_{VPWH}	F-VPP setup to WE# high	200	—	ns	1,2,3,7
W11	t_{QVVL}	F-VPP hold from Status read	0	—	ns	
W12	t_{QVBL}	F-WP# hold from Status read	0	—	ns	1,2,3,7
W13	t_{BHWH}	F-WP# setup to WE# high	200	—	ns	
W14	t_{WHGL}	WE# high to OE# low	0	—	ns	1,2,9
W16	t_{WHQV}	WE# high to read valid	t_{AVQV} + 35	—	ns	1,2,3,6,10
Write to Asynchronous Read Specifications						
W18	t_{WHAV}	WE# high to Address valid	0	—	ns	1,2,3,6
Write to Synchronous Read Specifications						
W19	$t_{WHCH/L}$	WE# high to Flash Clock valid	19	—	ns	1,2,3,6,10
W20	t_{WHVH}	WE# high to ADV# high	19	—	ns	
Write Specifications with Clock Active						
W21	t_{VHWL}	ADV# high to WE# low	—	20	ns	1,2,3,11
W22	t_{CHWL}	Flash Clock high to WE# low	—	20	ns	

NOTES:
1. Write timing characteristics during erase suspend are the same as write-only operations.
2. A write operation can be terminated with either F-CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from F-CE# or WE# low (whichever occurs last) to F-CE# or WE# high (whichever occurs first).
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from F-CE# or WE# high (whichever occurs first) to F-CE# or WE# low (whichever occurs last).
6. t_{WHVH} or $t_{WHCH/L}$ must be met when transitioning from a write cycle to a synchronous burst read.
7. F-VPP and F-WP# should be at a valid level until erase or program success is determined.
8. This specification is only applicable when transitioning from a write cycle to an asynchronous read. See spec W19 and W20 for synchronous read.
9. When doing a Read Status operation following any command that alters the Status Register, W14 is 20 ns.
10. Add 10 ns if the write operations results in a RCR or block lock status change, for the subsequent read operation to reflect this change.
11. These specs are required only when the device is in a synchronous mode and clock is active during address setup phase.

Figure 18. Flash Write to Flash Write Timing

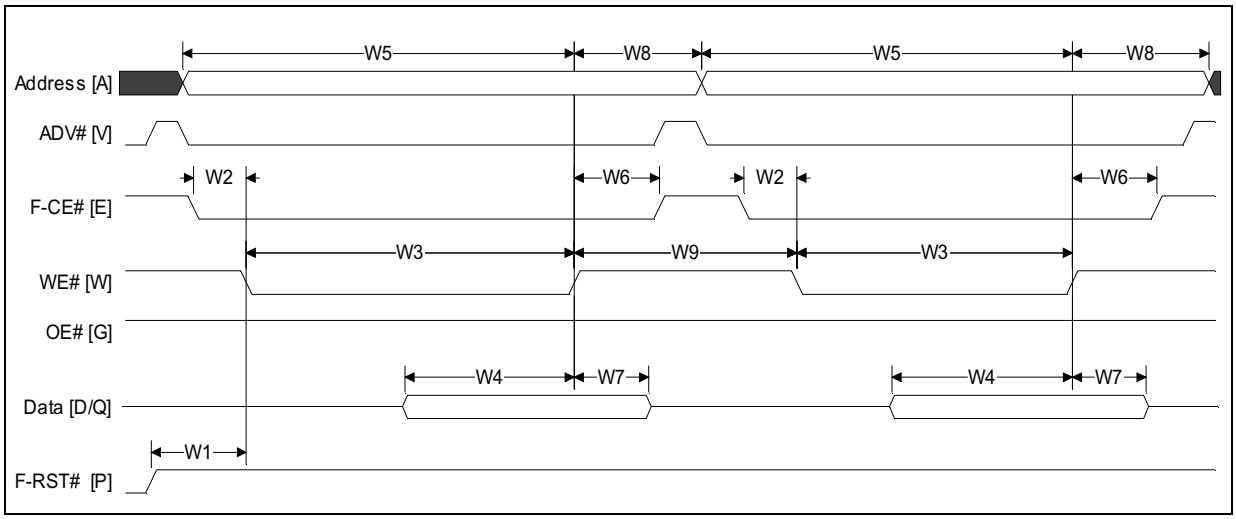


Figure 19. Flash Asynchronous Read to Flash Write Timing

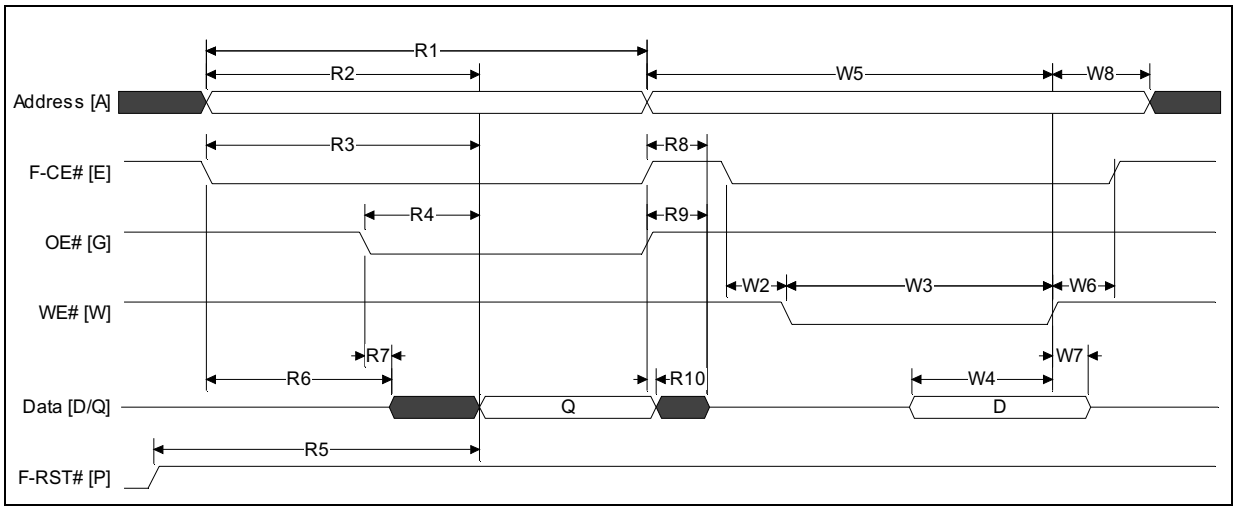


Figure 20. Flash Write to Flash Asynchronous Read Timing

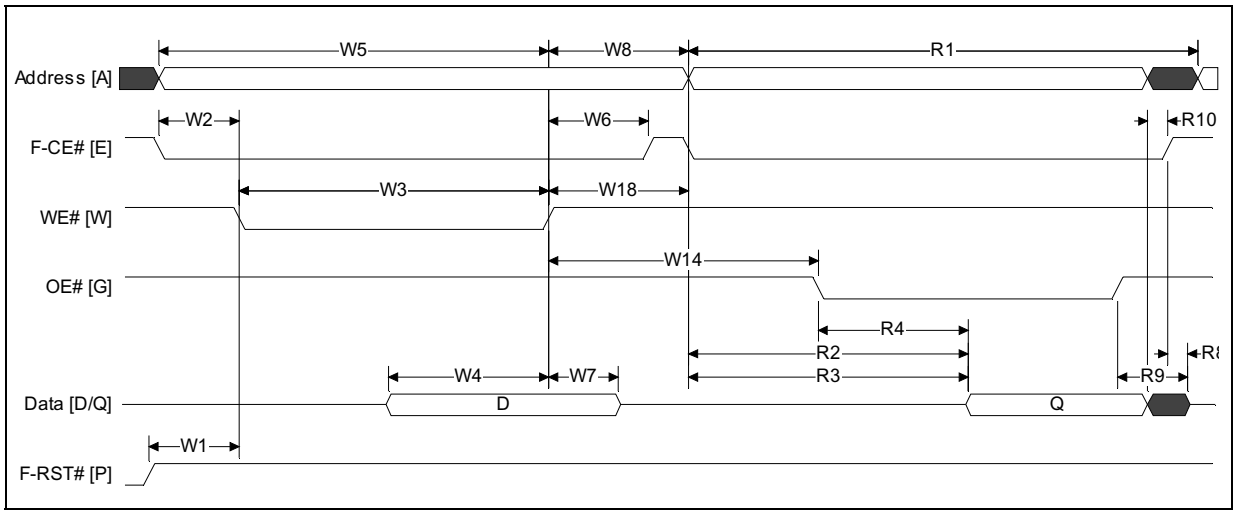


Figure 21. Flash Synchronous Read to Flash Write Timing

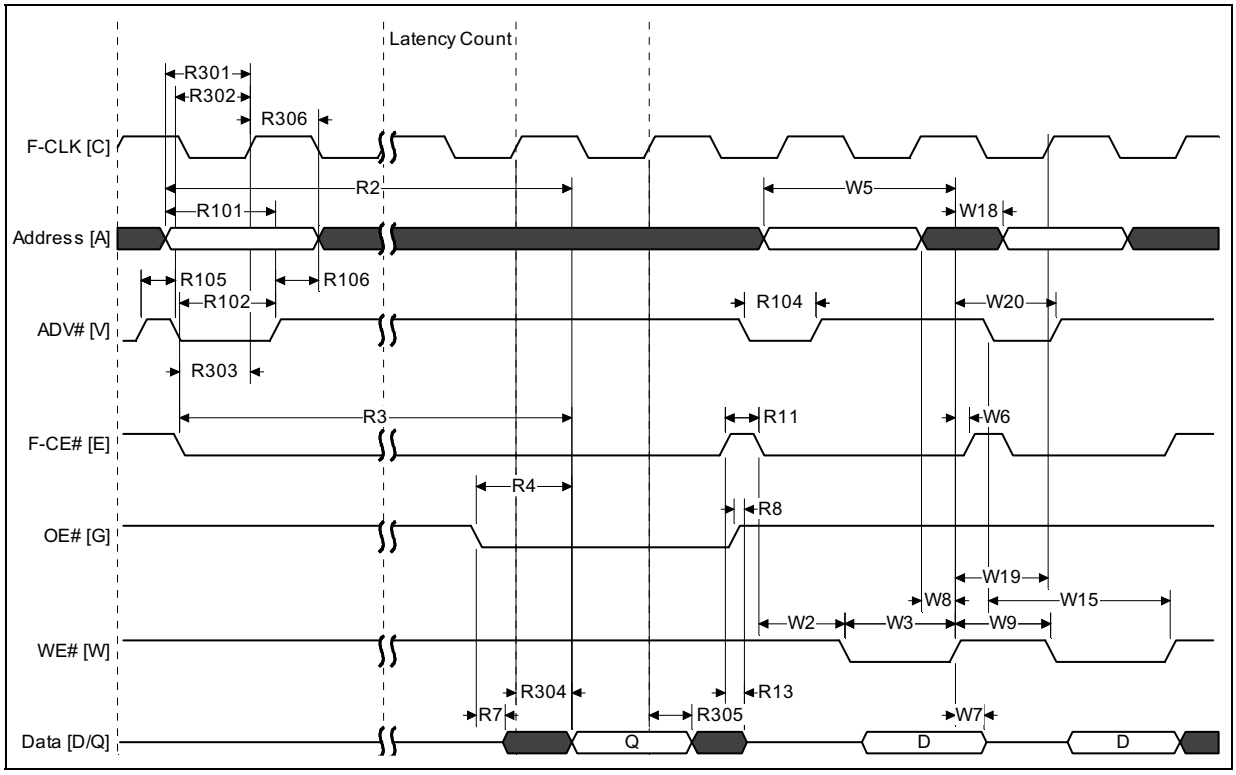
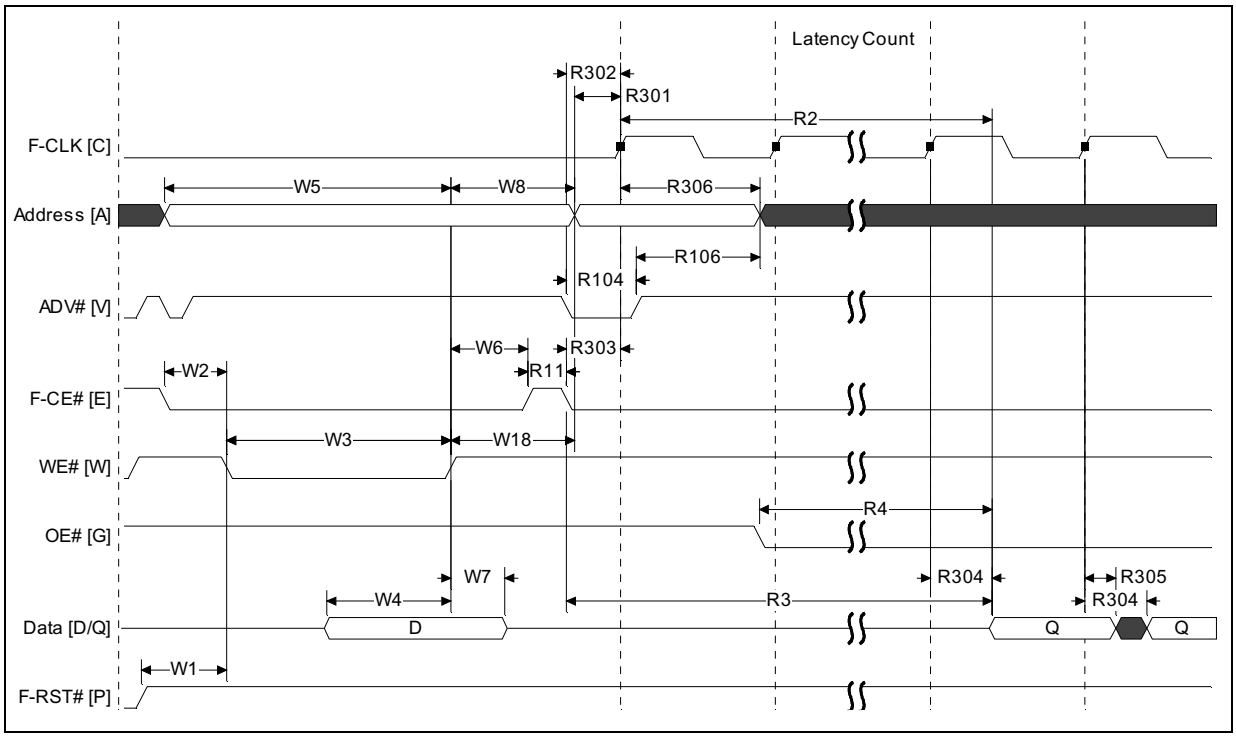


Figure 22. Flash Write to Flash Synchronous Read Timing



7.4 Flash Program and Erase Characteristics

Table 13. Intel® PXA27x Flash Program and Erase Characteristics

Number.	Symbol	Parameter		V_{PPL}			V_{PPH}			Units	Notes
				MIN	TYP	MAX	MIN	TYP	MAX		
Conventional Word Programming											
W200	$t_{PROG/W}$	Program Time	Single Word	—	90	180	—	85	170	µs	1
			Single Cell	—	30	60	—	30	60		1
Buffered Programming											
W200	$t_{PROG/Word}$	Program Time	Single Word	—	90	180	—	85	170	µs	1
W201	$t_{PROG/Buffer}$		One Buffer (32-words)	—	440	880	—	340	680		1
Buffered Enhanced Factory Programming											
W451	$t_{BEFP/Word}$	Program	Single Word	N/A	N/A	N/A	N/A	10	N/A	µs	1,2
W452	$t_{BEFP/Setup}$		Buffered EFP Setup	N/A	N/A	N/A	5	N/A	N/A		1
Erasing and Suspending											
W500	$t_{ERS/Buffer}$	Erase Time	16-KWord Parameter	—	0.4	2.5	—	0.4	2.5	µs	1
W501	$t_{ERS/Main\ Block}$		64-KWord Main	—	1.2	4	—	1.0	4		1
W600	$t_{SUSP/Prog\ Susp}$	Suspend Latency	Program Suspend	—	20	25	—	20	25	µs	1
W601	$t_{SUSP/Erase\ Susp}$		Erase Suspend	—	20	25	—	20	25		1

Notes:
1. Typical values measured at TC = +25 °C and nominal voltages. Excludes system overhead. Sampled, but not 100% tested.
2. Averaged programming time over entire flash arrays.

7.5 LPSDRAM Die Capacitance

Table 14. LPSDRAM Capacitance

Symbol	Parameter	MAX	Unit	Condition
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0 V

NOTE: Sampled, not 100% tested. T_C = 25 °C, f = 1 MHz.

7.6 LPSDRAM AC Characteristics

Table 15. 256-Mbit LPSDRAM AC Characteristics—Read-Only Operations

Symbol	Parameter	Test Condition	Min	Max	Unit	Notes
t_{RC}	Clock Cycle Time	CL = 3 R-CLK = 104 MHz	9.5	—	ns	1,2
t_{CKH}	Clock High Level Pulse Width		3	—	ns	1,2
t_{CKL}	Clock Low Level Pulse Width		3	—	ns	1,2
t_{T}	Transition Time		0.5	1.0	ns	1,2
t_{CKEH}	D-CKE Hold Time		1	—	ns	1,2
t_{CKES}	D-CKE Setup Time		2	—	ns	1,2
t_{AH}	Address Hold Time		1	—	ns	1,2
t_{AS}	Address Setup Time		2	—	ns	1,2
t_{IH}	Data Input Hold Time		1	—	ns	1,2
t_{IS}	Data Input Setup Time		2	—	ns	1,2
t_{CMH}	D-CS#, D-RAS#, D-CAS#, WE#, D-DM Hold Time		1	—	ns	1,2
t_{CMS}	D-CS#, D-RAS#, D-CAS#, WE#, D-DM Setup Time		2	—	ns	1,2
t_{AC}	Clock to valid output delay (positive edge of clock)	CL = 3	–	7	ns	1,2
t_{OH}	Data Out Hold Time		2.5	—	ns	1,2
t_{LZ}	Clock to Output in Low-Z		1	—	ns	1,2
t_{HZ}	Clock to Output in High-Z	CL = 3	—	7	ns	1,2
t_{RAS}	Row Active time (Active to Precharge command)		60	100K	ns	1,2
t_{RC}	Row Cycle time (Active to Active command on same bank)		90	—	ns	1,2
t_{RCD}	Row to column delay (Active to Read/Write)		28.5	—	ns	1,2
t_{RP}	Row Precharge Time		28.5	—	ns	1,2
t_{REF}	Refresh Period (4096 rows)		—	64	ms	1,2
t_{RFC}	Auto Refresh Period		110	—	ns	1,2
t_{SREX}	Self Refresh Exit Time (Self refresh to Active)		120	—	ns	1,2

Notes:
1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when normal output driver strength is used. See Table 35, “LPSDRAM Configurable Output Driver Strength” on page 100.

Table 16. 256-Mbit LPSDRAM AC Characteristics—Write Operations[1,2]

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{WR}	Write Recovery Time		20	—	ns
t_{RRD}	Active bank a to Active Bank b command		20	—	ns
t_{DAL}	Last data input to Active Delay		$t_{WR} + t_{RP}$	—	ns
t_{CDL}	Last data input to New Read/Write command		1	—	t_{CK}
t_{BDL}	Last data input to Burst Terminate command		1	—	t_{CK}
t_{CCD}	Read/Write command to Read/Write command		1	—	t_{CK}
t_{DQW}	D-DM write mask latency		0	—	t_{CK}
t_{DQZ}	D-DM data out mask latency		2	—	t_{CK}
t_{MRD}	Load Mode Register command to Active/Refresh command		2	—	t_{CK}
t_{WR}	Write Recovery Time	$t_{WR} / t_{CK} < 1$	1	—	t_{CK}
		$1 < t_{WR} / t_{CK} < 2$	2	—	
t_{PHZ}	Data out to High Z from Precharge command	CL = 3	3	—	t_{CK}
t_{INI}	Initialization Delay		200	—	µs

Notes:
1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when normal output driver strength is used. See Table 35, “LPSDRAM Configurable Output Driver Strength” on page 100.

Power and Reset Specifications 8

8.1 Flash Power-Up and Power-Down

Power supply sequencing is not required if F-VCC, VCCQ, and F-VPP are connected together. If VCCQ and/or F-VPP are not connected to the F-VCC supply, then F-V_{CC} should reach F-$V_{CC\ MIN}$ before applying V_{CCQ} and F-V_{PP}. Device inputs should not be driven before supply voltage equals F-$V_{CC\ MIN}$.

Power supply transitions should only occur when F-RST# is low. This protects the device from accidental programming or erasure during power transitions.

8.2 Flash Output Disable

When OE# is deasserted, the flash outputs DQ[MAX:0] are disabled and placed in Hign-Z.

8.3 Flash Standby

When F-CE# is deasserted the flash is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, independent of the level placed on OE#. Standby current, I_{CCS}, is the average current measured over any 5 ms time interval, 5 µs after F-CE# is deasserted.

When the flash is deselected (while F-CE# is deasserted) during a program or erase operation, it continues to consume active power until the program or erase operation is completed.

8.4 Flash Reset

When the PXA27x processor reset occurs with no flash memory reset, improper processor initialization may occur because the flash memory may be providing status information rather than array data. F-RST# should be controlled by the same low-true reset signal that resets the PXA27x processor.

After initial power-up or reset, the flash defaults to asynchronous Read Array, and the Status Register is set to 0x80. A minimum delay is required before an initial read access or a write cycle can be initiated. After this wake-up interval passes, normal operation is restored. See Table 17 and Figure 23 on page 56 for details about the flash reset timing.

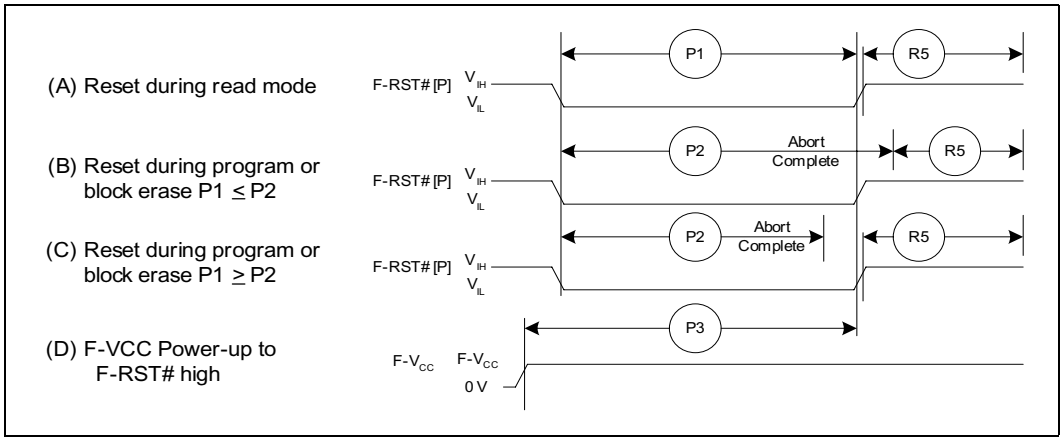
Note: If F-RST# is asserted during a program or erase operation, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data may have been only partially written or erased.

Table 17. Flash Reset Timing

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	F-RST# pulse width low	100	—	ns	1,2,3,5
P2	t_{PLRH}	F-RST# low to device reset during erase	—	25	µs	3,4,5
		F-RST# low to device reset during program	—	25		3,4,5
P3	t_{VCCPH}	F-V_{CC} Power valid to F-RST# de-assertion (high)	60	—		1,3,5

NOTES:
1. The device may reset if t_{PLPH} is < t_{PLPH} MIN, but this is not guaranteed.
2. If F-RST# is tied to the F-V_{CC} supply, the flash will not be ready until t_{VCCPH} and after F-V_{CC} ≥ F-$V_{CC\ MIN}$.
3. If F-RST# is tied to any pin or signal with V_{CCQ} voltage levels, the F-RST# input voltage must not exceed F-V_{CC} until F-V_{CC} ≥ F-$V_{CC\ MIN}$.
4. Reset completes within t_{PLPH} if F-RST# is asserted while no erase or program operation is executing.
5. Sampled, but not 100% tested.

Figure 23. Flash Reset Operation Waveforms



8.5 Flash Power Supply Decoupling

Flash memory device require careful power supply decoupling. Three basic power supply current considerations are require: 1) Standby current levels, 2) Active current levels, and 3) Transient peaks produced when F-CE# and OE# are asserted and deasserted.

When the flash is accessed, many internal conditions change. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and correct decoupling capacitor selection suppress transient voltage peaks. Because Intel StrataFlash® memory draws its power from F-VCC, F-VPP, and VCCQ, therefore each power connection should have a 0.1 µF ceramic capacitor connected to a corresponding ground connection (e.g.,VCCQ to VSS). High-frequency, inherently low-inductance capacitors should be placed as close as possible to package leads.

It is recommended, for every eight devices used in the system, a 4.7 µF electrolytic capacitor should be placed between power and ground close to the devices. The bulk capacitor is meant to overcome voltage droop caused by PCB trace inductance.

8.6 Flash Automatic Power Saving

Automatic Power Saving (APS) provides low power operation during a read's active state. During APS, I_{CCAPS} average current is measured over any 5 ms time interval, 5 µs after F-CE# is deasserted. APS, the same time interval 5 µs after the following events:

1. There is no internal read, program, or erase operations.
2. F-CE# is asserted.
3. The address lines are quiescent and at VSS or VCCQ. OE# may also be driven during APS.

8.7 LPSDRAM Power-up Sequence and Initialization

The LPSDRAM must be powered up and initialized in a predefined manner. Once power is applied to D-VCC and VCCQ simultaneously, and the clock is stable, the LPSDRAM requires a t_{INI} delay prior to issuing any command other than the NOP command. The NOP command should be applied at least once during the t_{INI} delay. After the t_{INI} delay, a Precharge command should be applied to precharge all banks. This must be followed by two back to back Auto Refresh cycles. After the Auto Refresh cycles are complete, the Mode registers must be programmed. The Mode Register will power up in an unknown state. The Mode Register and the Extended Mode Register should be loaded prior to issuing any operational commands.

Part 2: Flash Device Operations

Device Operations Overview 9

9.1 Flash and LPSDRAM Bus Operations

Bus operations for the PXA27x processor memory subsystem device involve the control of flash and LPSDRAM inputs. The bus operations are shown from Table 18 to Table 20. Fully synchronous operations are performed by the flash or LPSDRAM to latch the commands at the positive edges of F-CLK or R-CLK respectively

Table 18. Flash + LPSDRAM Bus Operations (Sheet 1 of 2)

Device	Mode	F-RST#	F-CE#	OE#	ADV#	F-VPP	WE#	D-CKE$_{n-1}$	D-CKE$_n$	D-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
Flash Die	Sync Read	H	L	L	L	X	H	LPSDRAM outputs must be in High-Z									Flash DQ$_{OUT}$	1,2,3,4, 15
	Async Read	H	L	L	L	X	H										Flash DQ$_{OUT}$	1,2,3,4, 15
	Write	H	L	H	L	V_{PPL}/ V_{PPH}	L										Flash DQ$_{IN}$	1,2,4,15
	Output Disable	H	L	H	X	X	H	Any LPSDRAM mode is allowed									Flash High-Z	4,15
	Standby	H	H	X	X	X	X										Flash High-Z	4,15
	Reset	L	X	X	X	X	X										Flash High-Z	4,15
LPSDRAM Die	Active	Flash outputs must be in High-Z					H	H	X	L	L	H	X	V	Row Address		LPSDRAM DQ$_{OUT}$	5,6,7
	Read						H	H	X	L	H	L	V	V	L	Col Addr	LPSDRAM DQ$_{OUT}$	5,6,7,13
	With Auto Precharge														H			
	Write						L	H	X	L	H	L	V	V	L	X	LPSDRAM DQ$_{IN}$	5,6,8
	With Auto Precharge														H			
	Burst Stop						L	H	H	L	H	H	X	X	X	X	LPSDRAM High-Z	9
	Precharge One Bank						L	H	X	L	L	H	X	V	L	X	LPSDRAM High-Z	6
	All Banks													X	H			
	Auto Refresh	Flash outputs must be in High-Z					H	H	H	L	L	L	X	X	X	X	LPSDRAM High-Z	6, 12
	Self Refresh Entry	Flash must be in High-Z					H	H	L	L	L	L	X	X	X	X	LPSDRAM High-Z	6
	Self Refresh Exit	Any flash mode is allowed					H	L	H	L	H	H	X	X	X	X	LPSDRAM High-Z	6
							X			H	X	X						

Table 18. Flash + LPSDRAM Bus Operations (Sheet 2 of 2)

Device	Mode	F-RST#	F-CE#	OE#	ADV#	F-VPP	WE#	D-CKE$_{n-1}$	D-CKE$_n$	D-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
LPSDRAM Die	Load Mode Register	Flash outputs must be in High-Z					L	H	X	L	L	L	X	Operand Code			LPSDRAM High-Z	6, 10,11
	Input/ Output Enable						X	H	X				L	X			LPSDRAM High-Z	6, 9
	Input Inhibit/ Output High-Z	Any flash mode is allowed					X	H	X				H	X			LPSDRAM High-Z	6, 9
	Clock Suspend Entry	Any flash mode is allowed					X	H	L	H	X	X	X	X	X	X	LPSDRAM High-Z	6, 13
							V			L	V	V						
	Clock Suspend Exit	Flash outputs must be in High-Z					X	L	H	X	X	X	X	X	X	X	LPSDRAM High-Z	6,13
	Power Down Entry	Any flash mode allowed					X	H	L	H	X	X	X	X	X	X	LPSDRAM High-Z	6, 14
		Flash outputs must be in High-Z					H			L	H	H						
	Power Down Exit	Any flash mode is allowed					X	L	H	H	X	X	X	X	X	X	LPSDRAM High-Z	6,14
							H			L	H	H						
	Deep Power Down Entry	Flash outputs must be in High-Z					L	H	L	L	H	H	X	X	X	X	LPSDRAM High-Z	6,14
	Deep Power Down Exit						X	L	H	X	X	X	X	X	X	X	LPSDRAM High-Z	6,14
	Device Deselect (NOP)	Any flash mode is allowed					X	H	X	H	X	X	X	X	X	X	LPSDRAM High-Z	6
	No Operation (NOP)	Flash outputs must be in High-Z					H	H	X	L	H	H	X	X	X	X	LPSDRAM High-Z	6

Notes:
1. OE# and WE# should never be asserted simultaneously.
2. X can be V_{IL} or V_{IH} for inputs.
3. Flash CFI query and status register accesses use DQ[7:0] only, all other reads use DQ[15:0].
4. All states and sequences not shown are illegal or reserved.
5. V = Valid.
6. A[13:1] provide row address for LPSDRAM. A[9:1] provide column address for LPSDRAM.
7. Select bank and column address, and start Read. A11 High enables auto precharge.
8. Select bank and column address, and start Write. A11 High enables auto precharge.
9. Activate or deactivate the data during Writes with zero-clock delay and during Reads with two-clock delay. D-DM0 corresponds to DQ[7:0], D-DM1 corresponds to DQ[15:8].
10. A[11:1] define the DRAM operand code to the register
11. Extended mode register is programmed by setting D-BA1 = H and D-BA0 = L. For Mode register programming, set D-BA1 = D-BA0 = L
12. All banks must be precharged before issuing an Auto-refresh command.
13. Clock suspend mode occurs when Column access or burst is in progress
14. Power-Down occurs when no accesses are in progress.
15. For x32 Flash only stacked combination, the bus operations are equivalent to x16 flash die bus operations.

Table 19. LPSDRAM Functional Mode Description: Current State bank *n*, Command to Bank *n*

Current State	D-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	No Operation	Continue previous Operation	1,2
	L	H	H	H	No Operation	Continue previous Operation	1,2
Idle	L	L	H	H	Active	Select and activate row	1,2
	L	L	L	H	Auto refresh	Auto refresh	1,2
	L	L	L	L	Load Mode register	Mode register set	1,2
	L	L	H	L	Precharge	NOP	1,2
Row Active	L	H	L	H	Read	Select Column & start read burst	1,2,4
	L	H	L	L	Write	Select Column & start write burst	1,2,4
	L	L	H	L	Precharge	Deactivate Row in bank (or banks)	1,2,3,4
Read (without Auto precharge)	L	H	L	H	Read	Truncate Read & start new Read burst	1,2,5
	L	H	L	L	Write	Truncate Read & start new Write burst	1,2,5
	L	L	H	L	Prechard	Truncate Read, start Precharge	1,2
	L	H	H	L	Burst Terminate	Burst terminate	1,2
Write (without Auto precharge)	L	H	L	H	Read	Truncate Write & start new Read burst	1,2,5
	L	H	L	L	Write	Truncate Write& start new Write burst	1,2,5
	L	L	H	L	Precharge	Truncate Write, start Precharge	1,2
	L	H	H	L	Burst Terminate	Burst terminate	1,2

Notes:
1. The table applies when both D-CKE$_{n-1}$ and D-CKE$_n$ are high.
2. All states and sequences not shown are illegal or reserved.
3. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
4. A command other than No Operation (NOP), should not be issued to the same bank while a Read or Write Burst with auto precharge is enabled.
5. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

Table 20. LPSDRAM Functional Mode Description: Current State bank *n*, Command to Bank *m*

Current State	D-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	No Operation	Continue previous Operation	1,2
	L	H	H	H	No Operation	Continue previous Operation	1,2
Idle	X	X	X	X	Any	Any command allowed to bank m	1,2
Row Activating, Active, or Precharging	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Read with Auto Precharge disabled	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Write with Auto precharge disabled	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Read with Auto Precharge	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2
Write with Auto precharge	L	L	H	H	Active	Activate Row	1,2
	L	H	L	H	Read	Start Read burst	1,2
	L	H	L	L	Write	Start Write burst	1,2
	L	L	H	L	Precharge	Precharge	1,2

Notes:
1. The table applies when both D-CKE$_{n-1}$ and D-CKE$_n$ are high.
2. All states and sequences not shown are illegal or reserved.

9.2 Flash Bus Operations

F-CE# low and F-RST# high enable device read operations. The flash device internally decodes upper address inputs to determine the accessed partition. ADV# low opens the internal address latches. OE# low activates the outputs and gates selected data onto the I/O bus.

In asynchronous mode, the addresses are latched when ADV# goes high or continuously flows through if ADV# is held low. In synchronous burst-mode, the addresses are latched by the first rising edge of ADV#, or the next valid F-CLK edge with ADV# low (WE# and F-RST# must be high, and F-CE# must be low).

Table 21. Flash Command Bus Cycles

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr[1]	Data[2]	Oper	Addr[1]	Data[2]
Read	Read Array	1	Write	PnA	0xFF	—	—	—
	Read Device Identifier	≥ 2	Write	PnA	0x90	Read	PBA+IA	ID
	CFI Query	≥ 2	Write	PnA	0x98	Read	PnA+QA	QD
	Read Status Register	2	Write	PnA	0x70	Read	PnA	SRD
	Clear Status Register	1	Write	X	0x50	—	—	—
Program	Word Program	2	Write	WA	0x40/ 0x10	Write	WA	WD
	Buffered Program[3]	> 2	Write	WA	0xE8	Write	WA	N - 1
	Buffered Enhanced Factory Program (Buffered EFP)[4]	> 2	Write	WA	0x80	Write	WA	0xD0
Erase	Block Erase	2	Write	BA	0x20	Write	BA	0xD0
Suspend	Program/Erase Suspend	1	Write	X	0xB0	—	—	—
	Program/Erase Resume	1	Write	X	0xD0	—	—	—
Block Locking/ Unlocking	Lock Block	2	Write	BA	0x60	Write	BA	0x01
	Unlock Block	2	Write	BA	0x60	Write	BA	0xD0
	Lock-down Block	2	Write	BA	0x60	Write	BA	0x2F
Protection	Program Protection Register	2	Write	PRA	0xC0	Write	PRA	PD
	Program Lock Register	2	Write	LRA	0xC0	Write	LRA	LRD
Configuration	Program Read Configuration Register	2	Write	RCD	0x60	Write	RCD	0x03

Notes:

1. First command cycle address should be the same as the operation's target address.
   PnA = Address within the partition.
   PBA = Partition base address.
   IA = Identification code address offset.
   QA = CFI Query address offset.
   BA = Address within the block.
   WA = Word address of memory location to be written.
   PRA = Protection Register address.
   LRA = Lock Register address.
   X = Any valid address within the flash.
2. ID = Identifier data.
   QD = Query data on DQ[15:0].
   SRD = Status Register data.
   WD = Word data.
   N = Word count of data to be loaded into the write buffer.
   PD = Protection Register data.
   PD = Protection Register data.
   LRD = Lock Register data.
   RCD = Read Configuration Register data on A[15:0]. A[MAX:16] can select any partition.
3. The second cycle of the Buffered Program Command is the word count of the data to be loaded into the write buffer. This is followed by up to 32-words of data.Then the confirm command (0xD0) is issued, triggering the array programming operation.
4. The confirm command (0xD0) is followed by the buffer data.

9.3 Flash Command Definitions

Table 22. Flash Command Codes and Definitions (Sheet 1 of 2)

Mode	Code	Device Mode	Description
Read	0xFF	Read Array	Places the addressed partition in Read Array mode. Array data is output on DQ[15:0].
	0x70	Read Status Register	Places the addressed partition in Read Status Register mode. The partition enters this mode after a program or erase command is issued. Status Register data is output on DQ[7:0].
	0x90	Read Device ID or Configuration Register	Places the addressed partition in Read Device Identifier mode. Subsequent reads from addresses within the partition outputs manufacturer/device codes, Configuration Register data, Block Lock status, or Protection Register data on DQ[15:0].
	0x98	Read Query	Places the addressed partition in Read Query mode. Subsequent reads from the partition addresses output Common Flash Interface information on DQ[7:0].
	0x50	Clear Status Register	The WSM can only set Status Register error bits. The Clear Status Register command is used to clear the SR error bits.
Write	0x40	Word Program Setup	First cycle of a 2-cycle programming command; prepares the CUI for a write operation. On the next write cycle, the address and data are latched and the WSM executes the programming algorithm at the addressed location. During program operations, the partition responds only to Read Status Register and Program Suspend commands. F-CE# or OE# must be toggled to update the Status Register in asynchronous read. F-CE# or ADV# must be toggled to update the Status Register Data for synchronous Non-array read. The Read Array command must be issued to read array data after programming has finished.
	0x10	Alternate Word Program Setup	Equivalent to the Word Program Setup command, 0x40.
	0xE8	Buffered Program	This command loads a variable number of bytes up to the buffer size of 32-words onto the program buffer.
	0xD0	Buffered Program Confirm	The confirm command is Issued after the data streaming for writing into the buffer is done. This instructs the WSM to perform the Buffered Program algorithm, writing the data from the buffer to the flash memory array.
	0x80	Buffered Enhanced Factory Programming Setup	First cycle of a 2-cycle command; initiates Buffered Enhanced Factory Program mode (Buffered EFP). The CUI then waits for the Buffered EFP Confirm command, 0xD0, that initiates the Buffered EFP algorithm. All other commands are ignored when Buffered EFP mode begins.
	0xD0	Buffered EFP Confirm	If the previous command was Buffered EFP Setup (0x80), the CUI latches the address and data, and prepares the flash for Buffered EFP mode.
Erase	0x20	Block Erase Setup	First cycle of a 2-cycle command; prepares the CUI for a block-erase operation. The WSM performs the erase algorithm on the block addressed by the Erase Confirm command. If the next command is not the Erase Confirm (0xD0) command, the CUI sets Status Register bits SR.4 and SR.5, and places the addressed partition in read status register mode.
	0xD0	Block Erase Confirm	If the first command was Block Erase Setup (0x20), the CUI latches the address and data, and the WSM erases the addressed block. During block-erase operations, the partition responds only to Read Status Register and Erase Suspend commands. F-CE# or OE# must be toggled to update the Status Register in asynchronous read. F-CE# or ADV# must be toggled to update the Status Register Data for synchronous Non-array read.
Suspend	0xB0	Program or Erase Suspend	This command issued to any flash address initiates a suspend of the currently-executing program or block erase operation. The Status Register indicates successful suspend operation by setting either SR.2 (program suspended) or SR.6 (erase suspended), along with SR.7 (ready). The Write State Machine remains in the suspend mode regardless of control signal states (except for F-RST# asserted).
	0xD0	Suspend Resume	This command issued to any flash address resumes the suspended program or block-erase operation.

Table 22. Flash Command Codes and Definitions (Sheet 2 of 2)

Mode	Code	Device Mode	Description
Block Locking/ Unlocking	0x60	Lock Block Setup	First cycle of a 2-cycle command; prepares the CUI for block lock configuration changes. If the next command is not Block Lock (0x01), Block Unlock (0xD0), or Block Lock-Down (0x2F), the CUI sets Status Register bits SR.4 and SR.5, indicating a command sequence error.
	0x01	Lock Block	If the previous command was Block Lock Setup (0x60), the addressed block is locked.
	0xD0	Unlock Block	If the previous command was Block Lock Setup (0x60), the addressed block is unlocked. If the addressed block is in a lock-down state, the operation has no effect.
	0x2F	Lock-Down Block	If the previous command was Block Lock Setup (0x60), the addressed block is locked down.
Protection	0xC0	Program Protection Register Setup	First cycle of a 2-cycle command; prepares the flash for a Protection Register or Lock Register program operation. The second cycle latches the register address and data, and starts the programming algorithm.
Configu-ration	0x60	Read Configuration Register Setup	First cycle of a 2-cycle command; prepares the CUI for flash read configuration. If the Set Read Configuration Register command (0x03) is not the next command, the CUI sets Status Register bits SR.4 and SR.5, indicating a command sequence error.
	0x03	Read Configuration Register	If the previous command was Read Configuration Register Setup (0x60), the CUI latches the address and writes A[15:0] to the Read Configuration Register. Following a Configure Read Configuration Register command, subsequent read operations access array data.

Flash Read Operations 10

The flash supports two read modes: asynchronous page-mode and synchronous burst-mode. Asynchronous page-mode is the default read mode after flash power-up or a reset. The Read Configuration Register must be configured to enable synchronous burst reads of the flash memory array (see Section 10.3, "Flash Read Configuration Register" on page 70).

To perform a read operation, F-RST# and WE# must be deasserted while F-CE# and OE# are asserted. F-CE# is the flash-select control. When asserted, it enables the flash memory. OE# is the data-output control. When asserted, the addressed flash memory data is driven onto the I/O bus. See Section 10.3, "Flash Read Configuration Register" on page 70 for details on the available read modes, and Section 15, "Special Flash Read States" on page 93 for details regarding the available read states.

The Automatic Power Savings (APS) feature provides low power operation following reads during active mode. After data is read from the memory array and the address lines are quiescent, APS automatically places the flash into standby. In APS, flash current is reduced to I_{CCAPS} (see Section 6.1, "Flash DC Current Characteristics" on page 37).

Each partition of the flash can be in any of four read states: Read Array, Read Identifier, Read Status or Read Query. Upon power-up, or after a reset, all partitions of the flash default to Read Array. To change a partition's read state, the appropriate read command must be written to the flash (see Section 9.3, "Flash Command Definitions" on page 66).

10.1 Flash Asynchronous Page-Mode Read

Following a flash power-up or reset, asynchronous page-mode is the default flash read mode and all partitions are set to Read Array. However, to perform array reads after any other flash operation (e.g. write operation), the Read Array command must be issued in order to read from the flash memory array.

Note: Asynchronous page-mode reads can only be performed when Read Configuration Register bit RCR.15 is set (see Section 10.3, "Flash Read Configuration Register" on page 70).

To perform an asynchronous page-mode read, an address is driven onto A[MAX:MIN], and F-CE# and ADV# are asserted. WE# and F-RST# must already have been deasserted. ADV# can be driven high to latch the address, or it must be held low throughout the read cycle. F-CLK is not used for asynchronous page-mode reads, and is ignored. If only asynchronous reads are to be performed, F-CLK should be tied to a valid V_{IH} level, and ADV# must be tied to ground. Flash array data are driven onto DQ[15:0] after an initial access time t_{AVQV} delay. (see Section 7.2, "Flash AC Read Specifications" on page 42).

In asynchronous page-mode, four-data words are "sensed" simultaneously from the flash memory array and loaded into an internal page buffer. The buffer word corresponding to the initial address on A[MAX:MIN] is driven onto DQ[15:0] after the initial access delay. Address bits A[MAX:MIN+2] select the 4-word page. Address bits A[MIN+1:MIN] determine which word of the 4-word page is output from the data buffer at any given time.

Note: AMIN for a 16-bit operations is A1 while a 32-bit operations, AMIN = A2 on the package ballout.

10.2 Flash Synchronous Burst-Mode Read

Read Configuration register bits RCR[15:0] must be set before flash synchronous burst operation can be performed. Synchronous burst mode can be performed for both array and non-array reads such as Read ID, Read Status or Read Query. (See Section 10.3, "Flash Read Configuration Register" on page 70 for details). Synchronous burst-mode outputs 4-, 8-, 16-, or continuous-words. To perform a synchronous burst- read, an initial address is driven onto A[MAX:MIN], and F-CE# and ADV# are asserted. WE# and F-RST# must already have been deasserted. ADV# is asserted, and then deasserted to latch the address. Alternately, ADV# can remain asserted throughout the burst access, in which case the address is latched on the next valid F-CLK edge while ADV# is asserted.

During synchronous array and non-array read modes, the first word is output from the data buffer on the next valid F-CLK edge after the initial access latency delay (see Section 10.3.2, "Flash Latency Count" on page 72). Subsequent data is output on valid F-CLK edges following a minimum delay. However, for a synchronous non-array read, the same word of data will be output on successive clock edges until the burst length requirements are satisfied.

10.2.1 Flash Burst Suspend

The Burst Suspend feature of the flash can reduce or eliminate the initial access latency incurred when system software needs to suspend a burst sequence that is in progress in order to retrieve data from another device on the same system bus. The PXA27x processor can resume the burst sequence later. Burst suspend provides maximum benefit in non-cache systems.

Burst accesses can be suspended during the initial access latency (before data is received) or after the flash has output data. When a burst access is suspended, internal array sensing continues and any previously latched internal data are retained. A burst sequence can be suspended and resumed without limit as long as flash operation conditions are met.

Burst Suspend occurs when F-CE# is asserted, the current address has been latched (either ADV# rising edge or valid F-CLK edge), F-CLK is halted, and OE# is deasserted. F-CLK can be halted when it is at V_{IH} or V_{IL}.

To resume the burst access, OE# is reasserted, and F-CLK is restarted. Subsequent F-CLK edges resume the burst sequence.

10.3 Flash Read Configuration Register

The flash Read Configuration Register (RCR) is used to select the read mode (synchronous or asynchronous), and it defines the synchronous burst characteristics of the flash. To modify RCR settings, use the Configure Read Configuration Register command (see Section 9.2, "Flash Bus Operations" on page 64).

RCR contents can be examined using the Read Device Identifier command, and then reading from <partition base address> + 0x05 offset. See Section 15.2, "Flash Read Device Identifier" on page 95. The RCR is shown in Table 23 on page 71.

Table 23. Flash Read Configuration Register Description

Read Configuration Register (RCR)															
Read Mode	RES	Latency Count			RES	Data Hold	RES	Burst Seq	F-CLK Edge	RES	RES	Burst Wrap	Burst Length		
RM	R	LC[2:0]			R	DH	R	BS	CE	R	R	BW	BL[2:0]		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Name	Description
15	Read Mode (RM)	0 = Synchronous burst-mode read 1 = Asynchronous page-mode read (default)
14	Reserved (R)	Reserved bits should be cleared (0)
13:11	Latency Count (LC[2:0])	010 =Code 2 011 =Code 3 100 =Code 4 101 =Code 5 110 =Code 6 111 =Code 7 (default) • Other bit settings are reserved.
10	Reserved (R)	Default to an active high (1)
9	Data Hold (DH)	0 =Data held for a 1-clock data cycle 1 =Data held for a 2-clock data cycle (default)
8	Reserved (R)	Default to an active high (1)
7	Burst Sequence (BS)	0 =Reserved 1 =Linear (default)
6	Clock Edge (CE)	0 = Falling edge 1 = Rising edge (default)
5:4	Reserved (R)	Reserved bits should be cleared (0)
3	Burst Wrap (BW)	0 =Wrap; Burst accesses wrap within burst length set by BL[2:0] 1 =No Wrap; Burst accesses do not wrap within burst length (default)
2:0	Burst Length (BL[2:0])	001 =Reserved 010 =8-word burst 011 =16-word burst 111 =Reserved (default) • Other bit settings are reserved.

10.3.1 Flash Read Mode

The flash Read Mode (RM) bit selects synchronous burst-mode or asynchronous page-mode operation for the flash. When the RM bit is set, asynchronous page-mode is selected (default). When RM is cleared, synchronous burst-mode is selected.

10.3.2 Flash Latency Count

The Latency Count bits, LC[2:0], tell the flash how many clock cycles must elapse from the rising edge of ADV# (or from the first valid clock edge after ADV# is asserted) until the first data word is to be driven onto DQ[15:0]. The input clock frequency is used to determine this value. Table 24 on page 72 shows the data output latency for the different settings of LC[2:0].

Refer to Table 24, "Flash LC and Frequency Support" on page 72 for Latency Code Settings example.

Figure 24. Flash First-Access Latency Count

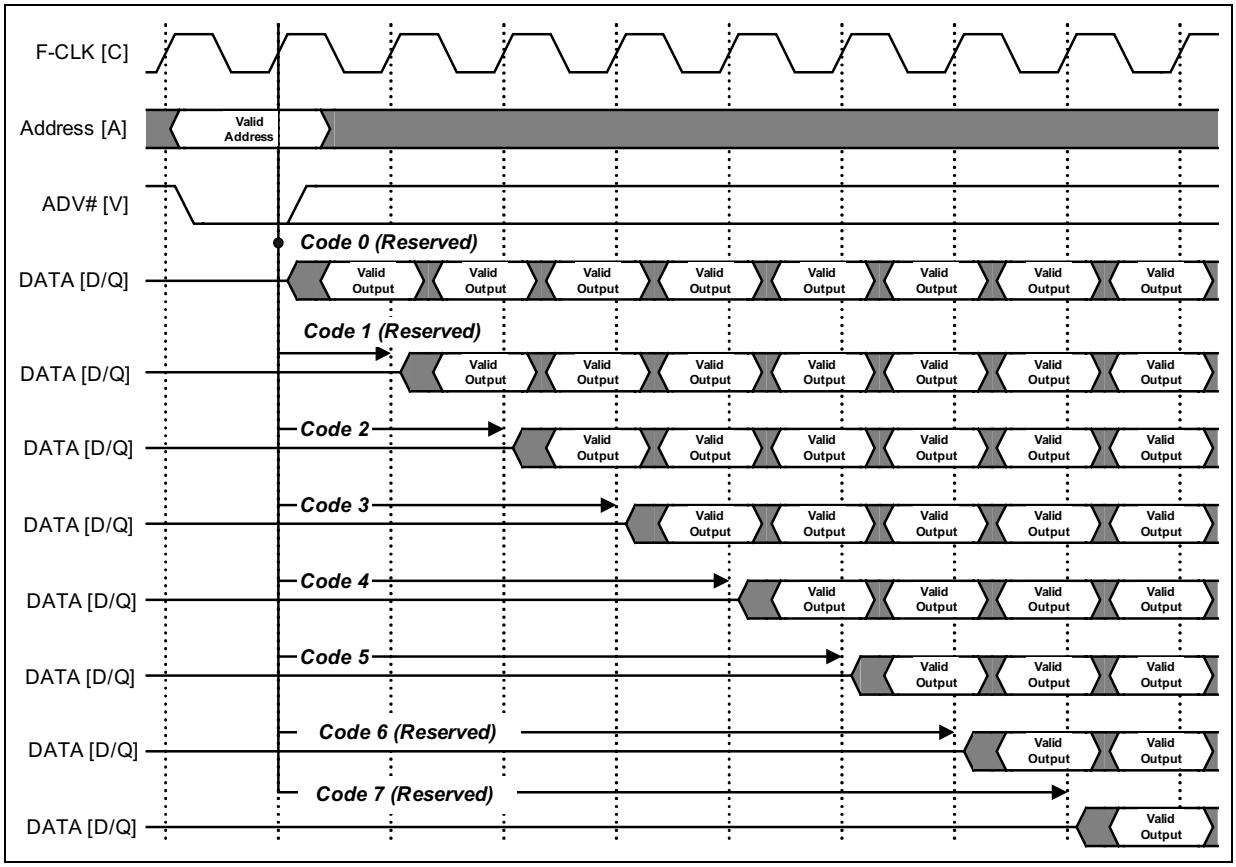
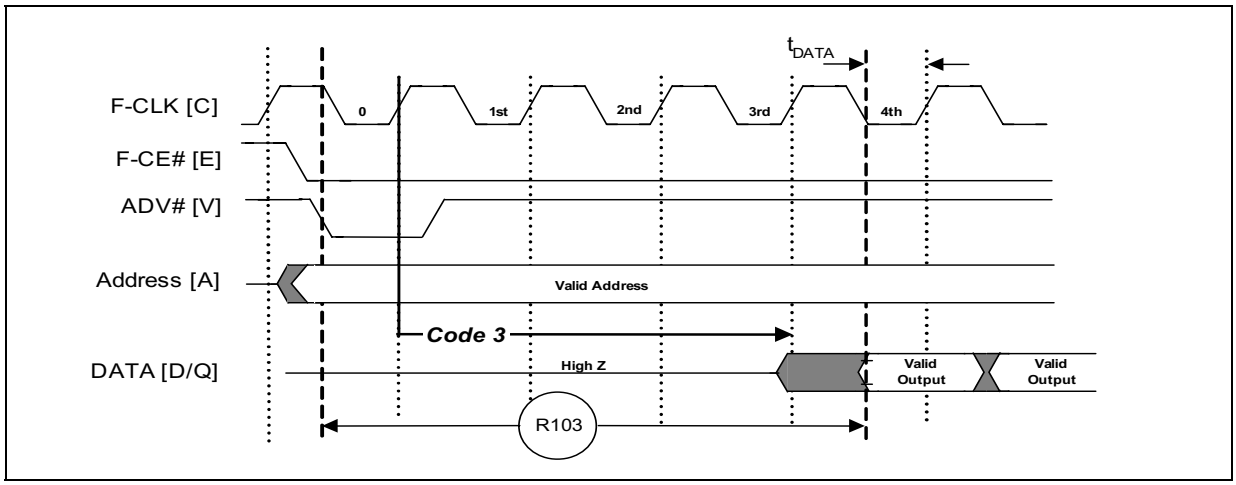


Table 24. Flash LC and Frequency Support

Latency Count Settings	Frequency Support (MHz)
2	≤ 28
3	≤ 40
4 or 5	≤ 52
NOTE: LC is based on t_{AVQV} = 85 ns and t_{CHQV} = 14 ns.	

Figure 25. Example of Flash Latency Count Setting



10.3.3 Flash Burst Sequence

The Burst Sequence (BS) bit selects linear-burst sequence (default). Only linear-burst sequence is supported. Table 25 shows the synchronous burst sequence for all burst lengths supported by PXA27x processor.

Table 25. Flash Burst Sequence Word Ordering

Start Addr. (DEC)	Burst Wrap (RCR.3)	Burst Addressing Sequence (DEC)	
		8-Word Burst (BL[2:0] = 0x010)	16-Word Burst (BL[2:0] = 0x011)
0	0	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15
1	0	1-2-3-4-5-6-7-0	1-2-3-4-5…15-0
2	0	2-3-4-5-6-7-0-1	2-3-4-5-6…15-0-1
3	0	3-4-5-6-7-0-1-2	3-4-5-6-7…15-0-1-2
4	0	4-5-6-7-0-1-2-3	4-5-6-7-8…15-0-1-2-3
5	0	5-6-7-0-1-2-3-4	5-6-7-8-9…15-0-1-2-3-4
6	0	6-7-0-1-2-3-4-5	6-7-8-9-10…15-0-1-2-3-4-5
7	0	7-0-1-2-3-4-5-6	7-8-9-10…15-0-1-2-3-4-5-6
⋮	⋮	⋮	⋮
14	0		14-15-0-1-2…12-13
15	0		15-0-1-2-3…13-14
⋮	⋮	⋮	⋮
0	1	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15
1	1	1-2-3-4-5-6-7-8	1-2-3-4-5…15-16
2	1	2-3-4-5-6-7-8-9	2-3-4-5-6…16-17
3	1	3-4-5-6-7-8-9-10	3-4-5-6-7…17-18
4	1	4-5-6-7-8-9-10-11	4-5-6-7-8…18-19
5	1	5-6-7-8-9-10-11-12	5-6-7-8-9…19-20
6	1	6-7-8-9-10-11-12-13	6-7-8-9-10…20-21
7	1	7-8-9-10-11-12-13-14	7-8-9-10-11…21-22
⋮	⋮	⋮	⋮
14	1		14-15-16-17-18…28-29
15	1		15-16-17-18-19…29-30

10.3.4 Flash Clock Edge

The Clock Edge (CE) bit selects either a rising (default) or falling clock edge for F-CLK. This clock edge is used at the start of a burst cycle, to output synchronous data, and to assert/deassert WAIT.

10.3.5 Flash Burst Wrap

The Burst Wrap (BW) bit determines whether 8-word, or 16-word burst length accesses wrap within the selected word-length boundaries or cross word-length boundaries. When BW is set, burst wrapping does not occur (default). When BW is cleared, burst wrapping occurs.

10.3.6 Flash Burst Length

The Burst Length bit (BL[2:0]) selects the linear burst length for all synchronous burst reads of the flash memory array. The burst lengths are 8-word and 16-word.

Flash Programming Operations 11

The flash supports three programming methods: Single-word programming (0x40/0x10), Buffered Programming (0xE8, 0xD0), and Buffered Enhanced Factory Programming (Buffered EFP) (0x80, 0xD0). See Section 9.3, "Flash Command Definitions" on page 66 for details on the various programming commands issued to the flash.

To perform a write operation, both F-CE# and WE# are asserted while F-RST# and OE# are deasserted. During a write operation, address and data are latched on the rising edge of WE# or F-CE#, whichever occurs first. Table 21, "Flash Command Bus Cycles" on page 65 shows the bus cycle sequence for each of the supported flash commands, while Table 22, "Flash Command Codes and Definitions" on page 66 describes each command. See Section 7.3, "Flash AC Write Specifications" on page 47 for signal-timing details.

Warning: Write operations with invalid F-V_{CC} and/or F-V_{PP} voltages can produce spurious results and should not be attempted.

Successful programming requires the addressed block to be unlocked. If the block is locked down, F-WP# must be deasserted and the block must be unlocked before attempting to program the block. Attempting to program a locked block causes a program error (SR.4 and SR.1 are set) and termination of the operation. See Section 13, "Flash Security Modes" on page 83 for details on locking and unlocking blocks.

11.1 Flash Word Programming

Word programming operations are initiated by writing the Word Program Setup command to the flash (see Section 9.2, "Flash Bus Operations" on page 64). This is followed by a second write to the flash with the address and data to be programmed. The partition accessed during both write cycles outputs Status Register data when read. The partition accessed during the second cycle (the data cycle) of the program command sequence is the location where the data is written. See Figure 52, "Flash Word Program Flowchart" on page 113.

Programming can occur in only one partition at a time; all other partitions must be in a read state or in erase suspend. F-V_{PP} must be above V_{PPLK}, and within the specified V_{PPL} value.

During programming, the flash Write State Machine (WSM) executes a sequence of internally-timed events that program the desired data bits at the addressed location, and verifies that the bits are sufficiently programmed. Programming the flash memory array changes "ones" to "zeros." Flash array bits that are zeros can be changed to ones only by erasing the block. See Section 12, "Flash Erase Operations" on page 81.

The flash Status Register can be examined for programming progress and errors by reading any address within the partition that is being programmed. The partition remains in the Read Status Register state until another command is written to that partition. Issuing the Read Status Register command to another partition address sets that partition to the Read Status Register state, allowing programming progress to be monitored at that partition's address.

Status Register bit SR.7 indicates the programming status while the sequence executes. Commands that can be issued to the programming partition during programming are Program Suspend, Read Status Register, Read Device Identifier, CFI Query, and Read Array (this returns unknown data).

When programming has finished, SR.4 (when set) indicates a programming failure. If SR.3 is set, the WSM could not perform the word programming operation because F-VPP was outside of its acceptable limits. If SR.1 is set, the word programming operation attempted to program a locked block, causing the operation to abort.

Before issuing a new command, the Status Register contents should be examined and then cleared using the Clear Status Register command. Any valid command can follow, when word programming has completed.

11.1.1 Flash Factory Word Programming

Factory word programming is similar to word programming in that it uses the same commands and programming algorithms. However, factory word programming enhances the programming performance with $F\text{-}V_{PP} = V_{PPH}$. This can enable faster programming times during factory manufacturing processes. Factory word programming is not intended for extended use. See Section 5.2, "Operating Conditions" on page 36 for limitations when $F\text{-}V_{PP} = V_{PPH}$.

Note: When $F\text{-}V_{PP} = V_{PPL}$, the flash draws programming current from the F-VCC supply. If F-VPP is driven by a logic signal, V_{PPL} must remain above $V_{PPL\ MIN}$ to program the flash. When $F\text{-}V_{PP} = V_{PPH}$, the flash draws programming current from the F-VPP supply. Figure 26, "Example F-VPP Supply Connections" on page 80 shows examples of flash power supply configurations.

11.2 Flash Buffered Programming

The flash features a 32-word buffer to enable optimum programming performance. For Buffered Programming, data is first written to an on-chip write buffer. Then the buffer data is programmed into the flash memory array in buffer-size increments. This can improve system programming performance significantly over non-buffered programming.

When the Buffered Programming Setup command is issued. See Section 9.3, "Flash Command Definitions" on page 66, Status Register information is updated and reflects the availability of the write buffer. SR.7 indicates buffer availability: if set, the buffer is available; if cleared, the write buffer is not available. To retry, issue the Buffered Programming Setup command again, and re-check SR.7. When SR.7 is set, the buffer is ready for loading. See Figure 54, "Flash Buffer Program Flowchart" on page 115.

On the next write, a word count is written to the flash at the buffer address. This tells the flash how many data words will be written to the buffer, up to the maximum size of the buffer.

On the next write, a flash start address is given along with the first data to be written to the flash memory array. Subsequent writes provide additional flash addresses and data. All data addresses must lie within the start address plus the word count. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 32-word boundary (A[4:0] = 0x00). Crossing a 32-word boundary during programming will result in doubling the total programming time due to refilling the buffer region.

After the last data is written to the buffer, the Buffered Programming Confirm command must be issued to the original block address. The WSM begins to program buffer contents to the flash memory array. If a command other than the Buffered Programming Confirm command is written to the flash, a command sequence error occurs and SR[7,5,4] are set. If an error occurs while writing to the array, the flash stops programming, and SR[7,4] are set, indicating a programming failure.

Reading from another partition is allowed while data is being programmed into the array from the write buffer. See Section 14, “Flash Dual-Operation Considerations” on page 89.

When Buffered Programming has completed, additional buffer writes can be initiated by issuing another Buffered Programming Setup command and repeating the buffered program sequence. Buffered programming may be performed with F-V_{PP} = V_{PPL} or F-V_{PP} = V_{PPH}. See Section 5.2, “Operating Conditions” on page 36 for limitations when operating the flash with F-V_{PP} = V_{PPH}.

If an attempt is made to program past an erase-block boundary using the Buffered Program command, the flash aborts the operation. This generates a command sequence error, and SR[5,4] are set.

If Buffered programming is attempted while F-V_{PP} ≤ V_{PPLK}, SR[4,3] are set. If any errors are detected that have set Status Register bits, the Status Register should be cleared using the Clear Status Register command.

11.3 Flash Buffered Enhanced Factory Programming

Buffered Enhanced Factory Programing (Buffered EFP) is design to speed up flash programming for today's beat-rate-sensitive manufacturing environments. The enhanced programming algorithm used in Buffered EFP eliminates traditional programming elements that drive up overhead in flash programmer systems.

Buffered EFP consists of three phases: Setup, Program/Verify, and Exit. See Figure 55, “Flash Buffered EFP Flowchart” on page 116. It uses a write buffer to spread MLC program performance across 32-words. Verification occurs in the same phase as programming to accurately program the flash memory cell to the correct bit state.

A single two-cycle command sequence programs the entire block of data. This enhancement eliminates three write cycles per buffer: two commands and the word count for each set of 32-words. Host programmer bus cycles fill the flash write buffer followed by a status check. SR.0 indicates when data from the buffer has been programmed into sequential flash memory array locations.

Following the buffer-to-flash array programming sequence, the Write State Machine (WSM) increments internal addressing to automatically select the next 32-word array boundary. This aspect of Buffered EFP saves host programming equipment the address-bus setup overhead.

With adequate continuity testing, programming equipment can rely on the WSM’s internal verification to ensure that the flash has programmed properly. This eliminates the external post-program verification and its associated overhead.

11.3.1 Flash Buffered EFP Requirements and Considerations

Buffered EFP requirements:

- Case temperature: T_C = 25 °C, ±5 °C
- F-V_{CC} within specified operating range.
- F-V_{PP} driven to V_{PPH}.
- Target block unlocked before issuing the Buffered EFP Setup and Confirm commands.
- The first-word address (WA0) for the block to be programmed must be held constant from the setup phase through all data streaming into the target block, until transition to the exit phase is desired.
- WA0 must align with the start of an array buffer boundary[1].

Buffered EFP considerations:

- For optimum performance, cycling must be limited below 100 erase cycles per block[2].
- Buffered EFP programs one block at a time; all buffer data must fall within a single block[3].
- Buffered EFP cannot be suspended.
- Programming to the flash memory array can occur only when the buffer is full[4].
- Read operation while performing Buffered EFP is not supported.

Notes:
1. Word buffer boundaries in the array are determined by A[4:0] (0x00 through 0x1F). The alignment start point is A[4:0] = 0x00.
2. Some degradation in performance may occur if this limit is exceeded, but the flash will continue to work properly.
3. If the internal address counter increments beyond the block's maximum address, addressing wraps around to the beginning of the block.
4. If the number of words is less than 32, remaining locations must be filled with 0xFFFF.

11.3.2 Flash Buffered EFP Setup Phase

After receiving the Buffered EFP Setup and Confirm command sequence, SR.7 (Ready) is cleared, indicating that the WSM is busy with Buffered EFP algorithm startup. A delay before checking SR.7 is required to allow the WSM enough time to perform all of its setups and checks (Block-Lock status, F-V_{PP} level, etc.). If an error is detected, SR.4 is set and Buffered EFP operation terminates. If the block was found to be locked, SR.1 is also set. SR.3 is set if the error occurred due to an incorrect F-V_{PP} level.

Note: Reading from the flash after the Buffered EFP Setup and Confirm command sequence outputs Status Register data. Do not issue the Read Status Register command; it will be interpreted as data to be loaded into the buffer.

11.3.3 Flash Buffered EFP Program/Verify Phase

After the Buffered EFP Setup Phase has completed, the host programming system must check SR[7,0] to determine the availability of the write buffer for data streaming. SR.7 cleared indicates the flash is busy and the Buffered EFP program/verify phase is activated. SR.0 indicates the write buffer is available.

Two basic sequences repeat in this phase: loading of the write buffer, followed by buffer data programming to the array. For Buffered EFP, the count value for buffer loading is always the maximum buffer size of 32-words. During the buffer-loading sequence, data is stored to sequential buffer locations starting at address 0x00. Programming of the buffer contents to the flash memory array starts as soon as the buffer is full. If the number of words is less than 32, the remaining buffer locations must be filled with 0xFFFF.

Caution: The buffer must be completely filled for programming to occur. Supplying an address outside of the current block's range during a buffer-fill sequence causes the algorithm to exit immediately. Any data previously loaded into the buffer during the fill cycle is not programmed into the array.

The starting address for data entry must be buffer size aligned, if not the Buffered EFP algorithm will be aborted and the program fail (SR.4) flag will be set.

Data words from the write buffer are directed to sequential memory locations in the flash memory array; programming continues from where the previous buffer sequence ended. The host programming system must poll SR.0 to determine when the buffer program sequence completes. SR.0 cleared indicates that all buffer data has been transferred to the flash array; SR.0 set indicates that the buffer is not available yet for the next fill cycle. The host system may check full status for errors at any time, but it is only necessary on a block basis after Buffered EFP exit. After the buffer fill cycle, no write cycles should be issued to the flash until SR.0 = 0 and the flash is ready for the next buffer fill.

Note: Any spurious writes are ignored after a buffer fill operation and when internal program is proceeding.

The host programming system continues the Buffered EFP algorithm by providing the next group of data words to be written to the buffer. Alternatively, it can terminate this phase by changing the block address to one outside of the current block’s range.

The Program/Verify phase concludes when the programmer writes to a different block address; data supplied must be 0xFFFF. Upon Program/Verify phase completion, the flash enters the Buffered EFP Exit phase.

11.3.4 Flash Buffered EFP Exit Phase

When SR.7 is set, the flash has returned to normal operating conditions. A full status check should be performed on the partition being programmed at this time to ensure the entire block programmed successfully. When exiting the Buffered EFP algorithm with a block address change, the read mode of both the programmed and the addressed partition will not change. After Buffered EFP exit, any valid command can be issued to the flash.

11.4 Flash Program Suspend

Issuing the Program Suspend command while programming suspends the programming operation. This allows data to be accessed from memory locations other than the one being programmed. The Program Suspend command can be issued to any flash address; the corresponding partition is not affected. A program operation can be suspended to perform reads only. Additionally, a program operation that is running during an erase suspend can be suspended to perform a read operation. See Figure 53, “Flash Program Suspend/Resume Flowchart” on page 114.

When a programming operation is executing, issuing the Program Suspend command requests the WSM to suspend the programming algorithm at predetermined points. The partition that is suspended continues to output SRD after the Program Suspend command is issued. Programming is suspended when SR[7,2] are set. Suspend latency is specified in Section 7.4, "Flash Program and Erase Characteristics" on page 51.

To read data from blocks within the suspended partition, the Read Array command must be issued to that partition. Read Array, Read Status Register, Read Device Identifier, CFI Query, and Program Resume are valid commands during a program suspend.

A program operation does not need to be suspended in order to read data from a block in another partition that is not programming. If the other partition is already in a Read Array, Read Device Identifier, or CFI Query state, issuing a valid address returns corresponding read data. If the other partition is not in a read mode, one of the read commands must be issued to the partition before data can be read.

During a program suspend, deasserting F-CE# places the flash in standby, reducing active current. F-VPP must remain at its programming level, and F-WP# must remain unchanged while in program suspend. If F-RST# is asserted, the flash is reset.

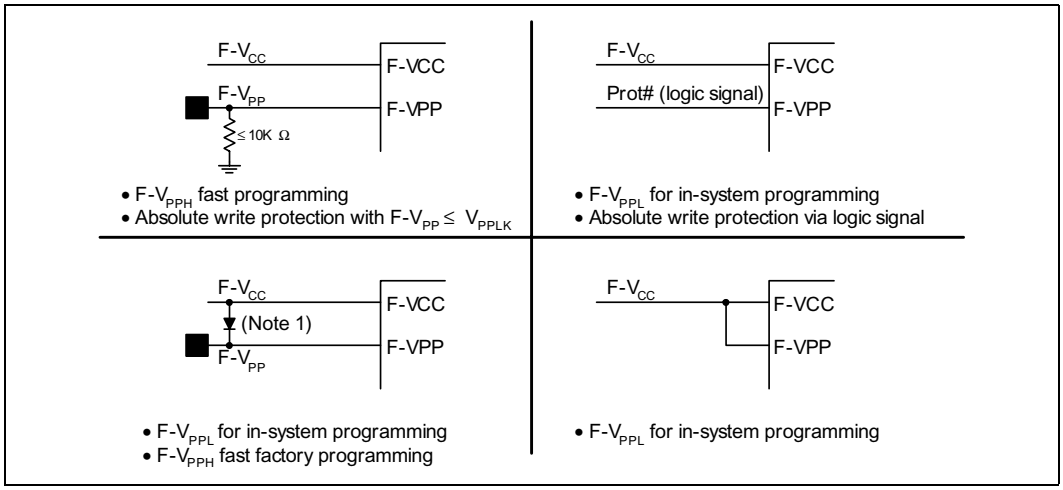
11.5 Flash Program Resume

The Resume command instructs the flash to continue programming, and automatically clears Status Register bits SR[7,2]. This command can be written to any partition. When read at the partition that's programming, the flash outputs data corresponding to the partition's last state. If error bits are set, the Status Register should be cleared before issuing the next instruction. F-RST# must remain deasserted. See Figure 53, "Flash Program Suspend/Resume Flowchart" on page 114.

11.6 Flash Program Protection

When F-V_{PP} = V_{IL}, absolute hardware write protection is provided for all flash blocks. If F-V_{PP} is below V_{PPLK}, programming operations halt and SR.3 is set indicating a F-V_{PP}-level error. Block lock registers are not affected by the voltage level on F-V_{PP}; they may still be programmed and read, even if F-V_{PP} ≤ V_{PPLK}.

Figure 26. Example F-VPP Supply Connections



Flash Erase Operations 12

Flash erasing is performed on an individual block basis. An entire block is erased each time an erase command sequence is issued, and only one block is erased at a time. When a block is erased, all bits within that block read as logical ones. The following sections describe block erase operations in detail.

12.1 Flash Block Erase

Block erase operations are initiated by writing the Block Erase Setup command to the address of the target block to be erased. See Section 9.3, “Flash Command Definitions” on page 66. Next, the Block Erase Confirm command is written to the address of the block to be erased. Erasing can occur in only one partition at a time; all other partitions must be in a read state. If the flash is placed in standby (F-CE# deasserted) during an erase operation, the flash continues to complete the erase operation before entering standby.

Note: $F\text{-}V_{PP} > V_{PPLK}$ and the block must be unlocked (see Figure 56, “Flash Block Erase Flowchart” on page 117).

During a block erase, the flash Write State Machine (WSM) executes a sequence of internally-timed events that conditions, erases, and verifies all bits within the block. Erasing the flash memory array changes “logical-zeros” to “logical-ones.” Memory array bits can be changed to zeros only by programming the block (see Section 11, “Flash Programming Operations” on page 75).

The Status Register can be examined for block erase progress and errors by reading any address within the partition that is being erased. The partition remains in the Read Status Register state until another command is written to that partition. Issuing the Read Status Register command to another partition address sets that partition to the Read Status Register state, allowing erase progress to be monitored at that partition’s address. SR.0 indicates whether the addressed partition or another partition is erasing. The partition’s Status Register bit SR.7 is set upon erase completion.

SR.7 indicates block erase status while the sequence executes. When the erase operation has finished, Status Register bit SR.5 indicates an erase failure if set. SR.3 set would indicate that the WSM could not perform the erase operation because $F\text{-}V_{PP}$ was outside of its acceptable limits. SR.1 set indicates that the erase operation attempted to erase a locked block, causing the operation to abort.

Before issuing a new command, the Status Register contents should be examined and then cleared using the Clear Status Register command. Any valid command can follow once the block erase operation has completed.

12.2 Flash Erase Suspend

Issuing the Erase Suspend command while erasing suspends the block erase operation. This allows data to be accessed from memory locations other than the one being erased. The Erase Suspend command can be issued to any flash address; the corresponding partition is not affected. A block

erase operation can be suspended to perform a word or buffer program operation, or a read operation within any block except the block that is erase suspended. See Figure 53, “Flash Program Suspend/Resume Flowchart” on page 114.

When a block erase operation is executing, issuing the Erase Suspend command requests the WSM to suspend the erase algorithm at predetermined points. The partition that is suspended continues to output SRD after the Erase Suspend command is issued. Block erase is suspended when SR[7,6] are set. Suspend latency is specified in Section 7.4, “Flash Program and Erase Characteristics” on page 51.

During Erase Suspend, a Program command can be issued to any block other than the erase-suspended block. Block erase cannot resume until program operations initiated during erase suspend complete. Read Array, Read Status Register, Read Device Identifier, CFI Query, and Erase Resume are valid commands during Erase Suspend. Additionally, Clear Status Register, Program, Program Suspend, Block Lock, Block Unlock, and Block Lock-Down are valid commands during Erase Suspend.

During an erase suspend, deasserting F-CE# places the flash in standby, reducing active current. F-V_{PP} must remain at a valid level, and F-WP# must remain unchanged while in erase suspend. If F-RST# is asserted, the flash is reset.

12.3 Flash Erase Resume

The Erase Resume command instructs the flash to continue erasing, and automatically clears status register bits SR[7,6]. This command can be written to any partition. When read at the partition that’s erasing, the flash outputs data corresponding to the partition’s last state. If status register error bits are set, the Status Register should be cleared before issuing the next instruction. F-RST# must remain deasserted (see Figure 53, “Flash Program Suspend/Resume Flowchart” on page 114).

12.4 Flash Erase Protection

When F-V_{PP} = V_{IL}, absolute hardware erase protection is provided for all flash blocks. If F-V_{PP} ≤ V_{PPLK}, erase operations halt and SR.3 is set indicating a F-V_{PP} level error.

Flash Security Modes 13

The flash features security modes used to protect the code or data information stored in the flash memory array. The following sections describe each security mode in detail.

13.1 Flash Block Locking

Individual instant block locking is used to protect user code and/or data within the flash memory array. All blocks power up in a locked state to protect array data from being altered during power transitions. Any block can be locked or unlocked with no latency. Locked blocks cannot be programmed or erased; they can only be read.

Software-controlled security is implemented using the Block Lock and Block Unlock commands. Hardware-controlled security can be implemented using the Block Lock-Down command along with asserting F-WP#.

13.1.1 Flash Lock Block

To lock a block, issue the Lock Block Setup command. The next command must be the Lock Block command issued to the desired block's address (see Section 9.3, "Flash Command Definitions" on page 66 and Figure 58, "Flash Block Lock Operations Flowchart" on page 119). If the Set Read Configuration Register command is issued after the Block Lock Setup command, the flash configures the RCR instead.

Block lock and unlock operations are not affected by the voltage level on F-V_{PP}. The block lock bits may be modified and/or read even if F-$V_{PP} \le V_{PPLK}$.

13.1.2 Flash Unlock Block

The Unlock Block command is used to unlock blocks (see Section 9.3, "Flash Command Definitions" on page 66). Unlocked blocks can be read, programmed, and erased. Unlocked blocks return to a locked state when the flash is reset or powered down. If a block is in a lock-down state, WP# must be deasserted before it can be unlocked (see Figure 27, "Flash Block Locking State Diagram" on page 84).

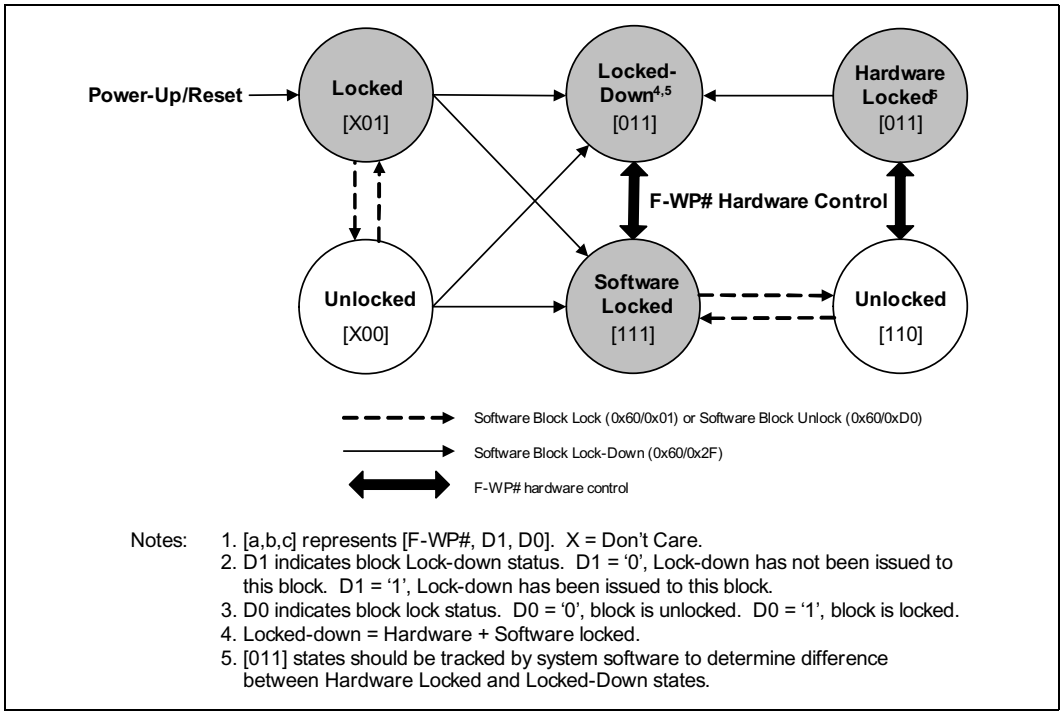
13.1.3 Flash Lock-Down Block

A locked or unlocked block can be locked-down by writing the Lock-Down Block command sequence (see Section 9.3, "Flash Command Definitions" on page 66). Blocks in a lock-down state cannot be programmed or erased; they can only be read. However, unlike locked blocks, their locked state cannot be changed by software commands alone. A locked-down block can only be unlocked by issuing the Unlock Block command with F-WP# deasserted. To return an unlocked block to locked-down state, a Lock-Down command must be issued prior to changing F-WP# to V_{IL}. Locked-down blocks revert to the locked state upon reset or power up the flash (see Figure 27, "Flash Block Locking State Diagram" on page 84).

13.1.4 Flash Block Lock Status

The Read Device Identifier command is used to determine a block's lock status (see Section 15.2, "Flash Read Device Identifier" on page 95). Data bits DQ[1:0] display the addressed block's lock status; DQ0 is the addressed block's lock bit, while DQ1 is the addressed block's lock-down bit.

Figure 27. Flash Block Locking State Diagram



Notes:
1. [a,b,c] represents [F-WP#, D1, D0]. X = Don't Care.
2. D1 indicates block Lock-down status. D1 = '0', Lock-down has not been issued to this block. D1 = '1', Lock-down has been issued to this block.
3. D0 indicates block lock status. D0 = '0', block is unlocked. D0 = '1', block is locked.
4. Locked-down = Hardware + Software locked.
5. [011] states should be tracked by system software to determine difference between Hardware Locked and Locked-Down states.

13.1.5 Flash Block Locking During Suspend

Block lock and unlock changes can be performed during an erase suspend. To change block locking during an erase operation, first issue the Erase Suspend command. Monitor the Status Register until SR.7 and SR.6 are set, indicating the flash is suspended and ready to accept another command.

Next, write the desired lock command sequence to a block, which changes the lock state of that block. After completing block lock or unlock operations, resume the erase operation using the Erase Resume command.

Note: A Lock Block Setup command followed by any command other than Lock Block, Unlock Block, or Lock-Down Block produces a command sequence error and set Status Register bits SR.4 and SR.5. If a command sequence error occurs during an erase suspend, SR.4 and SR.5 remains set, even after the erase operation is resumed. Unless the Status Register is cleared using the Clear Status Register command before resuming the erase operation, possible erase errors may be masked by the command sequence error.

If a block is locked or locked-down during an erase suspend of the same block, the lock status bits change immediately. However, the erase operation completes when it is resumed. Block lock operations cannot occur during a program suspend.

13.2 Flash One-Time Programmable Protection Registers

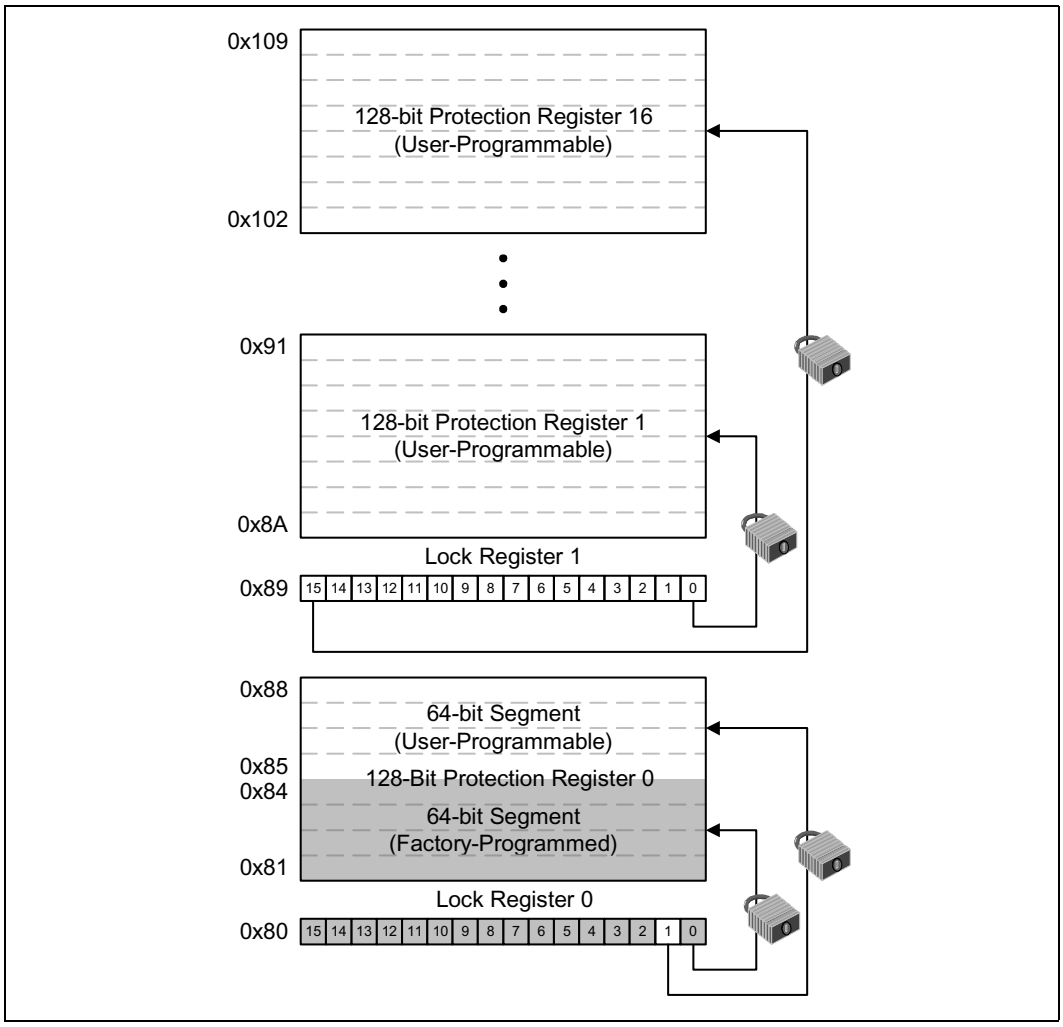
The flash contains seventeen Protection Registers (PRs) that can be used to implement system security measures and/or flash identification. Each Protection Register can be individually locked.

The first 128-bit Protection Register (PR0) is comprised of two 64-bit (8-word) segments. The lower 64-bit segment is pre-programmed at the factory with a unique 64-bit number. The remaining 64-bit segment, as well as the other sixteen 128-bit Protection Registers, are blank as default. Users can program these registers as needed. When programmed, users can then lock the Protection Register(s) to prevent additional bit programming. See Figure 28, “Flash One-Time Programmable Protection Register Map” on page 86.

The user-programmable Protection Registers contain one-time programmable (OTP) bits; when programmed, register bits cannot be erased. Each Protection Register can be accessed multiple times to program individual bits, as long as the register remains unlocked.

Each Protection Register has an associated Lock Register bit. When a Lock Register bit is programmed, the associated Protection Register can only be read; it can no longer be programmed. Additionally, because the Lock Register bits themselves are OTP, when programmed, Lock Register bits cannot be erased. Therefore, when a Protection Register is locked, it cannot be unlocked

Figure 28. Flash One-Time Programmable Protection Register Map



13.2.1 Flash Reading of the Protection Registers

The Protection Registers can be read from within any partition's address space. To read the Protection Register, first issue the Read flash Identifier command at any partitions' address to place that partition in the Read Device Identifier state (see Section 9.3, "Flash Command Definitions" on page 66). Next, perform a read operation at that partition's base address plus the address offset corresponding to the register to be read. Table 28, "Flash Die Identifier Information" on page 96 shows the address offsets of the Protection Registers and Lock Registers. Register data is read 16 bits at a time.

Note: If a program or erase operation occurs within the flash while it is reading a Protection Register, certain restrictions may apply. See Table 26, "Simultaneous Flash Operation Restrictions" on page 92 for details.

13.2.2 Flash Programming of the Protection Registers

To program any of the Protection Registers, first issue the Program Protection Register command at the parameter partition's base address plus the offset to the desired Protection Register (see Section 9.3, "Flash Command Definitions" on page 66). Next, write the desired Protection Register data to the same Protection Register address (see Figure 28, "Flash One-Time Programmable Protection Register Map" on page 86).

The flash programs the 64-bit and 128-bit user-programmable Protection Register data 16 bits at a time (see Figure 59, "Flash One-Time Programmable Protection Register Programming Flowchart" on page 120). Issuing the Program Protection Register command outside of the Protection Register's address space causes a program error (SR.4 set). Attempting to program a locked Protection Register causes a program error (SR.4 set) and a lock error (SR.1 set).

Note: If a program or erase operation occurs when programming a Protection Register, certain restrictions may apply. See Table 26, "Simultaneous Flash Operation Restrictions" on page 92 for details.

13.2.3 Flash Locking the Protection Registers

Each Protection Register can be locked by programming its respective lock bit in the Lock Register. To lock a Protection Register, program the corresponding bit in the Lock Register by issuing the Program Lock Register command, followed by the desired Lock Register data (see Section 9.3, "Flash Command Definitions" on page 66). The physical addresses of the Lock Registers are 0x80 for register 0 and 0x89 for register 1. These addresses are used when programming the lock registers. See Table 28, "Flash Die Identifier Information" on page 96.

Bit 0 of Lock Register 0 is already programmed at the factory, locking the lower, pre-programmed 64-bits region of the first 128-bit Protection Register containing the unique identification number of the flash. Bit 1 of Lock Register 0 can be programmed by the user to lock the user-programmable, 64-bits region of the first 128-bits Protection Register. The other bits in Lock Register 0 are not used.

Lock Register 1 controls the locking of the upper sixteen 128-bit Protection Registers. Each of the 16 bits of Lock Register 1 correspond to each of the upper sixteen 128-bit Protection Registers. Programming a bit in Lock Register 1 locks the corresponding 128-bit Protection Register.

Caution: After being locked, the Protection Registers cannot be unlocked.

Flash Dual-Operation Considerations 14

The multi-partition architecture of the flash allows background programming (or erasing) to occur in one partition while data reads (or code execution) take place in another partition.

14.1 Flash Partitioning

The flash memory array is divided into multiple 16-Mbit partitions, which allows simultaneous read-while-write operations. Simultaneous program and erase is not allowed. Only one partition at a time can be in program or erase mode.

The flash supports read-while-write operations with bus cycle granularity and not command granularity. In other words, it is not assumed that both bus cycles of a two cycle command (an erase command for example) will always occur as back to back bus cycles to the flash. In practice, code fetches (reads) may be interspersed between write cycles to the flash, and they will likely be directed to a different partition than the one being written. This is especially true when a processor is executing code from one partition that instructs the processor to program or erase in another partition.

14.2 Flash Read-While-Write Command Sequences

When issuing commands to the flash, a read operation can occur between 2-cycle Write command's (Figure 29, and Figure 30). However, a write operation issued between a 2-cycle commands write sequence causes a command sequence error. (See Figure 31, "Flash Operating Mode with Illegal Command Sequence Example" on page 90)

When reading from the same partition after issuing a Setup command, Status Register data is returned, regardless of the read mode of the partition prior to issuing the Setup command.

Figure 29. Flash Operating Mode with Correct Command Sequence Example

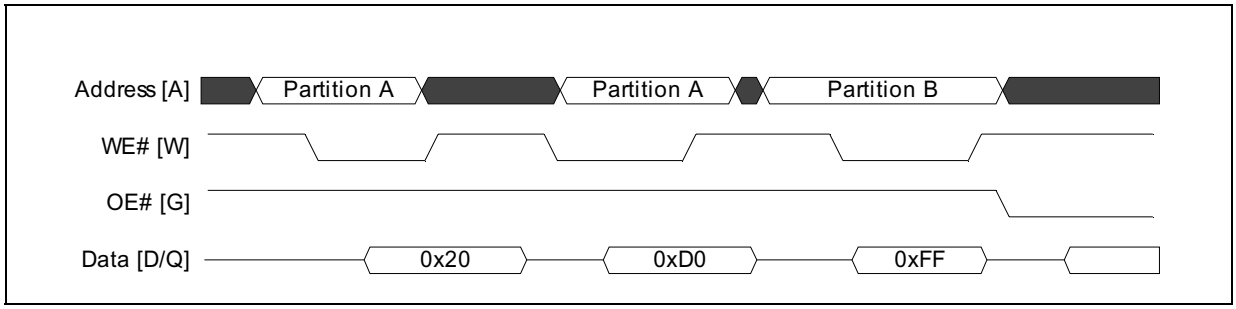


Figure 30. Flash Operating Mode with Correct Command Sequence Example

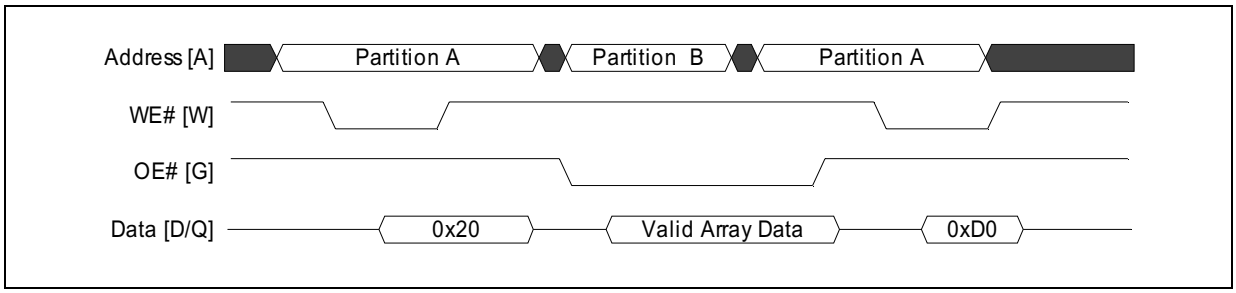
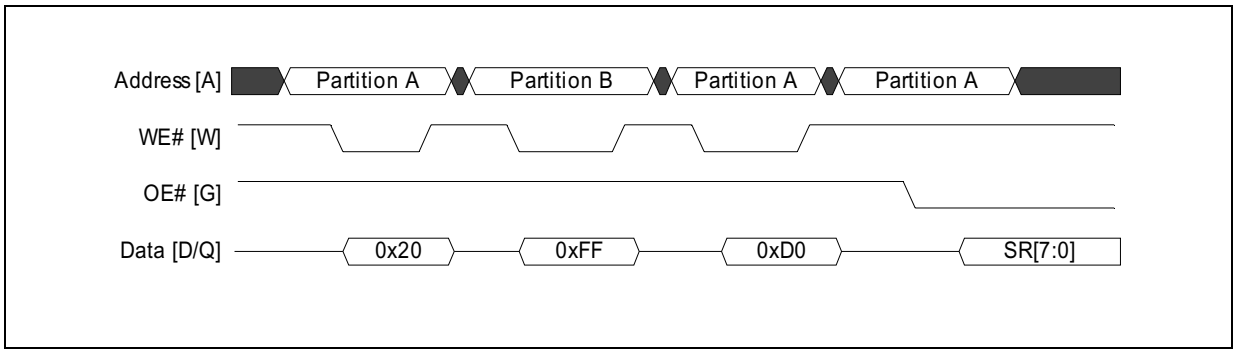


Figure 31. Flash Operating Mode with Illegal Command Sequence Example



14.2.1 Simultaneous Flash Operation Details

The flash supports simultaneous read from one partition while programming or erasing in any other partition. Certain features like the Protection Registers and Query data have special requirements with respect to simultaneous operation capability. These will be detailed in the following sections.

14.2.2 Flash Write to Flash Asynchronous Read Transition

The AC parameter W18 (t_{WHAV} - WE# High to Address Valid) is required when transitioning from a write cycle (WE# going high) to perform an asynchronous read (only address valid is required).

14.2.3 Flash Write to Flash Synchronous Read Operation Transition

The flash AC parameters W19 (t_{WHCV} : WE# High to Clock Valid) and W20 (t_{WHVH} : WE# High to ADV# High) are required when transitioning from a write cycle (WE# going high) to perform a synchronous burst read. A delay from WE# going high to a valid clock edge or ADV# going high to latch a new address must be met.

14.2.4 Flash Write with Clock Active

The flash AC parameters W21 (t_{VHWL}: ADV# High to WE# Low) and W22 (t_{CHWL}: Clock high to WE# low) are required during write operations when the flash is in a synchronous mode and the clock is active. A write bus cycle consists of two parts:

- The processor provides an address to the flash.
- The processor then provides data to the flash.

The flash in turn binds the received data with the received address. When operating synchronously (RCR.15 = 0), the address of a write cycle may be provided to the flash by the first active clock edge with ADV# low, or rising edge of ADV# as long as the applicable cycle separation conditions are met between each cycle.

If neither a clock edge nor a rising ADV# edge is used to provide a new address at the beginning of a write cycle (the clock is stopped and ADV# is low), the address may also be provided to the flash by holding the address bus stable for the required amount of time (W5, t_{AVWH}) before the rising WE# edge.

Alternatively, the host may choose not to provide an address to the flash during subsequent write cycles (if ADV# is high and only F-CE# or WE# is toggled to separate the prior cycle from the current write cycle). In this case, the flash will use the most recently provided address from the host.

For representation of these timings see:

- Figure 20, “Flash Write to Flash Asynchronous Read Timing” on page 49
- Figure 21, “Flash Synchronous Read to Flash Write Timing” on page 49
- Figure 22, “Flash Write to Flash Synchronous Read Timing” on page 50

14.2.5 Flash Read During Flash Buffered Programming

The multi-partition architecture of the flash allows background programming (or erasing) to occur in one partition while data reads (or code execution) take place in another partition.

To perform a read while buffered programming operation, first issue a Buffered Program set up command in a partition. When a read operation occurs in the same partition after issuing a setup command, Status Register data will be returned, regardless of the read mode of the partition prior to issuing the setup command.

To read data from a block in other partition and the other partition already in read array mode, a new block address must be issued. However, if the other partition is not already in read array mode, issuing a read array command will cause the buffered program operation to abort and a command sequence error would be posted in the Status Register.

Simultaneous read-while-Buffered EFP is not supported.

14.3 Simultaneous Flash Operation Restrictions

Since the flash supports simultaneous read from one partition while programming or erasing in another partition, certain features like the Protection Registers and CFI Query data have special requirements with respect to simultaneous operation capability. (Table 26 provides details on restrictions during simultaneous operations.)

Table 26. Simultaneous Flash Operation Restrictions

Protection Register or CFI data	Parameter Partition Array Data	Other Partitions	Notes
Read	(See Notes)	Write/Erase	While programming or erasing in a main partition, the Protection Register or CFI data may be read from any other partition. Reading the parameter partition array data is not allowed if the Protection Register or Query data is being read from addresses within the parameter partition.
(See Notes)	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the Protection Registers or CFI data from parameter partition addresses is not allowed when reading array data from the parameter partition.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the Protection Registers or CFI data in a partition that is *different* from the one being programed/erased, and also *different* from the parameter partition is allowed.
Write	No Access Allowed	Read	While programming the Protection Register, reads are only allowed in the other main partitions. Access to array data in the parameter partition is not allowed. Programming of the Protection Register can only occur in the parameter partition, which means this partition is in Read Status.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the Protection Registers or CFI data are not allowed in *any* partition. Reads in partitions other than the parameter partition are supported.

Special Flash Read States 15

The following sections describe non-array read states. Non-array reads can be performed in asynchronous read or synchronous burst mode. A non-array read operation occurs as asynchronous single-word mode. When non-array reads are performed in asynchronous page mode only the first data is valid and all subsequent data are undefined. When a non-array read operation occurs as synchronous burst mode, the same word of data requested will be output on successive clock edges until the burst length requirements are satisfied.

Each partition can be in one of its read states independent of other partitions' modes. See Figure 12, "Flash Asynchronous Single-Word Read with ADV# Low" on page 43 and Figure 15, "Flash Synchronous Single-Word Array or Non-array Read Timing" on page 45 for details.

15.1 Flash Read Status Register

The status of any partition is determined by reading the Status Register from the address of that particular partition. To read the Status Register, issue the Read Status Register command within the desired partition's address range. Status Register information is available at the partition address to which the Read Status Register, Word Program, or Block Erase command was issued. Status Register data is automatically made available following a Word Program, Block Erase, or Block Lock command sequence. Reads from a partition after any of these command sequences outputs that partition's status until another valid command is written to that partition (e.g. Read Array command).

The Status Register is read using single asynchronous-mode or synchronous burst mode reads. Status Register data is output on DQ[7:0], while 0x00 is output on DQ[15:8]. In asynchronous mode the falling edge of OE#, or F-CE# (whichever occurs first) updates and latches the Status Register contents. However, reading the Status Register in synchronous burst mode, F-CE# or ADV# must be toggled to update status data. The Status Register read operations do not affect the read state of the other partitions.

The flash Write Status bit (SR.7) provides overall status of the flash. The Partition Status bit (SR.0) indicates whether the addressed partition or some other partition is actively programming or erasing. Status register bits SR[6:1] present status and error information about the program, erase, suspend, F-V_{PP}, and block-locked operations.

Table 27. Flash Status Register Description

Status Register (SR)							Default Value = 0x80
Flash Write Status	Erase Suspend Status	Erase Status	Program Status	F-VPP Status	Program Suspend Status	Block-Locked Status	Partition Status
DWS	ESS	ES	PS	F-VPPS	PSS	BLS	PWS
7	6	5	4	3	2	1	0

Bit	Name	Description
7	Flash Write Status (DWS)	0 = Flash is busy; program or erase cycle in progress; SR.0 valid. 1 = Flash is ready; SR[6:1] are valid.
6	Erase Suspend Status (ESS)	0 = Erase suspend not in effect. 1 = Erase suspend in effect.
5	Erase Status (ES)	0 = Erase successful. 1 = Erase fail or program sequence error when set with SR[4,7].
4	Program Status (PS)	0 = Program successful. 1 = Program fail or program sequence error when set with SR[5,7]
3	F-VPP Status (F-VPPS)	0 = F-V_{PP} within acceptable limits during program or erase operation. 1 = F-$V_{PP} \leq V_{PPLK}$ during program or erase operation.
2	Program Suspend Status (PSS)	0 = Program suspend not in effect. 1 = Program suspend in effect.
1	Block Locked Status (BLS)	0 = Block not locked during program or erase. 1 = Block locked during program or erase; operation aborted.
0	Partition Write Status (PWS)	DWS PWS 0 0 = Program or erase operation in addressed partition. 0 1 = Program or erase operation in other partition. 1 0 = No active program or erase operations. 1 1 = Reserved. (For Buffered EFP operation, see Section 11.3, "Flash Buffered Enhanced Factory Programming" on page 77)

Always clear the Status Register prior to resuming erase operations to avoid Status Register ambiguity when issuing commands during Erase Suspend. If a command sequence error occurs during an erase-suspend state, the Status Register contains the command sequence error status (SR[7,5,4] are set). When the erase operation resumes and finishes, possible errors during the erase operation cannot be detected by the Status Register because it contains the previous error status.

15.1.1 Flash Clear Status Register

The flash Clear Status Register command clears the status register, leaving all partition read states unchanged. It functions independent of F-V_{PP}. The Write State Machine (WSM) sets and clears SR[7,6,2,0], but it sets bits SR[5:3,1] without clearing them. The Status Register should be cleared before starting a command sequence to avoid any ambiguity. A flash reset also clears the Status Register.

15.2 Flash Read Device Identifier

The Read Device Identifier command instructs the addressed partition to output manufacturer code, device identifier code, block-lock status, protection register data, or configuration register data when that partition's addresses are read (see Section 9.3, "Flash Command Definitions" on page 66 for details on issuing the Read Device Identifier command). Table 28, "Flash Die Identifier Information" on page 96 show the address offsets and data values for this flash.

Issuing a Read Device Identifier command to a partition that is programming or erasing places that partition in the Read Identifier state while the partition continues to program or erase in the background.

Table 28. Flash Die Identifier Information

Item	Address(1,2)	Data
Manufacturer Code	PBA + 0x00	0089h
Flash ID Code	PBA + 0x01	8810
Block Lock Configuration: • Block Is Unlocked • Block Is Locked • Block Is not Locked-Down • Block Is Locked-Down	BBA + 0x02	Lock Bit: <User Defined> DQ0 = 0b0 DQ1 = 0b1 DQ0 = 0b0 DQ1 = 0b1
Configuration Register	PBA + 0x05	Configuration Register Data
Lock Register 0	PBA + 0x80	PR-LK0
64-bit Factory-Programmed Protection Register	PBA + 0x81–0x84	Factory Protection Register Data
64-bit User-Programmable Protection Register	PBA + 0x85–0x88	User Protection Register Data
Lock Register 1	PBA + 0x89	Protection Register Data
16x128-bit User-Programmable Protection Registers	PBA + 0x8A–0x109	PR-LK1

Notes:
1. PBA = Partition Base Address.
2. BBA = Block Base Address.

15.3 CFI Query

The CFI Query command instructs the flash to output Common Flash Interface (CFI) data when partition addresses are read. See Section 9.3, “Flash Command Definitions” on page 66 for details on issuing the CFI Query command. Appendix B, “Common Flash Interface” on page 121 shows CFI information and address offsets within the CFI database.

Issuing the CFI Query command to a partition that is programming or erasing places that partition’s outputs in the CFI Query state, while the partition continues to program or erase in the background.

The CFI Query command is subject to read restrictions dependent on parameter partition availability, as described in Table 26, “Simultaneous Flash Operation Restrictions” on page 92.

Part 3: LPSDRAM Operations

LSDRAM Register Definition 16

16.1 Mode Register

The Mode Register is used to define specific modes of operation of the LPSDRAM. This definition includes the selection of a burst length, burst type, a CAS# latency, and a write burst mode. The Mode Register settings are illustrated in the Table below. The Mode Register is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the LPSDRAM loses power, or the LPSDRAM goes in Deep Power-Down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD}.

Addresses A[12:11, 9:8] must be set to "0" for all Mode Register programming. D-BA[1:0] should be set to (0,0) to differentiate from Extended Mode Register Programming.

Table 29. LPSDRAM Setting for Burst Length

Burst Length		A3	A2	A1
A4 = 0	A4 = 1			
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Full Page	Reserved	1	1	1

Notes:
1. States not mentioned are undefined.
2. The sequential burst will wrap on reaching the last column of the burst length.

Table 30. LPSDRAM Setting for Burst Type

A4	Burst Type
0	Sequential
1	Interleaved

Table 31. LPSDRAM Setting for CAS# Latency

A7	A6	A5	CAS# Latency
0	0	1	1
0	1	0	2
0	1	1	3

Note: CAS# Latency not mentioned are undefined.

Table 32. LPSDRAM Setting for Write Burst Mode

A10	Write Burst Mode
0	Programmed Burst
1	Single Word Burst

16.2 LPSDRAM Extended Mode Register

The Extended Mode Register controls two power saving functions: Temperature-Compensated Self Refresh (TCSR), and Partial-Array Self Refresh (PASR). Both these features can only be used when the LPSDRAM is under Self Refresh. In addition, the Configurable Output Driver Strength can be programmed through the Extended Mode Register.

The Extended Mode Register is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the LPSDRAM loses power, or the LPSDRAM goes in deep power down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD}.

To program the Extended Mode Register, bank addresses D-BA1 = 1, and D-BA0 = 0 should be used. Addresses A[12:6] should be set to '0'.

Table 33. LPSDRAM Setting for Partial-Array Self Refresh

A3	A2	A1	Self-Refresh Coverage
0	0	0	Four Banks
0	0	1	Two Banks (Bank 0 & Bank 1)
0	1	0	One Bank (Bank 0)

Table 34. LPSDRAM Setting for Temperature-Compensated Self Refresh

A5	A4	Maximum Ambient Temperature
1	1	85 °C
0	0	70 °C
0	1	45 °C
1	0	15 °C

Table 35. LPSDRAM Configurable Output Driver Strength

A7	A6	Strength	Output Load (pF)
0	0	Normal	30
0	1	Half	TBD
1	0	Reserved	NA
1	1	Reserved	NA

Note: LPSDRAM AC specs are guaranteed only when normal output driver strength is used.

LPSDRAM Command and Operation 17

17.1 LPSDRAM No Operation / LPSDRAM Deselect

The No Operation / LPSDRAM Deselect command is used on a LPSDRAM that is selected (D-CS# / R-DS# is low). It is also used to deselect the LPSDRAM by preventing new commands from being executed. Operations already in progress are not affected.

17.2 LPSDRAM Active

The Active command is used to activate a row in particular bank for a subsequent read or write access. The value of the bank D-BA[1:0] and the row address needs to be provided. The row remains active until a precharge command is issued to the bank. A Precharge command must be issued before opening a different row in the same bank.

More than one bank can be active at any time. A read or write command could be issued to that row, subject to the t_{RCD} specification. t_{RCD} (min) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the active command on which the read/write can be entered. A subsequent Active command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive active commands on the same bank is defined by t_{RC}. The minimum time interval between two successive active commands on the different banks is defined by t_{RRD}. This is illustrated in Figure 34 on page 104.

17.3 LPSDRAM Read Command

Read command is used to initiate a burst read to an active row. The value of D-BA[1:0] select the bank and address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Output data appears on the data bus, subject to the logic level on the D-DM[1:0] inputs two clocks earlier. D-DM[1:0] latency for read command is 2 clock cycles.

The burst length is set in the mode register. The starting column and bank address is provided along with the auto precharge option. During read bursts, the starting valid data-out corresponding to the starting column address will be available after CAS latency cycles after the read command. Each subsequent data-out will be valid by the next positive edge of the clock. This is shown in Figure 35, “LPSDRAM Example of CAS# Latency, CL = 2” on page 105 with a CAS latency of 2. Data from a read burst may be truncated by a subsequent read command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new read command can be issued as early as CL-1 cycles before the last desired element. This is shown in Figure 36, “Consecutive LPSDRAM Read Bursts with CL = 2” on page 105.

Figure 37 on page 105 shows random LPSDRAM access reads. These can be issued to the same or different banks.

A read burst can be terminated by a subsequent write command, and data from a fixed length read burst can be followed by a write command. The write command may be initiated on the clock edge immediately following the last data element from the read burst, provided the I/O contention could be avoided. D-DM[1:0] can be used to control I/O contention as shown in Figure 38, "LPSDRAM Read to LPSDRAM Write Command" on page 106. D-DM[1:0] latency is 2 clocks for output buffers masking, so the D-DM[1:0] signal must be set high at least 2 clocks prior to the write command. D-DM[1:0] latency for Write is zero clocks, so D-DM[1:0] must be set low before write command to ensure data written is not masked.

A read burst may be followed by or truncated with a Precharge command, which could be issued CL-1 cycles before the last desired element. This is shown in Figure 39, "LPSDRAM Read Command Followed by Precharge" on page 106. Following Precharge command, another command to the same bank cannot be issued until t_{RP} is met. Similarly Burst Terminate command can be used to stop a burst as shown in Figure 40, "LPSDRAM Read Followed by Burst Terminate" on page 106.

17.4 LPSDRAM Write Command

The write command is used to initiate a burst write access to an active row. The value of D-BA[1:0] select the bank and address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Input data appearing on the data bus, is written to the memory array subject to the D-DM[1:0] input logic level appearing coincident with the data. D-DM[1:0] latency for write command is 0-clock cycle.

The burst length is set in the mode register. The starting column and bank address is provided along with the auto precharge option. The first valid data-in is registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge. Figure 39, "LPSDRAM Read Command Followed by Precharge" on page 106 shows 2 consecutive 4 word write bursts. A write burst may be followed by or truncated with a Precharge command to the same bank. The Precharge should be issued t_{WR} after the clock edge after the last desired input data is entered. In addition, when truncating a Write burst, the D-DM[1:0] signal must be used to mask input data for the clock edge coincident with the precharge command. This is shown in Figure 42 and Figure 43 on page 107, where t_{WR} corresponds to either 1 or 2 clock cycles, respectively. Following the Precharge command, a subsequent command cannot be issued to the same bank until t_{RP} is met.

Write Burst can be truncated with a Burst Terminate command. While truncating, the input data being applied coincident to the Burst Terminate will be ignored.

Data for any Writes may be truncated by a subsequent Read command as shown in Figure 44 on page 108. Once the Read command is registered, the Data inputs will be ignored.

17.5 LPSDRAM Power-Down

Power down occurs if D-CKE is set low coincident with LPSDRAM Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power-Down. If power down occurs when one or more banks are active, it is referred to as Active power down. The LPSDRAM cannot stay in this mode for longer than the refresh period (64 ms) without losing data. The power down state is exited by setting D-CKE high while issuing a LPSDRAM Deselect or NOP command. This is shown in Figure 45 on page 108.

17.6 LPSDRAM Deep Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPSDRAM are stopped and all memory data are lost in this mode. To enter the DPD mode, all banks must be precharged, prior to the DPD command. To exit this mode, the D-CKE is taken high after the clock is stable.

17.7 LPSDRAM Clock Suspend

This mode occurs when a column access or burst is in progress, and D-CKE is set low. The internal clock gets suspended freezing the LPSDRAM logic. Any command or data present on the input pins at the time of suspended internal clock is ignored. The output data on the pins stays frozen. This mode is exited by setting D-CKE high, which results in resumption of the operation. Figure 46 on page 108 shown Clock suspend during a Write burst and Figure 47 on page 109 shows a clock suspend during a Read burst.

17.8 LPSDRAM Precharge

The Precharge is used to deactivate an active row in a particular bank or active row in all banks. The banks will be available for row access after a specified time (t_{RP}) after the Precharge command is issued. If one bank is to precharged, the particular bank address needs to be addressed. If all banks are to be precharged, A11 should be set high along with the Precharge command.

17.9 LPSDRAM Auto Precharge

Auto Precharge is accomplished when A11 is high, to enable auto precharge in conjunction with a specific read or write command. This precharges the row after the read or write burst is complete. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst. Another command to the same bank must not be issued until the precharge time (t_{RP}) is completed. Auto precharge does not apply in full-page burst mode. Auto precharge is non- persistent.

17.10 LPSDRAM Concurrent Auto Precharge

If an access command with Auto Precharge enabled is being executed, it can be interrupted by another access command.

- Figure 48 on page 109 shows a Read with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The Read to bank m will interrupt the Read to Bank n, CAS# latency later. The precharge to bank n will begin when the Read to bank m is registered.
- Figure 49 on page 109 shows a Read with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The precharge to bank n will begin when the Write to bank m is registered. D-DM[1:0] should be set high 2 clock before the Write command to prevent bus contention.

- Figure 50 on page 110 shows a Write with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Read to bank m.
- Figure 51 on page 110 shows a Write with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Write to bank m.

Figure 32. LPSDRAM Auto Refresh Cycles with D-CKE High

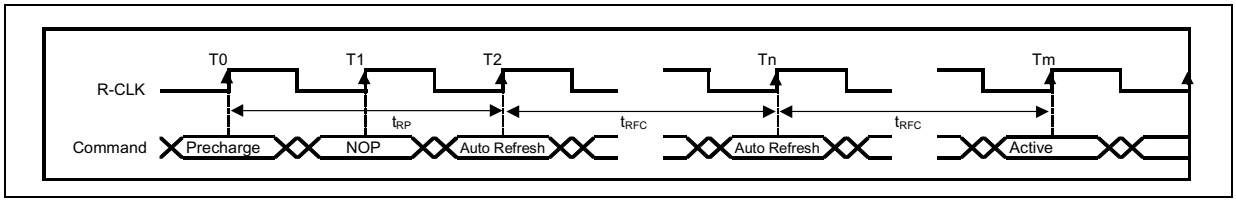


Figure 33. LPSDRAM Self Refresh Entry and Exit Mode

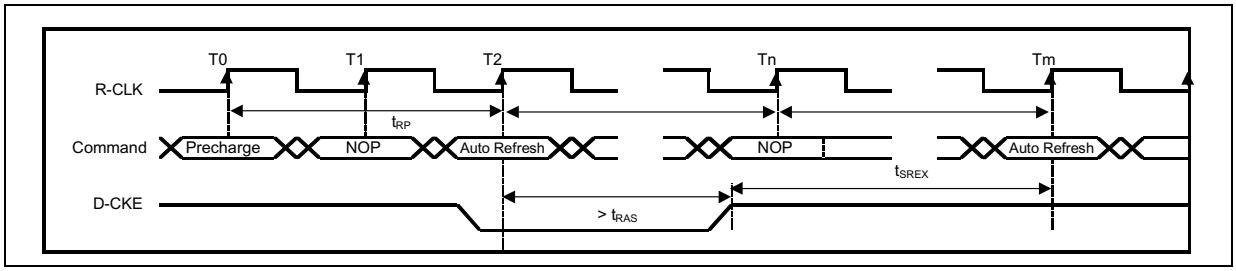


Figure 34. LPSDRAM Active Command and LPSDRAM Read Access Command Issued to 2 Different Banks

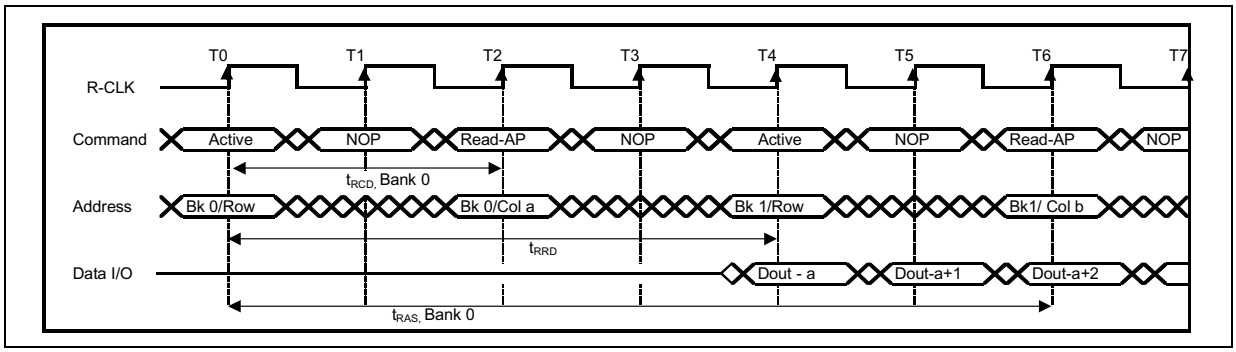


Figure 35. LPSDRAM Example of CAS# Latency, CL = 2

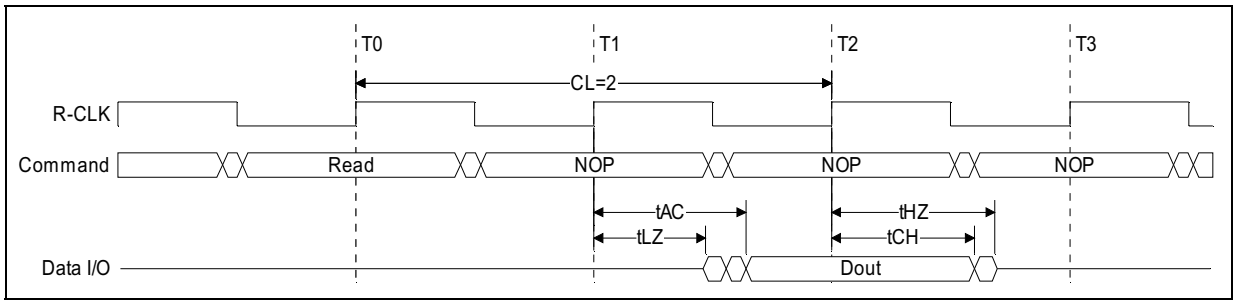
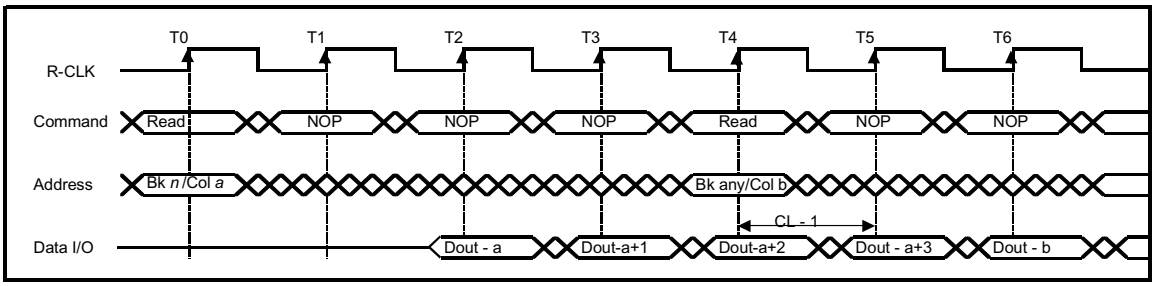


Figure 36. Consecutive LPSDRAM Read Bursts with CL = 2



Note: New command should be issued CL-1 clock cycles before the last desired data. New command can be used to truncate previous Read Burst.

Figure 37. Random LPSDRAM Read Access with CL = 2

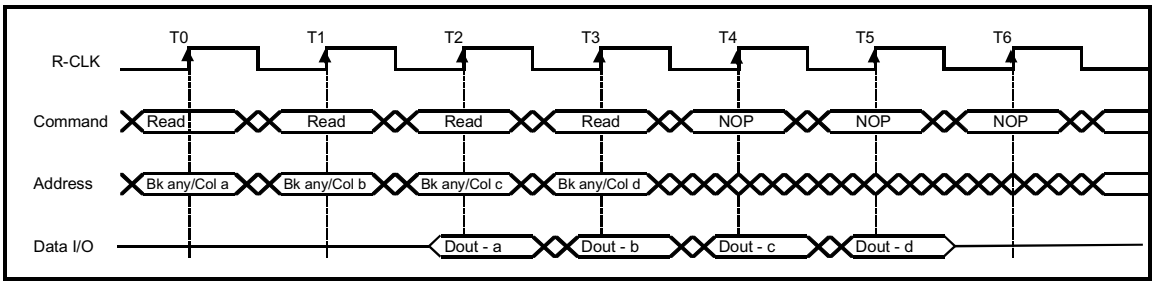
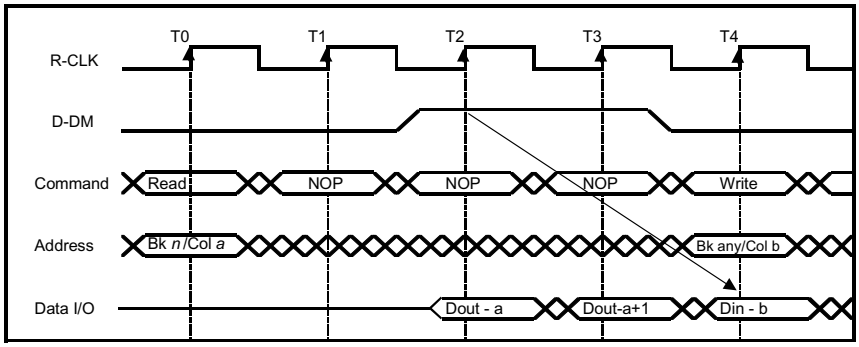
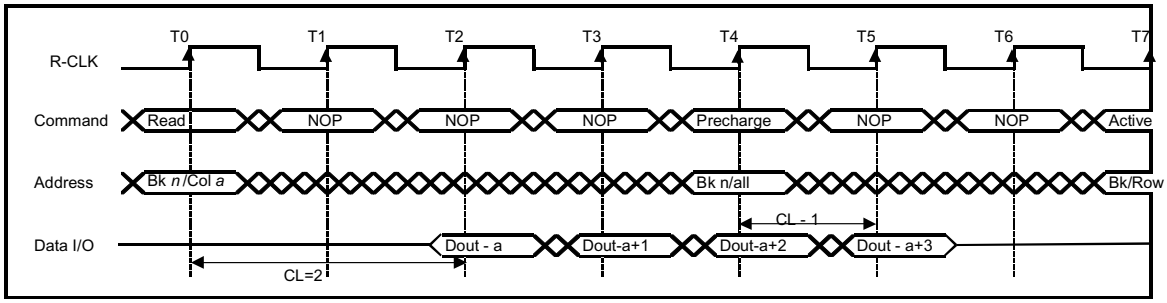


Figure 38. LPSDRAM Read to LPSDRAM Write Command



Note: Data masking used to prevent I/O contention.

Figure 39. LPSDRAM Read Command Followed by Precharge



Note: Command issued CL-1 clocks before last desired data-out element.

Figure 40. LPSDRAM Read Followed by Burst Terminate

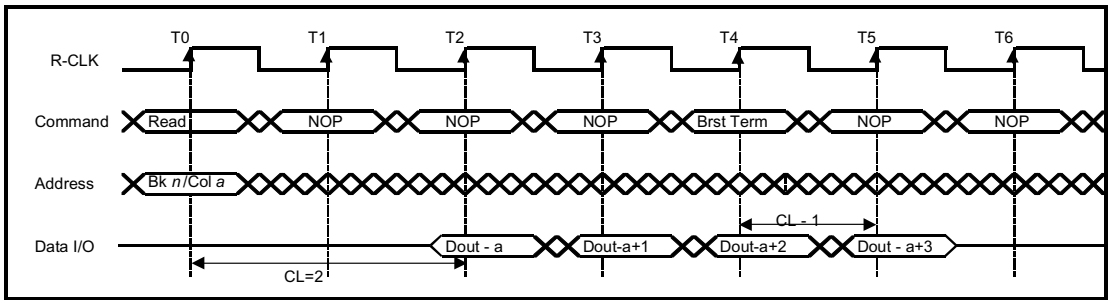
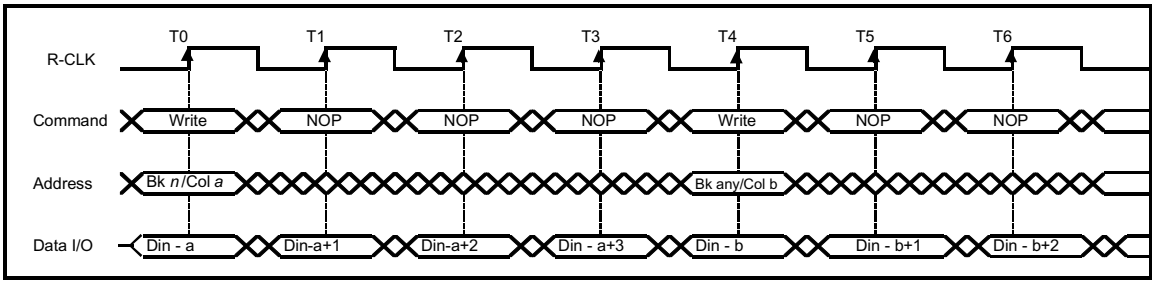


Figure 41. Random LPSDRAM Write to 4-Word Bursts



Note: The commands can be to any active bank.

Figure 42. LPSDRAM Write to Precharge Command Where Write Recovery Takes 1 Clock Cycle

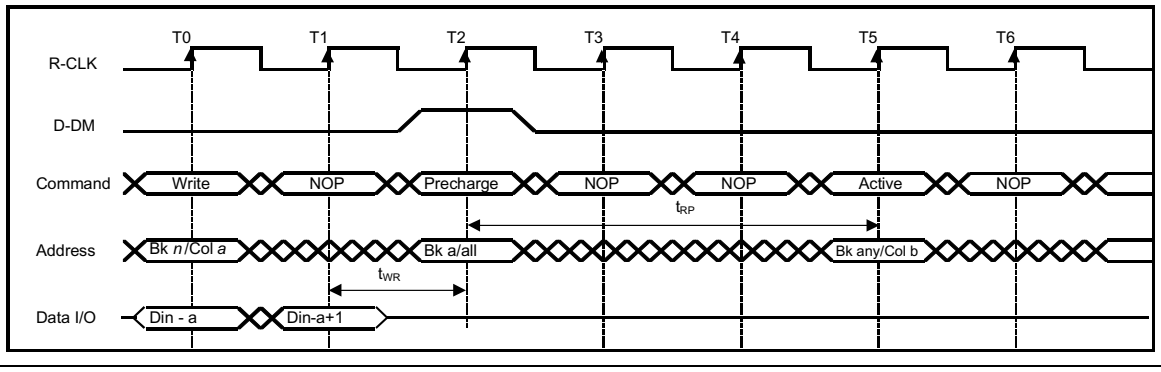


Figure 43. LPSDRAM Write to Precharge Command Where Write Recovery Takes 2 Clock Cycles

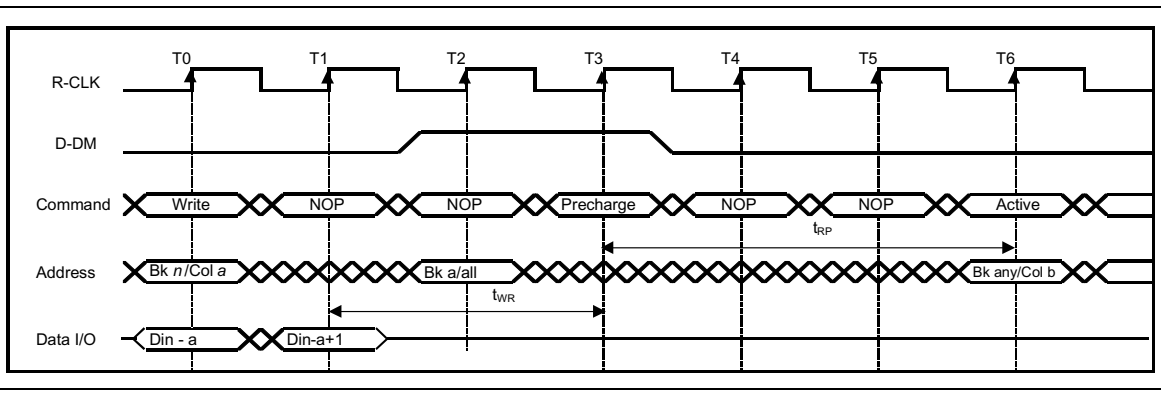
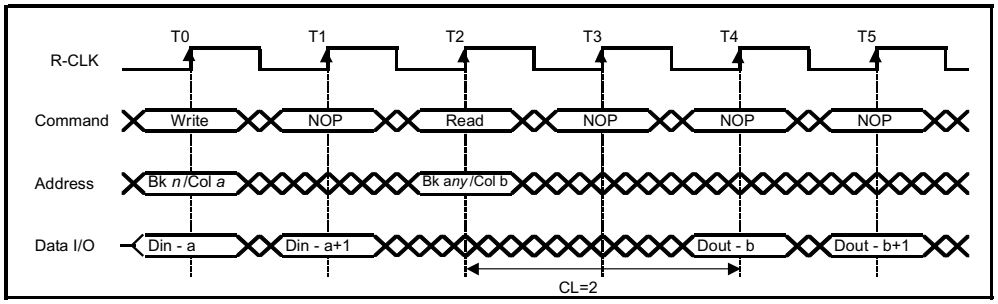
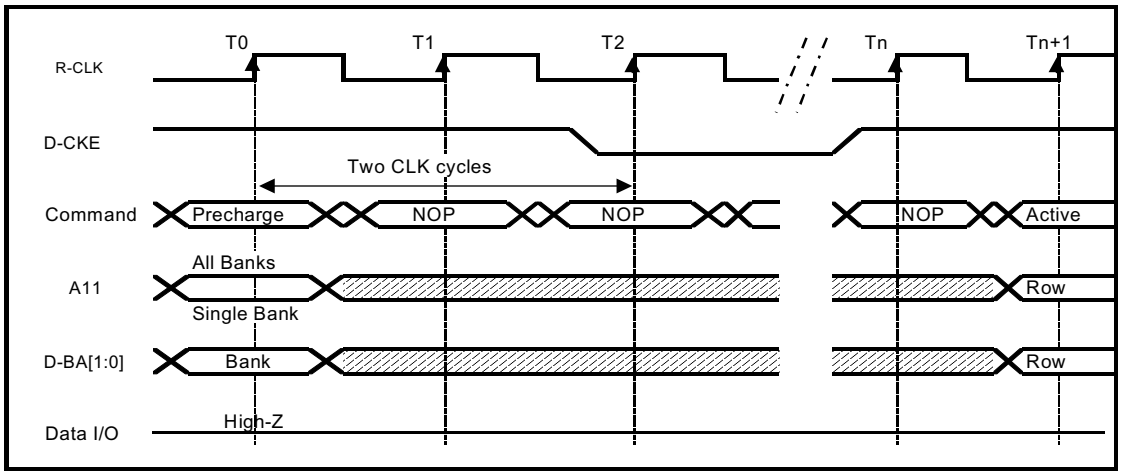


Figure 44. LPSDRAM Write Command Followed by LPSDRAM Read Command



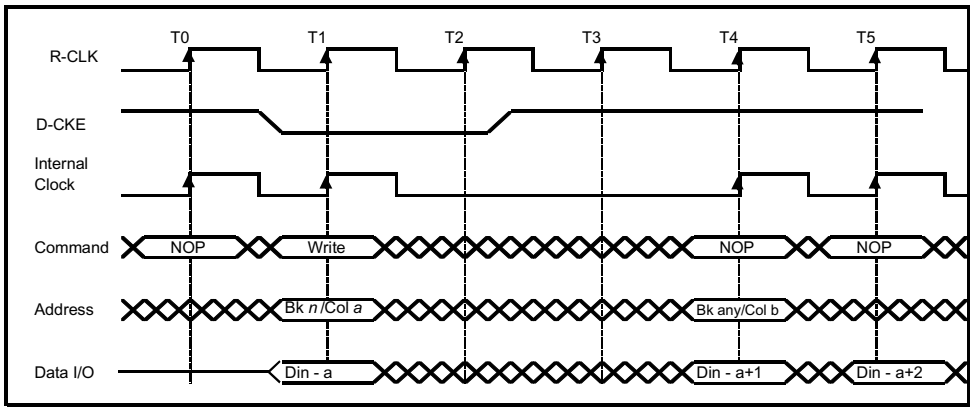
Note: The Read and Write command can be done to any bank. (CL = 2)

Figure 45. LPSDRAM Precharge Power-Down Mode



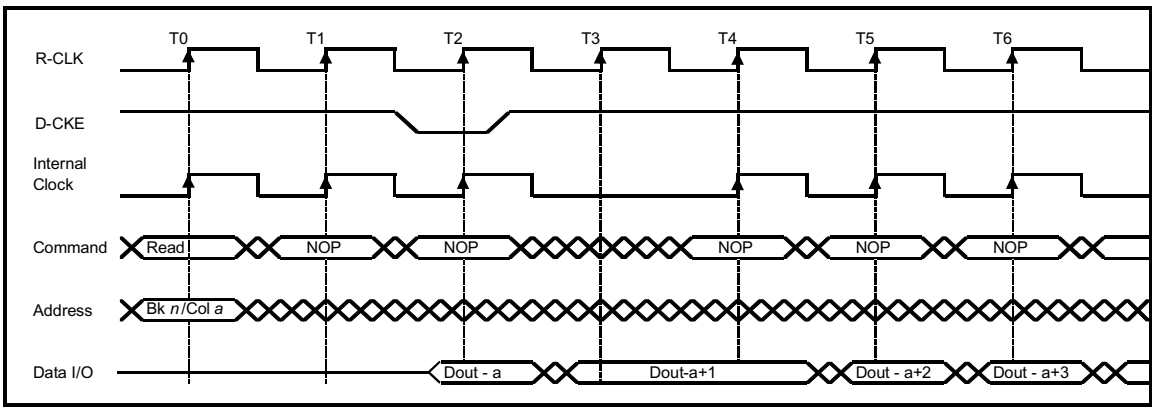
Note: All banks are idle with D-CKE low.

Figure 46. LPSDRAM Clock Suspend During LPSDRAM Write Burst



Note: Input data is ignored when internal clock is suspended.

Figure 47. LPSDRAM Clock Suspend During LPSDRAM Read Burst (CL = 2)



Note: Output data gets frozen while internal clock is suspended.

Figure 48. LPSDRAM Read with Auto Precharge to Bank n Interrupted by Read to Bank m

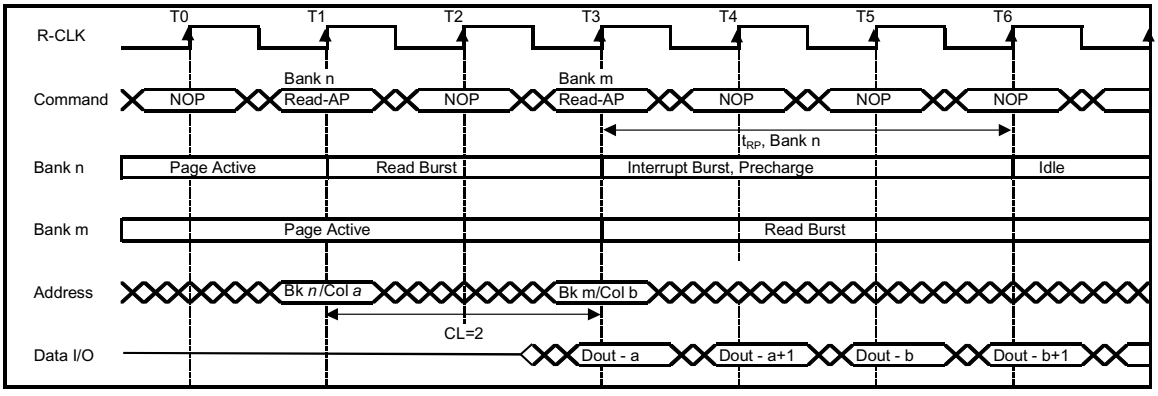


Figure 49. LPSDRAM Read with Auto Precharge to Bank n Interrupted by Write to Bank m

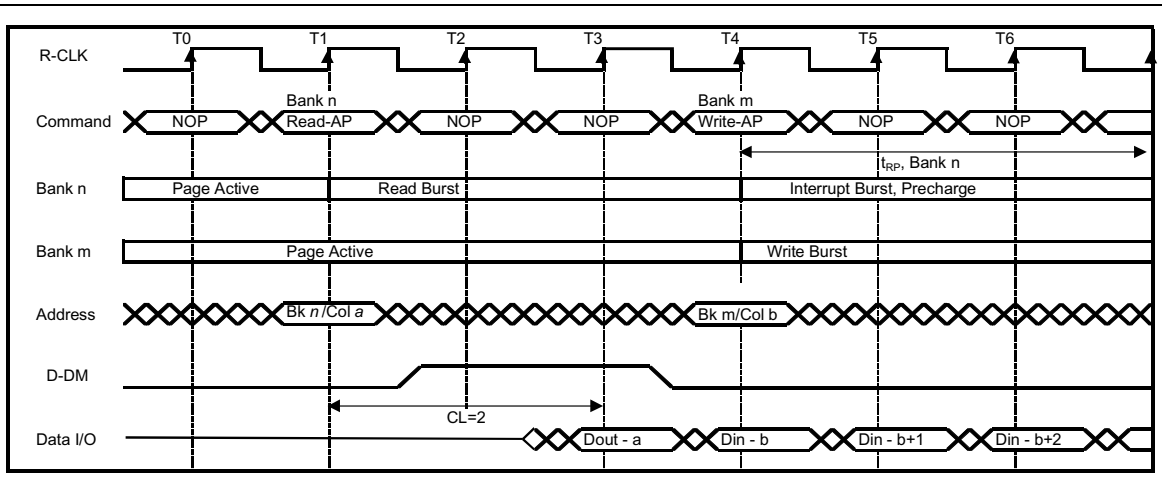


Figure 50. LPSDRAM Write with Auto Precharge to Bank n Interrupted by Read to Bank m

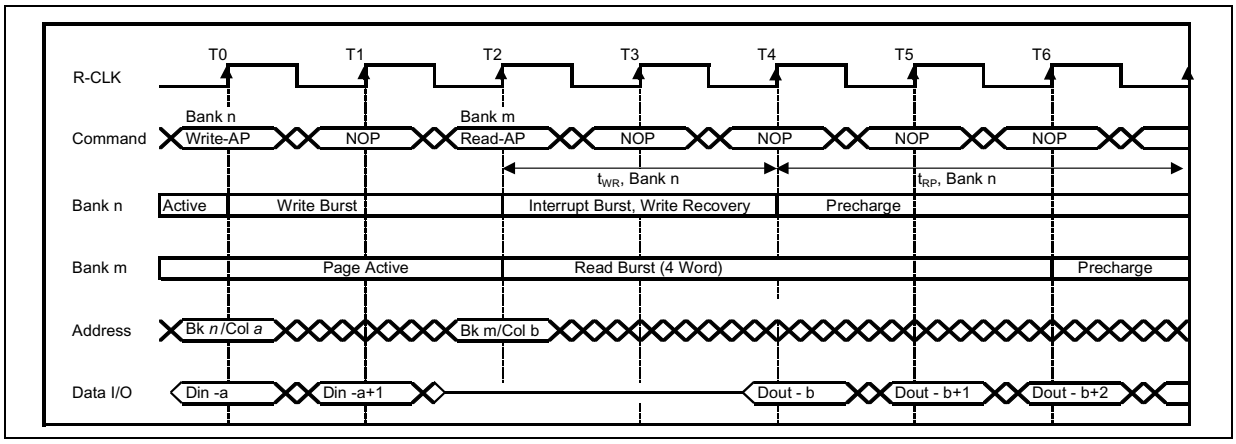
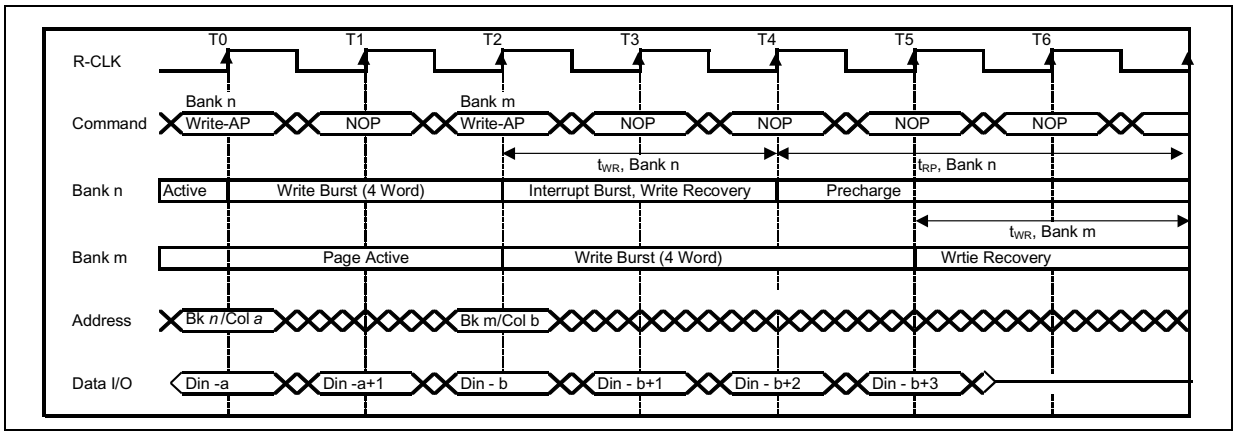


Figure 51. LPSDRAM Write with Auto Precharge to Bank n Interrupted by Write to Bank m



17.11 LPSDRAM Burst Terminate

This command is used to truncate bursts. The most recent command prior to the burst terminate command will be truncated.

17.12 LPSDRAM Auto Refresh

This command is used during normal operation of the LPSDRAM. This command is non-persistent. All banks must be idle before issuing Auto Refresh command. This command can be issued after a minimum of t_{RP} after the precharge command. The address bits are "Don't care" during the Auto Refresh command. As an example, the 256-Mbit LPSDRAM requires 4096 auto refresh cycles (4096 rows/bank) every 64 ms (t_{REF}). Providing a distributed Auto Refresh command every 15.625 µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4096 refresh command cycles can be issued in a burst at a minimum cycle rate (t_{RFC}), once every 64 ms. Figure 32 on page 104 shows auto refresh cycles.

17.13 LPSDRAM Self Refresh

This state retains data in the LPSDRAM, even as the rest of the system is powered down. The Self Refresh command is initiated like the auto refresh command, except the D-CKE is disabled (low). All banks must be idle before this command is issued. Once the Self Refresh command is registered, all inputs become "Don't Care" except D-CKE, which must remain low. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before D-CKE going high. NOP commands should be issued (minimum of 2 clocks) to meet the refresh exit time (t_{SREX}) limitation. Figure 33 on page 104 shows self refresh entry and exit mode.

Flash Flowcharts A

Figure 52. Flash Word Program Flowchart

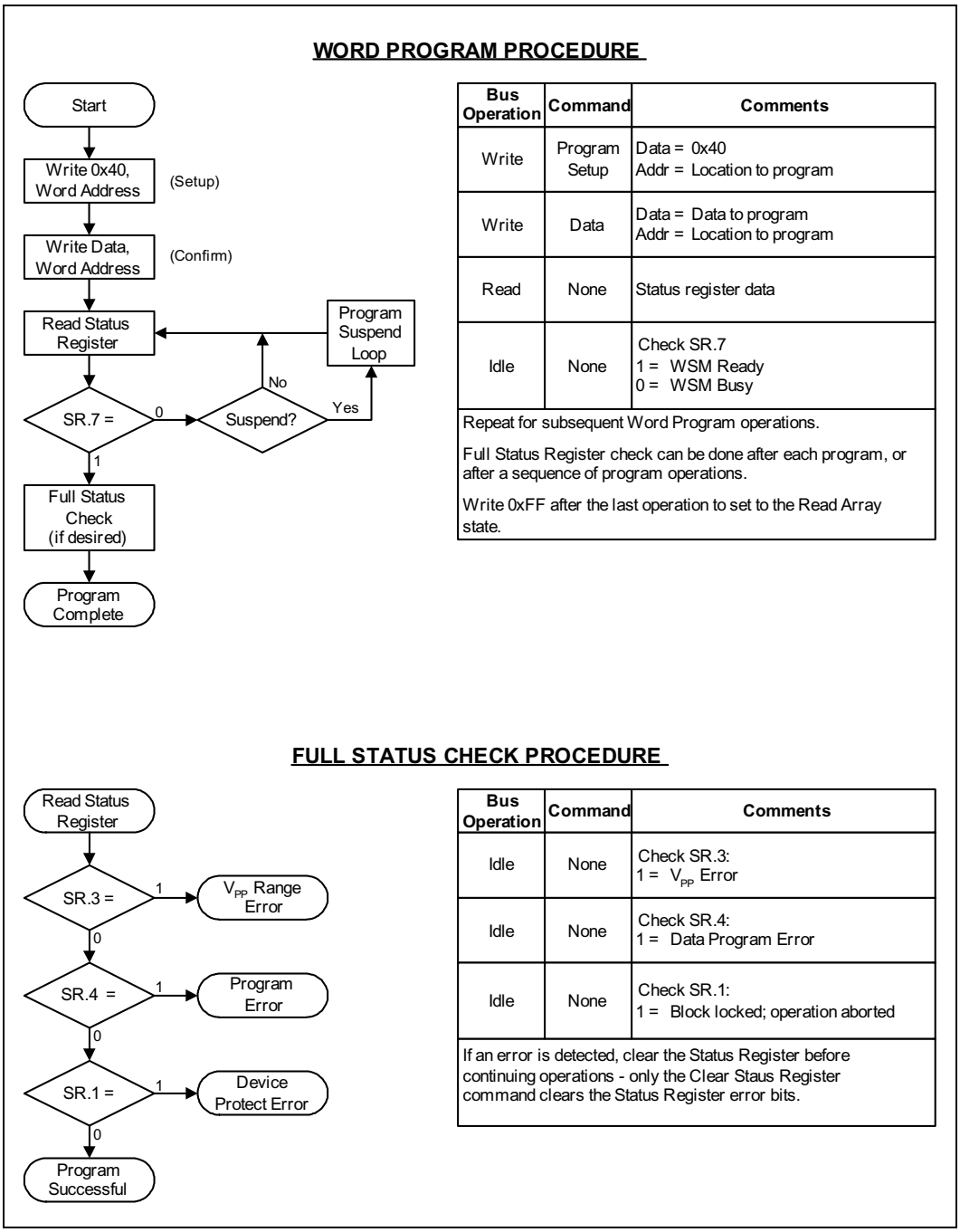
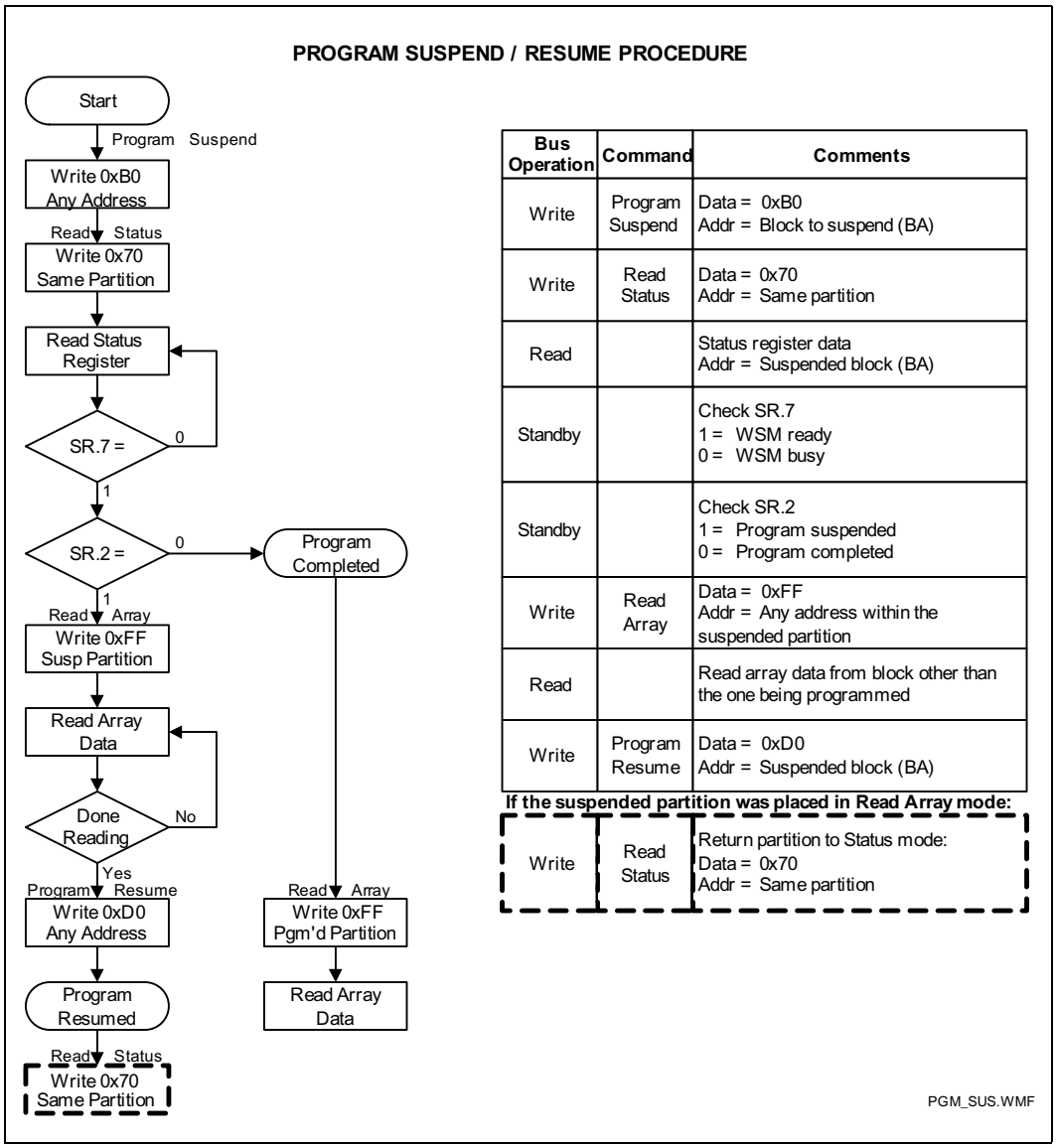


Figure 53. Flash Program Suspend/Resume Flowchart

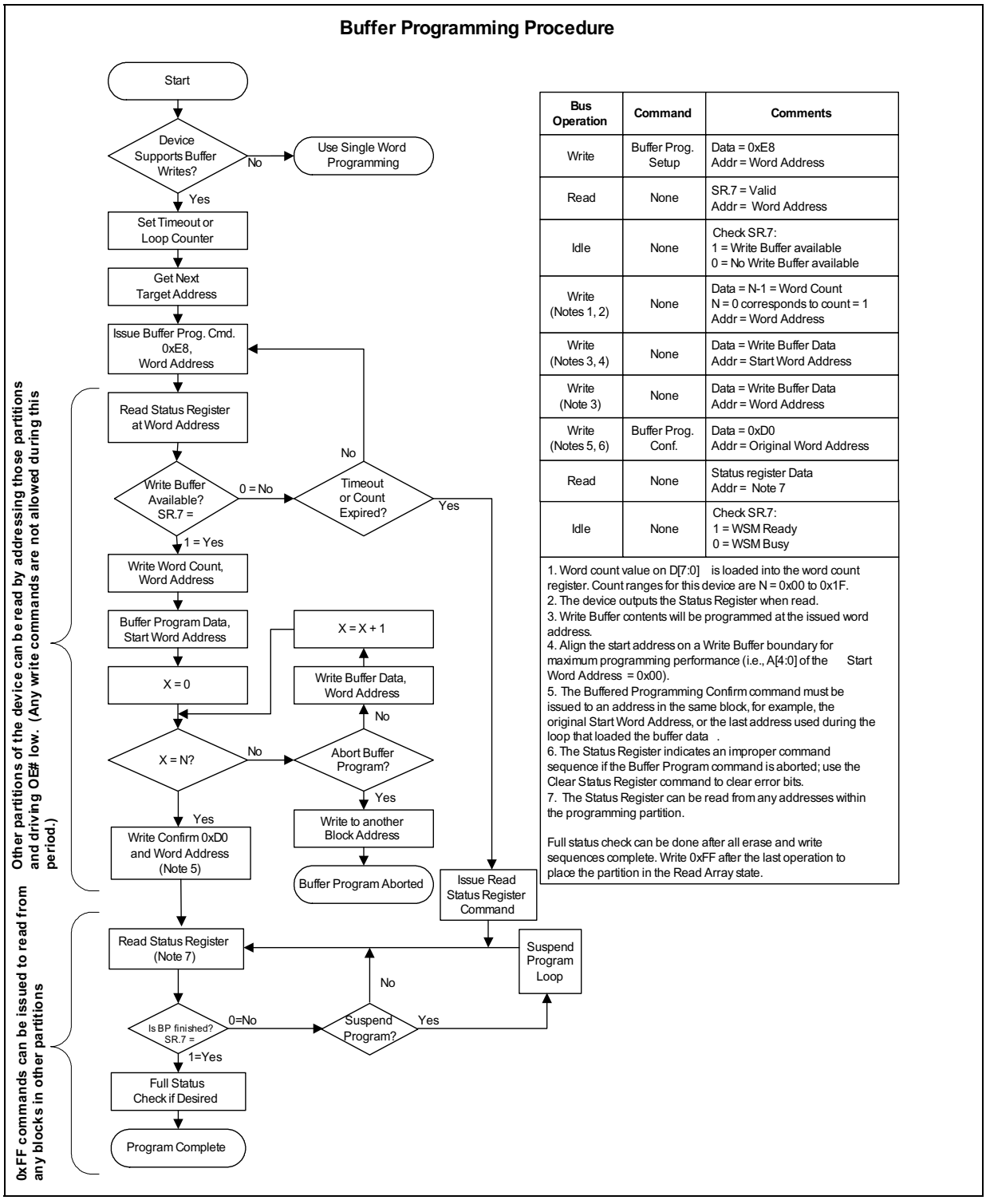


Bus Operation	Command	Comments
Write	Program Suspend	Data = 0xB0 Addr = Block to suspend (BA)
Write	Read Status	Data = 0x70 Addr = Same partition
Read		Status register data Addr = Suspended block (BA)
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = 0xFF Addr = Any address within the suspended partition
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = 0xD0 Addr = Suspended block (BA)

If the suspended partition was placed in Read Array mode:

Write	Read Status	Return partition to Status mode: Data = 0x70 Addr = Same partition

Figure 54. Flash Buffer Program Flowchart

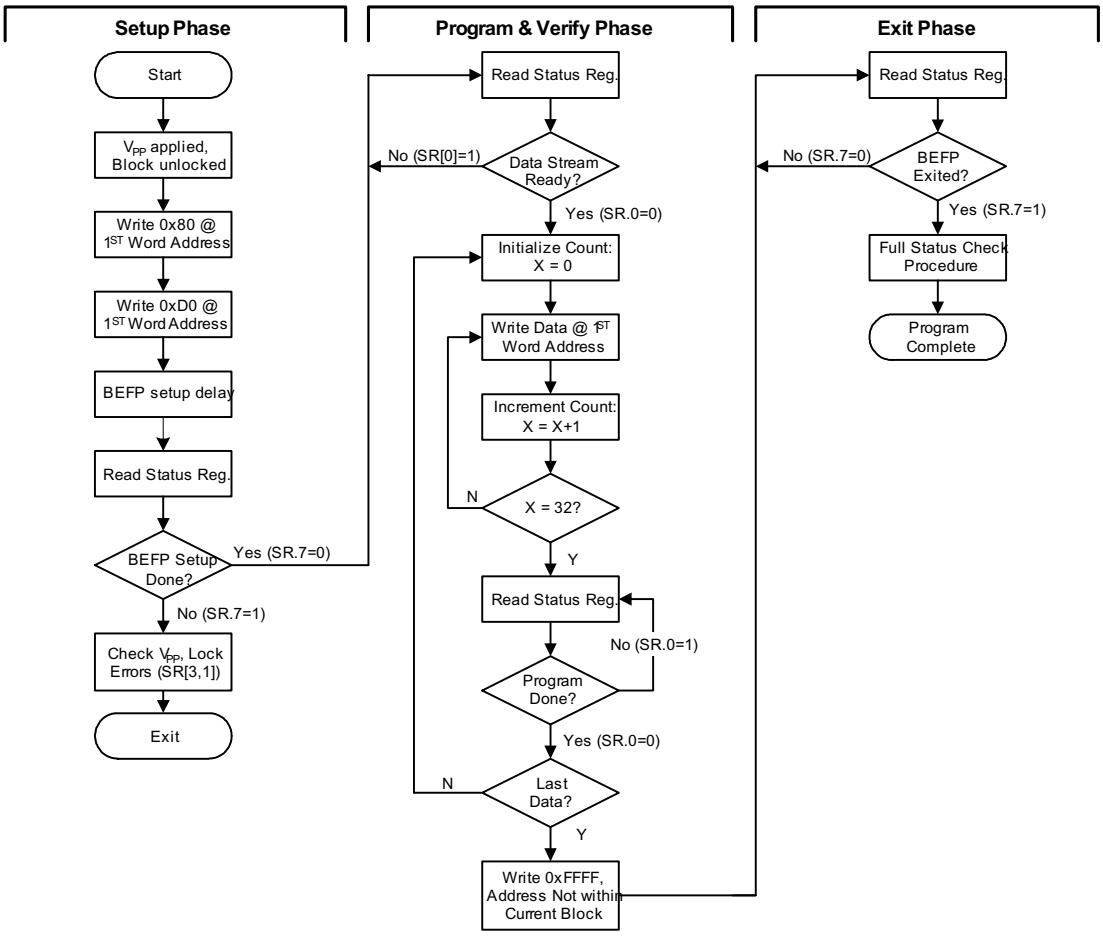


Bus Operation	Command	Comments
Write	Buffer Prog. Setup	Data = 0xE8 Addr = Word Address
Read	None	SR.7 = Valid Addr = Word Address
Idle	None	Check SR.7: 1 = Write Buffer available 0 = No Write Buffer available
Write (Notes 1, 2)	None	Data = N-1 = Word Count N = 0 corresponds to count = 1 Addr = Word Address
Write (Notes 3, 4)	None	Data = Write Buffer Data Addr = Start Word Address
Write (Note 3)	None	Data = Write Buffer Data Addr = Word Address
Write (Notes 5, 6)	Buffer Prog. Conf.	Data = 0xD0 Addr = Original Word Address
Read	None	Status register Data Addr = Note 7
Idle	None	Check SR.7: 1 = WSM Ready 0 = WSM Busy

1. Word count value on D[7:0] is loaded into the word count register. Count ranges for this device are N = 0x00 to 0x1F.
2. The device outputs the Status Register when read.
3. Write Buffer contents will be programmed at the issued word address.
4. Align the start address on a Write Buffer boundary for maximum programming performance (i.e., A[4:0] of the Start Word Address = 0x00).
5. The Buffered Programming Confirm command must be issued to an address in the same block, for example, the original Start Word Address, or the last address used during the loop that loaded the buffer data .
6. The Status Register indicates an improper command sequence if the Buffer Program command is aborted; use the Clear Status Register command to clear error bits.
7. The Status Register can be read from any addresses within the programming partition.

Full status check can be done after all erase and write sequences complete. Write 0xFF after the last operation to place the partition in the Read Array state.

Figure 55. Flash Buffered EFP Flowchart



BEFP Setup

Bus State	Operation	Comments
Write	Unlock Block	V_{PPH} applied to VPP
Write (Note 1)	BEFP Setup	Data = 0x80 @ 1ST Word Address
Write	BEFP Confirm	Data = 0xD0 @1ST Word Address[1]
Read	Status Register	Data = Status Reg. Data Address = 1ST Word Addr
Standby	BEFP Setup Done?	Check SR.7: 0 = BEFP Ready 1 = BEFP Not Ready
Standby	Error Condition Check	If SR.7 is set, check: SR.3 set = V_{PP} Error SR.1 set = Locked Block

BEFP Program & Verify

Bus State	Operation	Comments
Read	Status Register	Data = Status Register Data Address = 1ST Word Addr.
Standby	Data Stream Ready?	Check SR.0: 0 = Ready for Data 1 = Not Ready for Data
Standby	Initialize Count	X = 0
Write (Note 2)	Load Buffer	Data = Data to Program Address = 1ST Word Addr.
Standby	Increment Count	X = X+1
Standby	Buffer Full?	X = 32? Yes = Read SR.0 No = Load Next Data Word
Read	Status Register	Data = Status Reg. data Address = 1ST Word Addr.
Standby	Program Done?	Check SR.0: 0 = Program Done 1 = Program in Progress
Standby	Last Data?	No = Fill buffer again Yes = Exit
Write	Exit Prog & Verify Phase	Data = 0xFFFF @ address not in current block

BEFP Exit

Bus State	Operation	Comments
Read	Status Register	Data = Status Reg. Data Address = 1ST Word Addr
Standby	Check Exit Status	Check SR.7: 0 = Exit Not Completed 1 = Exit Completed

Repeat for subsequent blocks;

After BEFP exit, a full Status Register check can determine if any program error occurred;

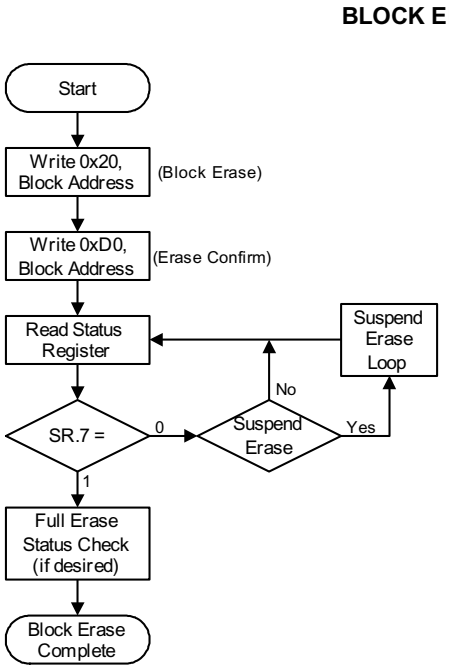
See full Status Register check procedure in the Word Program flowchart.

Write 0xFF to enter Read Array state.

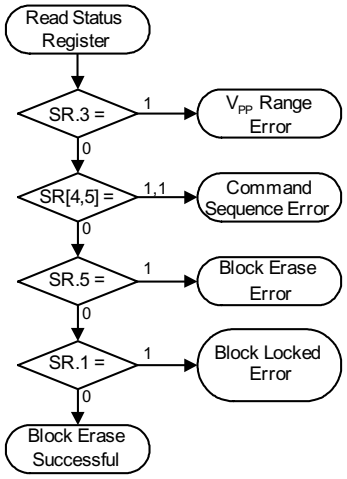
Notes:

1. First-word address to be programmed within the target block must be aligned on a write-buffer boundary.
2. Write-buffer contents are programmed sequentially sequentially to the flash array starting at the first word Address; WSM internally increments addressing.

Figure 56. Flash Block Erase Flowchart

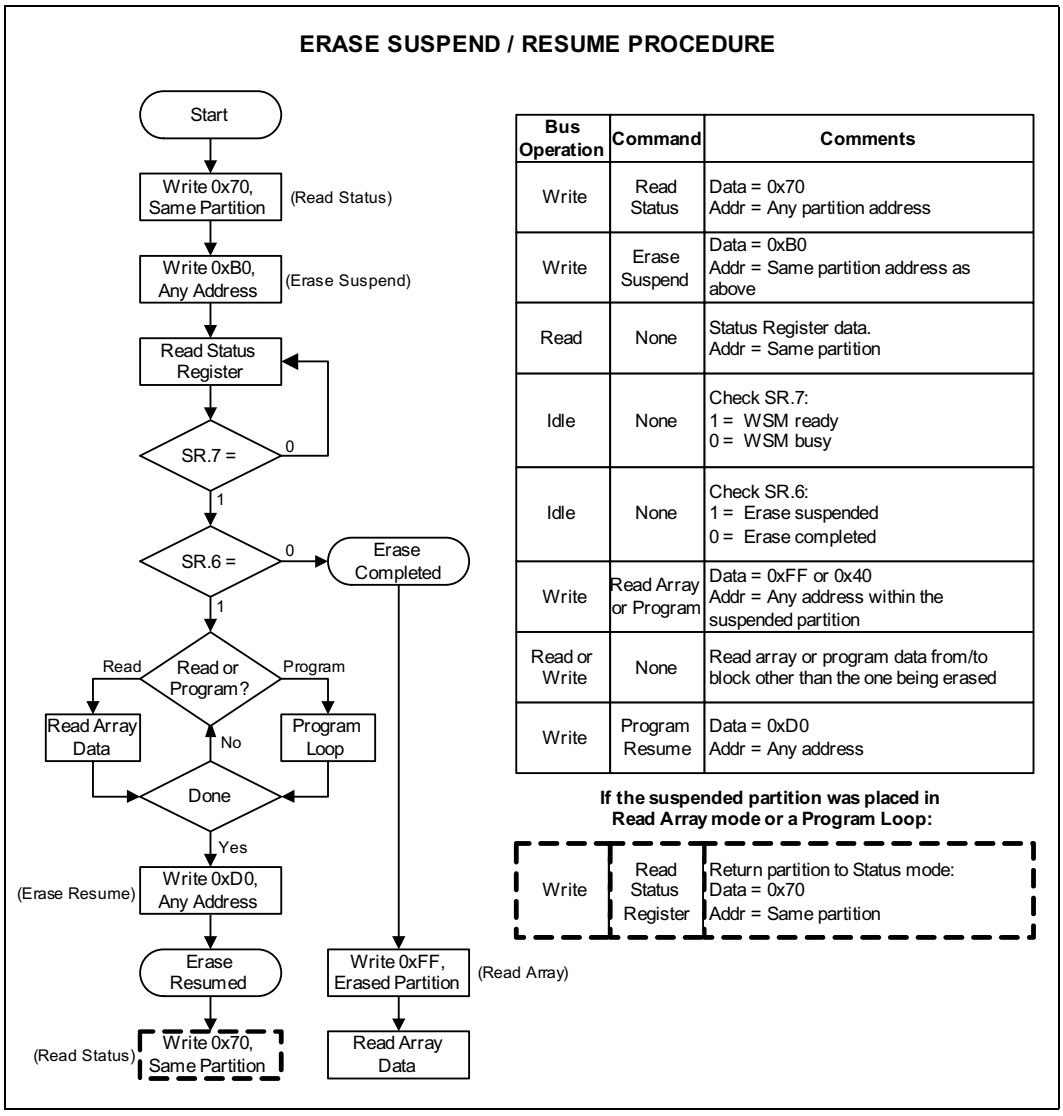


Bus Operation	Command	Comments
Write	Block Erase Setup	Data = 0x20 Addr = Block to be erased (BA)
Write	Erase Confirm	Data = 0xD0 Addr = Block to be erased (BA)
Read	None	Status Register data.
Idle	None	Check SR.7: 1 = WSM ready 0 = WSM busy
Repeat for subsequent block erasures. Full Status register check can be done after each block erase or after a sequence of block erasures. Write 0xFF after the last operation to enter read array mode.		



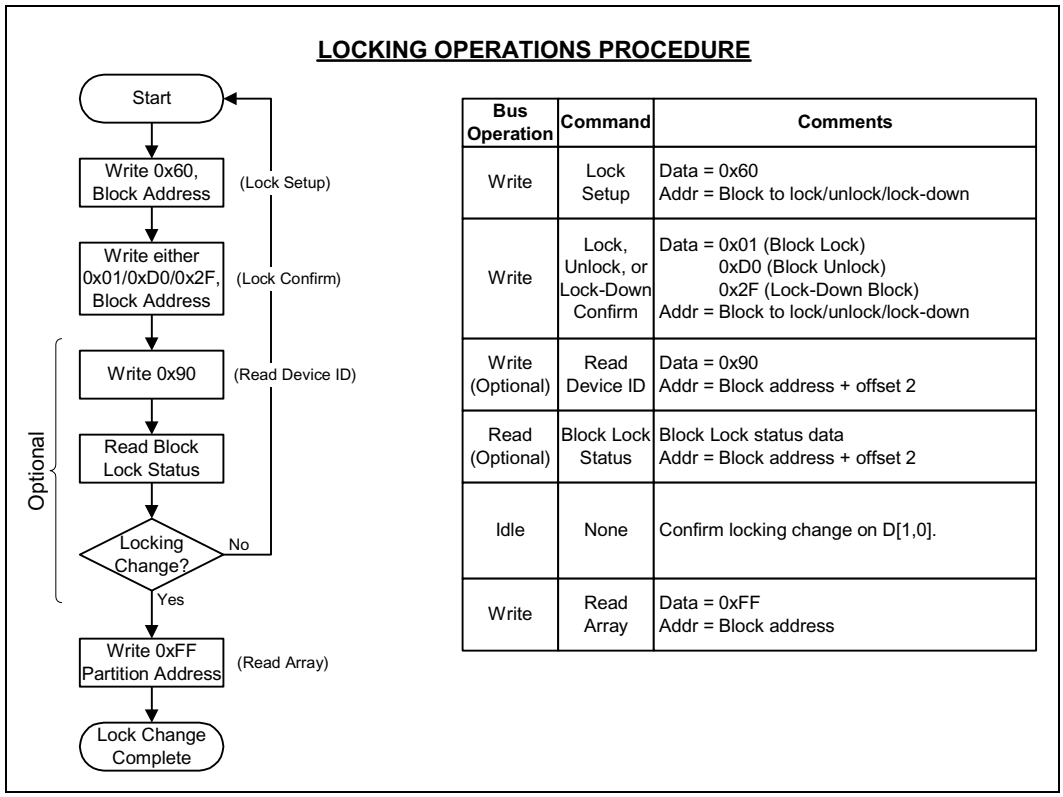
Bus Operation	Command	Comments
Idle	None	Check SR.3: 1 = V_{PP} Range Error
Idle	None	Check SR[4,5]: Both 1 = Command Sequence Error
Idle	None	Check SR.5: 1 = Block Erase Error
Idle	None	Check SR.1: 1 = Attempted erase of locked block; erase aborted.
Only the Clear Status Register command clears SR[1, 3, 4, 5]. If an error is detected, clear the Status register before attempting an erase retry or other error recovery.		

Figure 57. Flash Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Read Status	Data = 0x70 Addr = Any partition address
Write	Erase Suspend	Data = 0xB0 Addr = Same partition address as above
Read	None	Status Register data. Addr = Same partition
Idle	None	Check SR.7: 1 = WSM ready 0 = WSM busy
Idle	None	Check SR.6: 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = 0xFF or 0x40 Addr = Any address within the suspended partition
Read or Write	None	Read array or program data from/to block other than the one being erased
Write	Program Resume	Data = 0xD0 Addr = Any address

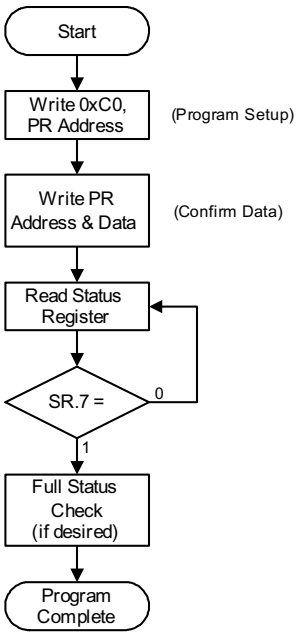
Figure 58. Flash Block Lock Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 0x60 Addr = Block to lock/unlock/lock-down
Write	Lock, Unlock, or Lock-Down Confirm	Data = 0x01 (Block Lock) 0xD0 (Block Unlock) 0x2F (Lock-Down Block) Addr = Block to lock/unlock/lock-down
Write (Optional)	Read Device ID	Data = 0x90 Addr = Block address + offset 2
Read (Optional)	Block Lock Status	Block Lock status data Addr = Block address + offset 2
Idle	None	Confirm locking change on D[1,0].
Write	Read Array	Data = 0xFF Addr = Block address

Figure 59. Flash One-Time Programmable Protection Register Programming Flowchart

PROTECTION REGISTER PROGRAMMING PROCEDURE



Bus Operation	Command	Comments
Write	Program PR Setup	Data = 0xC0 Addr = First Location to Program
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read	None	Status Register Data.
Idle	None	Check SR.7: 1 = WSM Ready 0 = WSM Busy

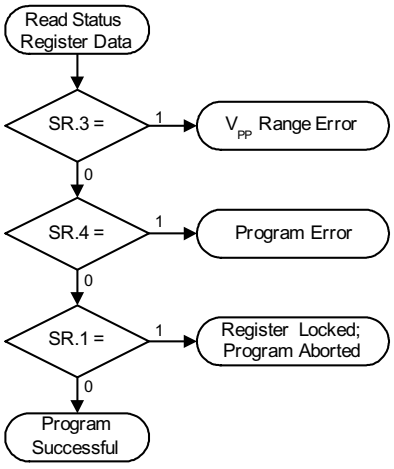
Program Protection Register operation addresses must be within the Protection Register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full Status Register check can be done after each program, or after a sequence of program operations.

Write 0xFF after the last operation to set Read Array state.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Idle	None	Check SR.3: 1 = V_{PP} Range Error
Idle	None	Check SR.4: 1 = Programming Error
Idle	None	Check SR.1: 1 = Block locked; operation aborted

Only the Clear Staus Register command clears SR[1, 3, 4].

If an error is detected, clear the Status register before attempting a program retry or other error recovery.

Common Flash Interface B

The Common Flash Interface (CFI) is part of an overall specification for multiple command-set and control-interface descriptions. This appendix describes the database structure containing the data returned by a read operation after issuing the CFI Query command (see Section 9.2, "Flash Bus Operations" on page 64). System software can parse this database structure to obtain information about the flash, such as block size, density, bus width, and electrical specifications. The system software will then know which command set(s) to use to properly perform flash writes, block erases, reads and otherwise control the flash.

B.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash. This section describes the flash CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (DQ[7:0]) only. The numerical offset value is the address relative to the maximum bus width supported by the flash. For the PXA27x processor memory subsystem, the flash Query table starting address is a 10h, which is a word address for x16 flash.

For a word-wide (x16) flash, the first two Query-structure bytes, ASCII "Q" and "R," appear on the low byte at word addresses 10h and 11h. This CFI-compliant flash outputs 00h data on upper bytes. The flash outputs ASCII "Q" in the low byte (DQ[7:0]) and 0x00 in the high byte (DQ[15:8]).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide flash is always "0x00," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 flash outputs can be assumed to have 0x00 on the upper byte in this mode.

Table 36. Summary of Query Structure Output as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII Value
Device Addresses	00010	51	"Q"
	00011	52	"R"
	00012	59	"Y"

Table 37. Example of Query Structure Output of x16- Flash

Word Addressing:			Byte Addressing:		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_X–A_0	D_{15}–D_0		A_X–A_0	D_7–D_0	
00010h	0051	"Q"	00010h	51	"Q"
00011h	0052	"R"	00011h	52	"R"
00012h	0059	"Y"	00012h	59	"Y"
00013h	P_ID_{LO}	PrVendor	00013h	P_ID_{LO}	PrVendor
00014h	P_ID_{HI}	ID #	00014h	P_ID_{LO}	ID #
00015h	P_{LO}	PrVendor	00015h	P_ID_{HI}	ID #
00016h	P_{HI}	TblAdr	00016h	...	...
00017h	A_ID_{LO}	AltVendor	00017h		
00018h	A_ID_{HI}	ID #	00018h		
...	...	...	...		

B.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or “database.” The structure sub-sections and address locations are summarized in Table 38.

Table 38. Query Structure

Offset	Sub-Section Name	Description(1)
00001-Fh	Reserved	Reserved for vendor-specific information
00010h	CFI query identification string	Command set ID and vendor data offset
0001Bh	System interface information	Device timing & voltage information
00027h	Device geometry definition	Flash device layout

Notes:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of flash bus width and mode.
2. BA = Block Address beginning location (i.e., 08000h is block 1’s beginning location when the block size is 16-KWord).
3. Offset 15 defines “P” which points to the Primary Intel-specific Extended Query Table.

B.3 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 39. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string “QRY“	10: 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--01 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--0A --01	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

Table 40. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--20	2.0V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--85	8.5V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--95	9.5V
1Fh	1	“n” such that typical single word program time-out = 2^n µ-sec	1F:	--08	256µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µ-sec	20:	--09	512µs
21h	1	“n” such that typical block erase time-out = 2^n m-sec	21:	--0A	1s
22h	1	“n” such that typical full chip erase time-out = 2^n m-sec	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--01	512µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--01	1024µs
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--02	4s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

B.4 Flash Geometry Definition

Table 41. Flash Geometry Definition

Offset	Length	Description	Code		
27h	1	"n" such that device size = 2^n in number of bytes	27:	See table below	
28h	2	Flash device interface code assignment: "n" such that n+1 specifies the bit field that represents the flash device width capabilities as described in the table: 7 6 5 4 3 2 1 0 — — — — x64 x32 x16 x8 15 14 13 12 11 10 9 8 — — — — — — — —	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--06 --00	64
2Ch	1	Number of erase block regions (x) within device: 1. x = 0 means no erase blocking; the device erases in bulk 2. x specifies the number of device regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region	2C:	See table below	
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:	See table below	
31h	4	Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	31: 32: 33: 34:	See table below	
35h	4	Reserved for future erase block region information	35: 36: 37: 38:	See table below	

Table 42. Flash Die Geometry Definition

Address	128 Mbit	256 Mbit
	–B	–B
27:	--18	--19
28:	--01	--01
29:	--00	--00
2A:	--06	--06
2B:	--00	--00
2C:	--02	--02
2D:	--03	--03
2E:	--00	--00
2F:	--80	--80
30:	--00	--00
31:	--7E	--FE
32:	--00	--00
33:	--00	--00
34:	--02	--02
35:	--00	--00
36:	--00	--00
37:	--00	--00
38:	--00	--00

B.5 Intel-Specific Extended Query Table

Table 43. Primary Vendor-Specific Extended Query

Offset[1] P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	10A	--50	"P"
(P+1)h		Unique ASCII string “PRI“	10B:	--52	"R"
(P+2)h			10C:	--49	"I"
(P+3)h	1	Major version number, ASCII	10D:	--31	"1"
(P+4)h	1	Minor version number, ASCII	10E:	--33	"3"
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	10F:	--E6	
(P+6)h		*bits 10–31 are reserved; undefined bits are “0.” If bit 31 is*	110:	--03	
(P+7)h		*“1” then another 31 bit field of Optional features follows at*	111:	--00	
(P+8)h		*the end of the bit–30 field.*	112:	--00	
		bit 0 Chip erase supported	bit 0	= 0	No
		bit 1 Suspend erase supported	bit 1	= 1	Yes
		bit 2 Suspend program supported	bit 2	= 1	Yes
		bit 3 Legacy lock/unlock supported	bit 3	= 0	No
		bit 4 Queued erase supported	bit 4	= 0	No
		bit 5 Instant individual block locking supported	bit 5	= 1	Yes
		bit 6 Protection bits supported	bit 6	= 1	Yes
		bit 7 Pagemode read supported	bit 7	= 1	Yes
		bit 8 Synchronous read supported	bit 8	= 1	Yes
		bit 9 Simultaneous operations supported	bit 9	= 1	Yes
(P+9)h	1	Supported functions after suspend: read Array, Status, Query	113:	--01	
		Other supported operations are:			
		bits 1–7 reserved; undefined bits are “0”			
		bit 0 Program supported after erase suspend	bit 0	= 1	Yes
(P+A)h	2	Block status register mask	114:	--03	
(P+B)h		*bits 2–15 are Reserved; undefined bits are “0”*	115:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0	= 1	Yes
		bit 1 Block Lock-Down Bit Status active	bit 1	= 1	Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage	116:	--18	1.8V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 BCD value in volts			
(P+D)h	1	V_{PP} optimum program/erase supply voltage	117:	--90	9.0V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 HEX value in volts			

Table 44. Protection Register Information

Offset[1] P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection fields are available	118:	--02	2
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0–7 = Lock/bytes Jedec-plane physical low address bits 8–15 = Lock/bytes Jedec-plane physical high address bits 16–23 = "n" such that 2^n = factory pre-programmed bytes bits 24–31 = "n" such that 2^n = user programmable bytes	119: 11A: 11B: 11C:	--80 --00 --03 --03	80h 00h 8 byte 8 byte
(P+13)h (P+14)h (P+15)h (P+16)h (P+17)h (P+18)h (P+19)h (P+1A)h (P+1B)h (P+1C)h	10	Protection Field 2: Protection Description Bits 0–31 point to the Protection register physical Lock-word address in the Jedec-plane. Following bytes are factory or user-programmable. bits 32–39 = "n" ∴ n = factory pgm'd groups (low byte) bits 40–47 = "n" ∴ n = factory pgm'd groups (high byte) bits 48–55 = "n" \ 2n = factory programmable bytes/group bits 56–63 = "n" ∴ n = user pgm'd groups (low byte) bits 64–71 = "n" ∴ n = user pgm'd groups (high byte) bits 72–79 = "n" ∴ 2^n = user programmable bytes/group	11D: 11E: 11F: 120: 121: 122: 123: 124: 125: 126:	--89 --00 --00 --00 --00 --00 --00 --10 --00 --04	89h 00h 00h 00h 0 0 0 16 0 16

Table 45. Burst Read Information

Offset[1] P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+1D)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	127:	--03	8 byte
(P+1E)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	128:	--04	4
(P+1F)h	1	Synchronous mode read capability configuration 1 Bits 3–7 = Reserved bits 0–2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the Read Configuration Register bits 0–2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	129:	--01	4
(P+20)h	1	Synchronous mode read capability configuration 2	12A:	--02	8
(P+21)h	1	Synchronous mode read capability configuration 3	12B:	--03	16
(P+22)h	1	Synchronous mode read capability configuration 4	12C:	--07	Cont

Table 46. Partition and Erase-block Region Information

Offset[1] P= 10Ah		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+23)h	(P+23)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	12D:	12D:

Table 47. Partition Region 1 Information

(P+24)h (P+25)h	(P+24)h (P+25)h	Number of identical partitions within the partition region	2	12E: 12F:	12E: 12F:
(P+26)h	(P+26)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	130:	130:
(P+27)h	(P+27)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	131:	131:
(P+28)h	(P+28)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	132:	132:
(P+29)h	(P+29)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) + … + (Type n blocks)x(Type n block sizes)	1	133:	133:
(P+2A)h (P+2B)h (P+2C)h (P+2D)h	(P+2A)h (P+2B)h (P+2C)h (P+2D)h	Partition Region 1 Erase Block Type 1 Information bits 0–15 = y, y+1 = # identical-size erase blks in a partition bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	134: 135: 136: 137:	134: 135: 136: 137:
(P+2E)h (P+2F)h	(P+2E)h (P+2F)h	Partition 1 (Erase Block Type 1) Minimum block erase cycles x 1000	2	138: 139:	138: 139:
(P+30)h	(P+30)h	Partition 1 (erase block Type 1) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved bits 5–7 = reserve for future use	1	13A:	13A:
(P+31)h	(P+31)h	Partition 1 (erase block Type 1) page mode and synchronous mode capabilities defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	13B:	13B:
(P+32)h (P+33)h (P+34)h (P+35)h		Partition Region 1 Erase Block Type 2 Information bits 0–15 = y, y+1 = # identical-size erase blks in a partition bits 16–31 = z, region erase block(s) size are z x 256 bytes (bottom parameter device only)	4	13C: 13D: 13E: 13F:	
(P+36)h (P+37)h		Partition 1 (Erase block Type 2) Minimum block erase cycles x 1000	2	140: 141:	
(P+38)h		Partition 1 (Erase block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved bits 5–7 = reserve for future use	1	142:	
(P+39)h		Partition 1 (Erase block Type 2) pagemode and synchronous mode capabilities defined in Table 10 bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	143:	

Figure 60. Partition Region 2 Information

(P+3A)h (P+3B)h	(P+32)h (P+33)h	Number of identical partitions within the partition region	2	144: 145:	13C: 13D:
(P+3C)h	(P+34)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	146:	13E:
(P+3D)h	(P+35)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	147:	13F:
(P+3E)h	(P+36)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	148:	140:
(P+3F)h	(P+37)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +… + (Type n blocks)x(Type n block sizes)	1	149:	141:
(P+40)h (P+41)h (P+42)h (P+43)h	(P+38)h (P+39)h (P+3A)h (P+3B)h	Partition Region 2 Erase Block Type 1 Information bits 0–15 = y, y+1 = # identical-size erase blks in a partition bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	14A: 14B: 14C: 14D:	142: 143: 144: 145:
(P+44)h (P+45)h	(P+3C)h (P+3D)h	Partition 2 (Erase block Type 1) Minimum block erase cycles x 1000	2	14E: 14F:	146: 147:
(P+46)h	(P+3E)h	Partition 2 (Erase block Type 1) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved bits 5–7 = reserve for future use	1	150:	148:
(P+47)h	(P+3F)h	Partition 2 (erase block Type 1) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	151:	149:
	(P+40)h (P+41)h (P+42)h (P+43)h	Partition Region 2 Erase Block Type 2 Information bits 0–15 = y, y+1 = # identical-size erase blks in a partition bits 16–31 = z, region erase block(s) size are z x 256 bytes	4		14A: 14B: 14C: 14D:
	(P+44)h (P+45)h	Partition 2 (Erase block Type 2) Minimum block erase cycles x 1000	2		14E: 14F:
	(P+46)h	Partition 2 (Erase block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved bits 5–7 = reserve for future use	1		150:
	(P+47)h	Partition 2 (erase block Type 2) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1		151:

Table 48. Flash Die Partition and Erase Block Region Information

Address	128 Mbit	256 Mbit
	–B	–B
12D:	--02	--02
12E:	--01	--01
12F:	--00	--00
130:	--11	--11
131:	--00	--00
132:	--00	--00
133:	--02	--02
134:	--03	--03
135:	--00	--00
136:	--80	--80
137:	--00	--00
138:	--64	--64
139:	--00	--00
13A:	--02	--02
13B:	--03	--03
13C:	--06	--0E
13D:	--00	--00
13E:	--00	--00
13F:	--02	--02
140:	--64	--64
141:	--00	--00
142:	--02	--02
143:	--03	--03
144:	--0F	--0F
145:	--00	--00
146:	--11	--11
147:	--00	--00
148:	--00	--00
149:	--01	--01
14A:	--07	--0F
14B:	--00	--00
14C:	--00	--00
14D:	--02	--02
14E:	--64	--64
14F:	--00	--00
150:	--02	--02
151:	--03	--03

PXA27x Processor Memory Subsystem RAM Type ID C

This field provides a means to identify a particular RAM type via software during both the engineering sample and production phases. The following PXA27x processor memory subsystem product information will be hard-coded at address 0x76 in the CFI space. This methodology shall be used for all subsequent PXA27x processor memory subsystem products.

Note: All 16 bits of the data bus are used in this field.

Table 49. PXA27x Processor Memory Subsystem RAM Type ID Field Description

CFI Offset	Description	Notes
0x76	Bits 15:0 correspond to the defined Revision ID field	This field shall only be used in PXA27x processor memory subsystem products, and wil be located at offset 0x76
	Bits 15:13 = RAM Density • 000b: No RAM (default) • 001b: 128-Mbit • 010b: 256-Mbit • 011b: 512-Mbit • 100b: 1-Gbit • 101b: 2-Gbit • 110b: 4-Gbit • 111b: Reserved	Bit 15:13 describe the total RAM density used in the PXA27x processor memory subsystem products. • Total RAM density could be from a single monolithic die, or made up of multiple RAM dies stacked to equate to a high density.
	Bits 12:11 = RAM Type • 00b: No RAM (default) • 01b: LPSDRAM • 10b: LPDDR RAM • 11b: Reserved	Bit 12:11 describe the RAM type used in the PXA27x processor memory subsystem products. • Valid RAM type options: LPSDRAM or LPDDR RAM. • RAM types not listed are not available.
	Bit 10 = Bus Width • 00b: 16-bits (default) • 01b: 32-bits • 10b: Reserved • 11b: Reserved	Bit 10 describe the bus width of the RAM type used in the PXA27x processor memory subsystem products.
	Bits 9:8 = Number of Banks • 00b: No RAM (default) • 01b: 4 Banks • 10b: Reserved • 11b: Reserved	Bit 9:8 describe the number of banks available in the RAM used in the PXA27x processor memory subsystem products.
	Bits 7:6 = Number of Rows • 00b: No RAM (default) • 01b: 12 Rows • 10b: 13 Rows • 11b: 14 Rows	Bit 7:6 describe the number of rows available in the RAM used in the PXA27x processor memory subsystem products.
0x76	Bit 5:4 = Number of Columns • 00b: No RAM (default) • 01b: 7 Columns • 10b: 8 Columns • 11b: 9 Columns	Bit 5:4 describe the number of columns available in the RAM used in the PXA27x processor memory subsystem products.
	Bits 3:2 = RAM Bus Clock Speed • 00b: No RAM (default) • 01b: 104 MHz • 10b: 133 MHz • 11b: 266 MHz	Bit 3:2 describe the RAM clock speed option available to used in the PXA27x processor memory subsystem products.
	Bits 1:0 = Reserved	Bit 1:0 is reserved for future use. The default setting is 0x00.

Additional Information D

Order Number	Document
280000	Intel® PXA27x Family Developer's Manual
280001	Intel® PXA27x Family Design Guide
280003	Intel® PXA27x Family Electrical, Mechanical, and Thermal Specification
280004	Intel® PXA27x Family Optimization Guide

Notes:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel® PXA27x Processor or Memory Subsystem, refer to http://developer.intel.com/design/pca/prodbref/253820.htm

Ordering Introduction E

Figure 61. Intel® PXA27x MCP Product Decoder