

*256K x 16 Bit CMOS Dynamic RAM with Extended Data Out***DESCRIPTION**

This is a family of 262,144 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in Low power version.

This 256Kx16 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
 - KM416C254B/BL (5V, 512 Ref.)
 - KM416V254B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	255	495
-7	235	440
-8	220	-

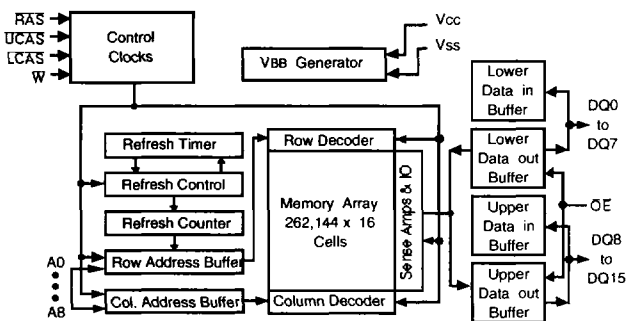
- Extended Data Out operation
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V $\pm$ 10% power supply (5V product)
- Triple +3.3V $\pm$ 0.3V power supply (3.3V product)

- Refresh cycles

Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C254B	5V	512	8ms	128ms
V254B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	17ns	84ns	20ns	5V Only
-6	60ns	17ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

FUNCTIONAL BLOCK DIAGRAM

SAMSUNG ELECTRONIC CO., LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• KM416C/V254BJ

VCC	1	40	Vss
DQ0	2	39	DQ15
DQ1	3	38	DQ14
DQ2	4	37	DQ13
DQ3	5	36	DQ12
VCC	6	35	Vss
DQ4	7	34	DQ11
DQ5	8	33	DQ10
DQ6	9	32	DQ9
DQ7	10	31	DQ8
N.C	11	30	N.C
N.C	12	29	LCAS
W	13	28	UCAS
RAS	14	27	OE
N.C	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
VCC	20	21	Vss

(SOJ)

• KM416C/V254BT

VCC	1	40	Vss
DQ0	2	39	DQ15
DQ1	3	38	DQ14
DQ2	4	37	DQ13
DQ3	5	36	DQ12
VCC	6	35	Vss
DQ4	7	34	DQ11
DQ5	8	33	DQ10
DQ6	9	32	DQ9
DQ7	10	31	DQ8
N.C	11	30	N.C
N.C	12	29	LCAS
W	13	28	UCAS
RAS	14	27	OE
N.C	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
VCC	20	21	Vss

(TSOP(II)-Forward Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.1	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1.0 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other pins not under test=0V)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V, (Any input 0≤V _{IN} ≤V _{CC} +0.5V, all other pins not under test=0V)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V254B	KM416C254B	
I _{CC1}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I _{CC2}	Don't care	Don't care	1	2	mA
I _{CC3}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I _{CC4}	Don't care	-5	-	70	mA
		-6	60	60	mA
		-7	55	50	mA
		-8	50	-	mA
I _{CC5}	Normal L	Don't care	0.5	1	mA
			100	150	μA
I _{CC6}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
		-8	60	-	mA
I _{CC7}	L	Don't care	200	300	μA
I _{CCS}	L	Don't care	100	200	μA

I_{CC1}* : Operating current (**RAS**, **UCAS**, **LCAS**, Address cycling @t_{RC}=min.)I_{CC2} : Standby current (**RAS**=**UCAS**=**LCAS**=**W**=V_{IH})I_{CC3}* : **RAS**-only refresh current (**UCAS**=**LCAS**=V_{IH}, **RAS**, Address cycling @t_{RC}=min.)I_{CC4}* : Hyper Page Mode current (**RAS**=V_{IL}, **UCAS** or **LCAS**, Address cycling @t_{HPC}=min.)I_{CC5} : Standby current (**RAS**=**UCAS**=**LCAS**=**W**=V_{CC}-0.2V)I_{CC6}* : **CAS**-before-**RAS** Refresh current (**RAS**, **UCAS** or **LCAS** cycling @t_{RC}=min.)I_{CC7} : Battery back-up current, Average power supply current, Battery back-up modeInput high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, **UCAS**, **LCAS**= 0.2VDin = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RASmin}~300 nsI_{CCS} : Self refresh current**RAS**=**UCAS**=**LCAS**=V_{IL}, **W**=**OE**=A0 ~ A8 = V_{CC}-0.2V or 0.2V,DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while **RAS**=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, t_{HPC}.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, See note 1,2)Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$ Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.1/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	84		104		124		144		ns	
Read-modify-write cycle time	t _{RWC}	116		140		165		190		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		17		17		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	3		3		3		3		ns	3
Output Buffer turn-off delay from $\overline{\text{CAS}}$	t _{CEZ}	3	13	3	15	3	20	3	20	ns	6, 13
Transition time (rise and fall)	t _T	2	50	2	50	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	17		17		20		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	40		50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	33	20	43	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		0		ns	14
Column address hold time (5V)	t _{CAH}	8		10		15		-		ns	14
Column address hold time (3.3V)	t _{CAH}	-		15		15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		35		40		ns	
Read command set-up time	t _{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		0		ns	8
Write command set-up time	t _{WCS}	0		0		0		0		ns	7
Write command hold time	t _{WCH}	10		10		10		10		ns	
Write command pulse width	t _{WP}	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	8		10		15		20		ns	17

Note) *1: 50ns product : $V_{CC}=5\text{V} \pm 5\%$, *2 : 3.3V only

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, See note 1,2)

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9,20
Data hold time (5V)	tDH	8		10		15		-		ns	9,20
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128 ¹		128		128		128	ms	
CAS to W delay time	tCWD	34		36		44		44		ns	7,16
RAS to W delay time	tRWD	67		79		94		104		ns	7
Column address to W delay time	tAWD	42		49		59		64		ns	7
CAS precharge to W delay time	tCPWD	45		54		64		69		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	5		5		5		5		ns	18
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		10		ns	19
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (CBR counter test cycle)	tCPT	20		20		25		30		ns	
Access time from CAS precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
CAS precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	15
RAS pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		15		15		20		20	ns	3
OE to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	3	13	3	15	3	20	3	20	ns	6
OE command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from W	tWEZ	3	13	3	15	3	20	3	20	ns	6
W to data delay	tWED	13		15		20		20		ns	
OE to CAS hold time	tOCH	5		5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		5		ns	
OE precharge time	tOEP	5		5		5		5		ns	
W pulse width (Hyper page cycle)	tWPE	5		5		5		5		ns	
RAS pulse width (C-B-R self refresh)	tRASS	100		100		100		100		μs	12
RAS precharge time (C-B-R self refresh)	tRPS	90		110		130		150		ns	12
CAS hold time (C-B-R self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 50ns product : V_{CC}=5V±5%, *2 : 3.3V only

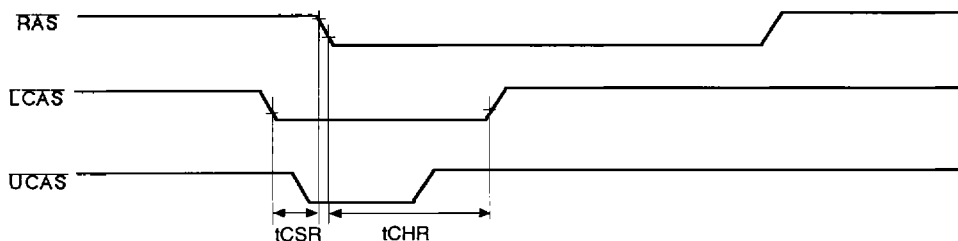
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
11. $t_{ASC} \geq 6ns$, Assume $t_T = 2.0ns$.

KM416C/V254B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 - DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

12. For all of the refresh modes except for distributed $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ refresh, 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
14. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
15. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
16. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
17. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
18. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
19. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



20. t_{DS} , t_{DH} is independently specified for lower byte $\text{D}_{\text{IN}}(0\sim7)$, upper byte $\text{D}_{\text{IN}}(8\sim15)$.