

1M x 32Bit x 4 Banks SDRAM in 90FBGA

FEATURES

- 3.0V & 3.3V power supply
- LVCMOS compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (1, 2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- EMRS cycle with address key programs.
 - PASR(Partial Array Self Refresh)
 - Internal TCSR(Temperature Compensated Self Refresh)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle).
- Extended Temperature Operation (-25°C ~ 85°C).
- Commercial Temperature Operation (-25°C ~ 70°C).
- 90Balls Monolithic FBGA(11mm x 13mm)
- Pb for -SXXX, Pb Free for -DXXX.

GENERAL DESCRIPTION

The K4S283233E is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

ORDERING INFORMATION

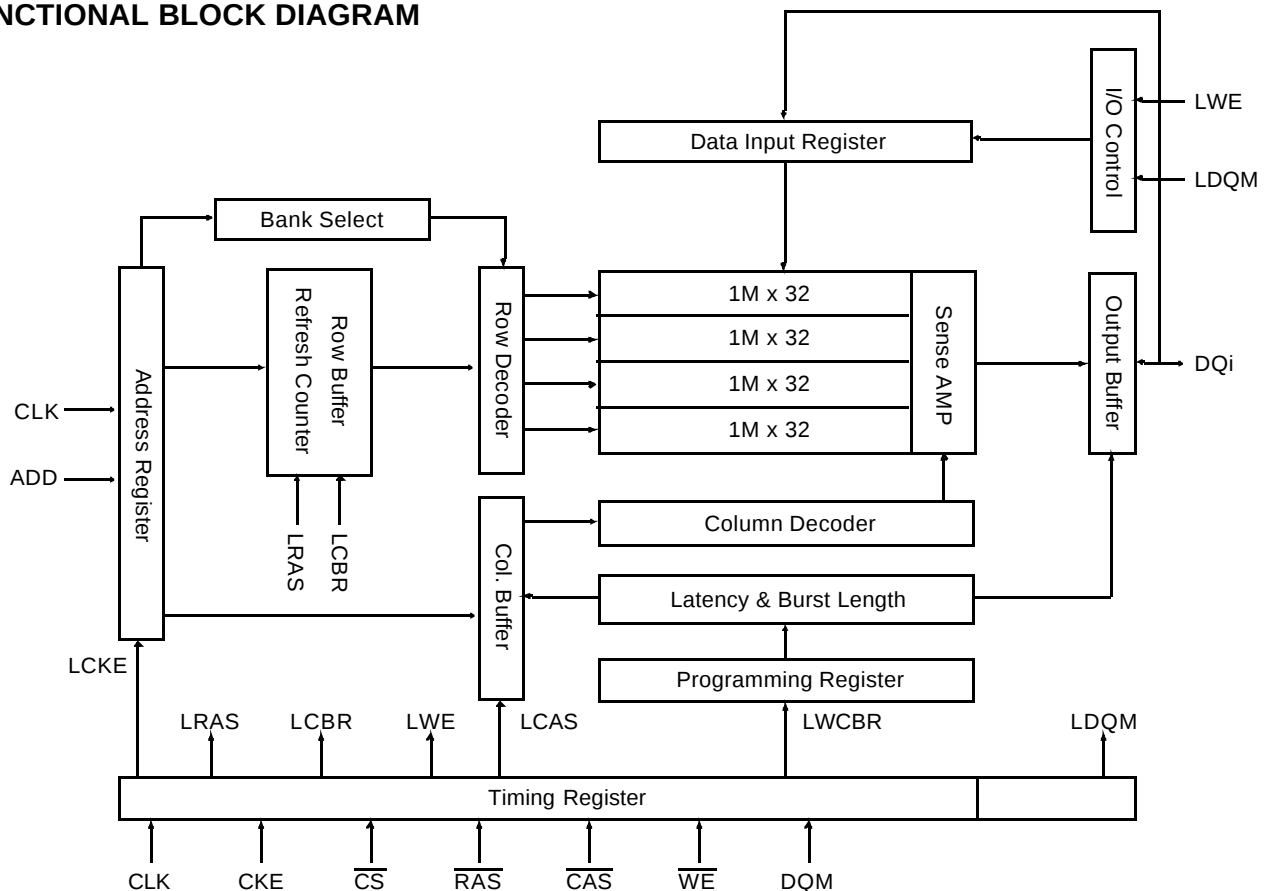
Part No.	Max Freq.	Interface	Package
K4S283233E-S(D)E/N/G/C/L/F60	166MHz(CL=3)	LVCMOS	90FBGA Pb (Pb Free)
K4S283233E-S(D)E/N/G/C/L/F75	133MHz(CL=3) 105MHz(CL=2)		
K4S283233E-S(D)E/N/G/C/L/F1H	105MHz(CL=2)		
K4S283233E-S(D)E/N/G/C/L/F1L	105MHz(CL=3) ^{*1}		

- S(D)E/N/G : Normal/Low Power, Extended Temperature.

- S(D)C/L/F : Normal/Low Power, Commercial Temperature.

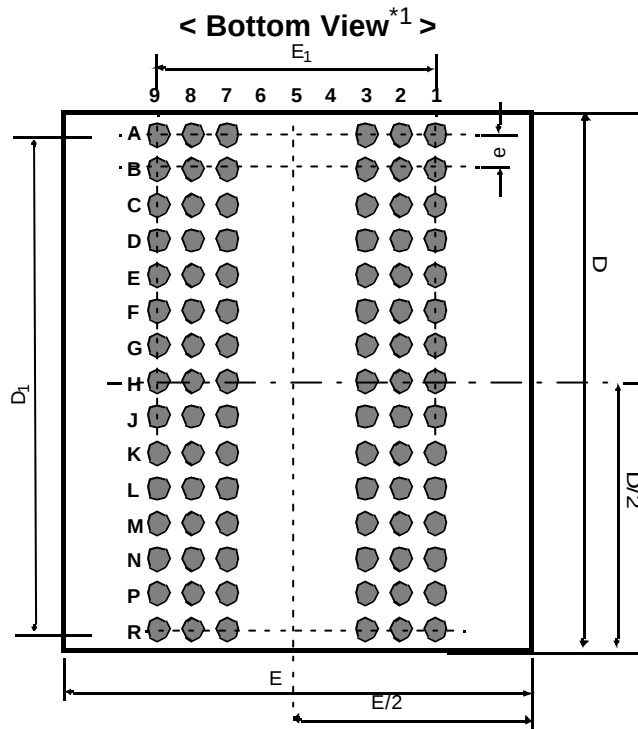
Note : 1. In case of 40MHz Frequency, CL1 can be supported.

FUNCTIONAL BLOCK DIAGRAM



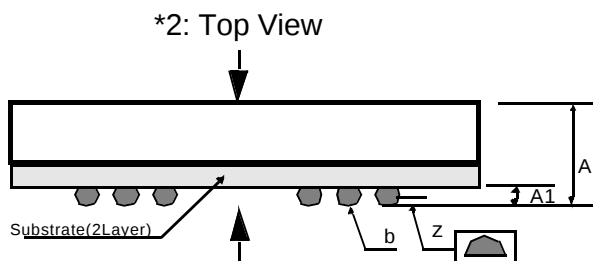
* Samsung Electronics reserves the right to change products or specification without notice.

Package Dimension and Pin Configuration



< Top View ^{*2} >

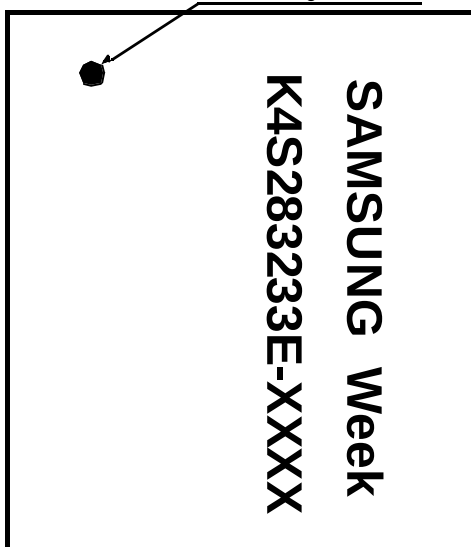
90Ball(6x15) CSP						
	1	2	3	7	8	9
A	DQ26	DQ24	VSS	VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ	VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25	DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30	DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC	NC	DQ16	VSSQ
F	VSS	DQM3	A3	A2	DQM2	VDD
G	A4	A5	A6	A10	A0	A1
H	A7	A8	NC	NC	BA1	A11
J	CLK	CKE	A9	BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC	$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS	VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9	DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14	DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ	VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS	VDD	DQ0	DQ2



*1: Bottom View

< Top View ^{*2} >

#A1 Ball Origin Indicator



Pin Name	Pin Function
CLK	System Clock
$\overline{CS}$	Chip Select
CKE	Clock Enable
A0 ~ A11	Address
BA0 ~ BA1	Bank Select Address
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ DQM3	Data Input/Output Mask
DQ0 ~ 31	Data Input/Output
VDD/VSS	Power Supply/Ground
VDDQ/VSSQ	Data Output Power/Ground

[Unit:mm]

Symbol	Min	Typ	Max
A	1.35	1.40	1.45
A1	0.30	0.35	0.40
E	-	11.00	-
E1	-	6.40	-
D	-	13.00	-
D1	-	11.20	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = -25 to 85°C for Extended, -25 to 70°C for Commercial)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	2.7	3.0	3.6	V	
	V _{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V _{IH}	2.2	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.5	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes :

1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.0V & 3.3, T_A = 23°C, f = 1MHz, V_{REF} = 0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	-	4.0	pF	
RAS, CAS, WE, CS, CKE, DQM ₀ ~ DQM ₃	C _{IN}	-	4.0	pF	
Address(A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{ADD}	-	4.0	pF	
DQ ₀ ~ DQ ₃₁	C _{OUT}	-	6.0	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85°C for Extended, -25 to 70°C for Commercial)

Parameter	Symbol	Test Condition		Version				Unit	Note	
				-60	-75	-1H	-1L			
Operating Current (One Bank Active)	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC} (min) I _O = 0 mA		100	85	85	80	mA	1	
Precharge Standby Current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = 10ns		0.5				mA		
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞		0.5						
Precharge Standby Current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{\text{CS}} \geq V_{IH}(\text{min})$, t _{CC} = 10ns Input signals are changed one time during 20ns		16				mA		
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable		8						
Active Standby Current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), t _{CC} = 10ns		5				mA		
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞		5						
Active Standby Current in non power-down mode (One Bank Active)	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{\text{CS}} \geq V_{IH}(\text{min})$, t _{CC} = 10ns Input signals are changed one time during 20ns		26				mA		
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable		22				mA		
Operating Current (Burst Mode)	I _{CC4}	I _O = 0 mA Page burst 4Banks Activated t _{CCD} = 2CLKs		110	85	80	80	mA	1	
Refresh Current	I _{CC5}	t _{RC} ≥ t _{RC} (min)		180	160	150	130	mA	2	
Self Refresh Current	I _{CC6}	CKE ≤ 0.2V	-S(D)E/C		1500			uA	4	
			-S(D)N/L		800				5	
			Internal TCSR		Max 40		Max 85/70		°C	3
			-S(D)G/F	4 Banks	500		800		uA	6
				2 Banks	460		650			
			1 Bank	440		550				

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Internal TCSR can be supported.

In Commercial Temp : Max 40°C/Max 70°C, In Extended Temp : Max 40°C/Max 85°C

4. K4S283233E-S(D)E/C**

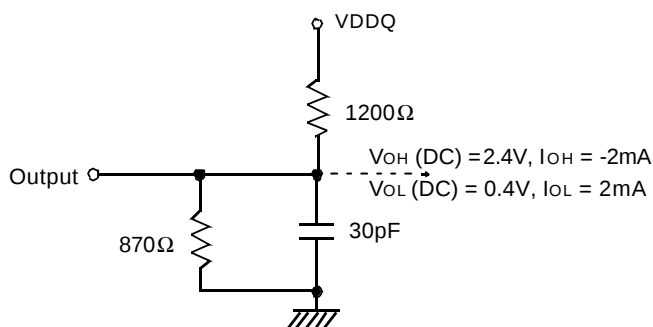
5. K4S283233E-S(D)N/L**

6. K4S283233E-S(D)G/F**

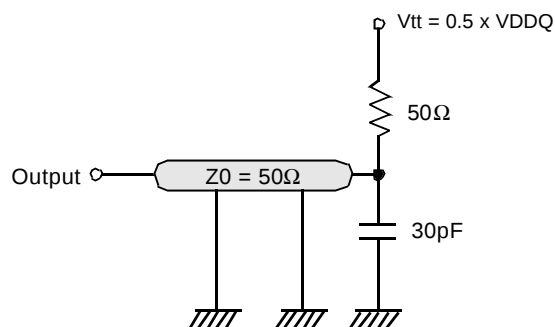
7. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS ($V_{DD} = 2.7V \sim 3.6V$, $T_A = -25$ to $85^\circ C$ for Extended, -25 to $70^\circ C$ for Commercial)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4 / 0.4	V
Input timing measurement reference level	$0.5 \times V_{DDQ}$	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	$0.5 \times V_{DDQ}$	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			- 60	- 75	-1H	-1L		
Row active to row active delay		tRRD(min)	12	15	19	19	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	18	19	19	24	ns	1
Row precharge time		tRP(min)	18	19	19	24	ns	1
Row active time		tRAS(min)	42	45	50	60	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	60	64	69	84	ns	1
Last data in to row precharge		tRDL(min)	2				CLK	2,3
Last data in to Active delay		tDAL(min)	tRDL + tRP				-	3
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	4
Number of valid output data	CAS latency=3		2				ea	5
	CAS latency=2		-	1				
	CAS latency=1		-		0			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. Minimum $2RDL=2CLK$ and $t_{DAL}(=t_{RDL} + t_{RP})$ is required to complete both of last data write command(t_{RDL}) and precharge command(t_{RP}).
 4. All parts allow every cycle column address change.
 5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 60		- 75		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t _{CC}	6.0	1000	7.5	1000	9.5	1000	9.5	1000	ns	1
	CAS latency=2		-		9.5		9.5		12			
	CAS latency=1		-		-		-		25			
CLK to valid output delay	CAS latency=3	t _{SAC}		5.4		6		7		7	ns	1,2
	CAS latency=2			-		7		7		8		
	CAS latency=1			-		-		-		20		
Output data hold time	CAS latency=3	t _{OH}	2.5		2.5		2.5		2.5		ns	2
	CAS latency=2		-		2.5		2.5		2.5			
	CAS latency=1		-		-		-		2.5			
CLK high pulse width		t _{CH}	2.5		2.5		3		3		ns	3
CLK low pulse width		t _{CL}	2.5		2.5		3		3		ns	3
Input setup time		t _{SS}	2.0		2.0		2.5		2.5		ns	3
Input hold time		t _{SH}	1.0		1.0		1.5		1.5		ns	3
CLK to output in Low-Z		t _{SLZ}	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t _{SHZ}		5.4		6		7		7	ns	
	CAS latency=2			-		7		7		8		
	CAS latency=1			-		-		-		20		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A ₀ ~ A ₇)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A ₀ ~ A ₇)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes :

- OP Code : Operand Code
A₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA₀ ~ BA₁ : Bank select addresses.
- During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1	A11 ~ A10/AP	A9 ^{*2}	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU ^{*1}	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

* Full Page Length

64Mb : x16(256) / x32(256), 128Mb : x16(512) / x32(256), 256Mb : x16(512) / x32(512), 512Mb : x16(1024) / x32(512)

Register Programmed with Extended MRS

Address	BA1	BA0	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU ^{*1}								PASR		

Extended MRS for PASR(Partial Array Self Refresh)

Mode Select								PASR ^{*3,4}				
BA1	BA0	Mode						A2	A1	A0	# of Banks	
0	0	Normal MRS						0	0	0	4 Banks(All Banks)	
0	1	Reserved						0	0	1	2 Banks(1/2 of All Banks)	
1	0	EMRS for Mobile SDRAM						0	1	0	1 Bank(1/4 of All Banks)	
1	1	Reserved						0	1	1	Reserved	
Reserved Address ^{*1}								1	0	0	Reserved	
A11~A10/AP		A9	A8	A7	A6	A5	A4	A3	1	0	1	Reserved
0		0	0	0	0	0	0	0	1	1	0	Reserved
									1	1	1	Reserved

- Notes :** 1. RFU(Reserved for future use) should stay "0" during MRS cycle.
 2. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
 3. In case of 1 Bank Partial Refresh, one bank(BA1=BA0=0) is selected.
 In case of 2 Banks Partial Refresh, two banks(BA1=0) are selected.
 4. Mobile SDRAM supports PASR of 4 Banks(128Mb), 2 Banks(64Mb) and 1Bank(32Mb).

Partial Array Self Refresh

1. In order to save power consumption, Mobile SDRAM has PASR option.
2. Mobile SDRAM supports 3 kinds of PASR in self refresh mode ; 4 Banks(128Mb), 2 Banks(64Mb), 1 Bank(32Mb).

BA1=0 BA0=0	BA1=0 BA0=1
BA1=1 BA0=0	BA1=1 BA0=1

- 4 Banks

BA1=0 BA0=0	BA1=0 BA0=1
BA1=1 BA0=0	BA1=1 BA0=1

- 2 Banks

BA1=0 BA0=0	BA1=0 BA0=1
BA1=1 BA0=0	BA1=1 BA0=1

- 1 Bank



Partial Self Refresh Area

Temperature Compensated Self Refresh

1. In order to save power consumption, Mobile SDRAM has includes the Internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range : Max 40°C and Max 85°C(for Extended), Max 70°C(for Commercial).
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (Icc 6)			Unit
	- G/F			
	4 Banks	2 Banks	1 Bank	
Max 85/70 °C	800	650	550	uA
Max 40 °C	500	460	440	

B. Power Up Sequence

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
 - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue an extended mode register set command to define PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and EMRS command needs to be issued only when PASR is used.

The default state without EMRS command issued is all 4banks refreshed.

The device is now ready for the operation selected by EMRS.

For operating with PASR, set PASR mode in EMRS setting stage.

In order to adjust another mode in the state of PASR mode, additional EMRS set is required but power up sequence is not needed again at this time, In that case, all banks have to be in idle state prior to adjusting EMRS set.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A ₁	A ₀								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0