

IM[S/H]H1GP03A1F1C
IM[S/H]H2GP[13/02]A1F1C
IM[S/H]H4GP[23/12]A1F1C

*240-Pin DDR3 Registered Modules with Parity bit
1-GByte, 2-GByte and 4-GByte
EU RoHS Compliant*

Advance
Internet Data Sheet

Rev. 0.63



IM[S/H]H1GP03A1F1C, IM[S/H]H2GP[13/02]A1F1C, IM[S/H]H4GP[23/12]A1F1C	
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All	Updated package outline, SPD codes, and editorial changes.
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All	Added Product Types and related information for modules with Heat Spreader.
Previous Revision: 2007-12, Rev. 0.5	
All	Data sheet for 1GB, 2GB and 4GB Registered Memory Modules with Parity bit Product Family.

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1 Overview

This chapter gives an overview of the 240-pin Registered DDR3 Dual-In-Line Memory Modules product family with parity bit for address and control bus and describes its main characteristics.

1.1 Features

- 240-pin 8-Byte DDR3 SDRAM Registered Dual-In-Line Memory Modules with parity bit for address and control bus.
- Module organization: One rank – 128M × 72, 256M × 72, two rank – 256M × 72, 512M × 72, four rank – 512M × 72
Chip organization: 128M × 8, 256M × 4
- PC3-10600 and PC3-8500 module speed grades.
- 4-GB, 2-GB, 1-GB modules built with 1-Gbit DDR3 SDRAMs in packages PG-TFBGA-78
- DDR3 SDRAMs with a single 1.5 V (± 0.075 V) power supply.
- Asynchronous Reset.
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
- Serial Presence Detect with EEPROM.
- On-DIMM Thermal Sensor.
- RDIMM dimensions: 133.35 mm x 30 mm.
- Based on standard reference raw cards: 'A', 'B', 'C', 'E' and 'H'
- RoHS compliant products¹⁾.

TABLE 1

Performance Table for DDR3-1600 and DDR3-1333

Qimonda Speed Code		-13G	-13H	Unit	Note ²⁾
Module Speed Bin	PC3	-10600G	-10600H		
Device Speed Bin	DDR3	-1333G	-1333H		
CL- <i>n</i> _{RCD} - <i>n</i> _{RP}		8-8-8	9-9-9		
CL and CWL settings for maximum clock frequency		CL = 8 CWL = 7	CL = 9 CWL = 7	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		667 1333	667 1333	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		533 1066	533 1066	MHz Mb/s	



TABLE 2

Performance Table for DDR3–1066 and DDR3–800

Qimonda Speed Code		-10F	-10G	Unit	Note ²⁾
Module Speed Bin	PC3	-8500F	-8500G		
Device Speed Bin	DDR3	-1066F	-1066G		
CL- <i>n</i> _{RCD} - <i>n</i> _{RP}		7-7-7	8-8-8		
CL and CWL settings for maximum clock frequency		CL = 7 CWL = 6	CL = 8 CWL = 6	MHz	
Maximum Clock Frequency and Data Rate with above CL and CWL settings		533 1066	533 1066	MHz Mb/s	
Minimum Clock Frequency and Data Rate with above CL and CWL settings		400 800	400 800	MHz Mb/s	

- 1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit www.qimonda.com/green_products.
- 2) The available CL and CWL settings depend on the SDRAM device speed bin. The CL setting and CWL setting result in maximum but also minimum clock frequency requirements. When making a selection of operating clock frequency, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting. For details, refer to **Chapter 4.1** Speed Bins.



1.2 Description

The Qimonda IM[S/H]H[1G/2G/4G]PxxA1F1C are Registered DIMM (PDIMM) family with parity bit for address and control bus and 30 mm height based on DDR3 SDRAM technology. DIMMs are available in 128M × 72 (1-GB), 256M × 72 (2-GB), 512M × 72 (4-GB) organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 1-Gbit Double-Data-Rate-Three (DDR3) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and

a PLL for the clock distribution. De-coupling capacitors, stub resistors, calibration resistors and termination resistors are mounted on the PCB. The DIMMs feature serial presence detect based on a 256 byte serial EEPROM device using the 2-pin I2C protocol. The first 176 bytes are programmed with module specific SPD data.



TABLE 3
Product Information for Modules without Heat Spreader

Qimonda Product Type	Compliance Code	Description
1-GByte Registered DIMM IMSH1GP03A1F1C		
IMSH1GP03A1F1C-10F	1GB 1R×8 PC3-8500P-7-10-A0	240-pin 1-GByte DDR3 registered DIMM with one rank and on-DIMM thermal sensor. The memory rank consists of nine DDR3 components in x8 organization. Standard reference card A is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH1GP03A1F1C-10G	1GB 1R×8 PC3-8500P-8-10-A0	
IMSH1GP03A1F1C-13G	1GB 1R×8 PC3-10600P-8-10-A0	
IMSH1GP03A1F1C-13H	1GB 1R×8 PC3-10600P-9-10-A0	
2-GByte Registered DIMM IMSH2GP13A1F1C		
IMSH2GP13A1F1C-10F	2GB 2R×8 PC3-8500P-7-10-B0	240-pin 2-GByte DDR3 registered DIMM with two ranks and on-DIMM thermal sensor. Each memory rank consists of nine DDR3 components in x8 organization. Standard reference card B is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH2GP13A1F1C-10G	2GB 2R×8 PC3-8500P-8-10-B0	
IMSH2GP13A1F1C-13G	2GB 2R×8 PC3-10600P-8-10-B0	
IMSH2GP13A1F1C-13H	2GB 2R×8 PC3-10600P-9-10-B0	
2-GByte Registered DIMM IMSH2GP02A1F1C		
IMSH2GP02A1F1C-10F	2GB 1R×4 PC3-8500P-7-10-C0	240-pin 2-GByte DDR3 registered DIMM with one rank and on-DIMM thermal sensor. The memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card C is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-02A1F1C Density: 1-Gbit Organization: 256Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMSH2GP02A1F1C-10G	2GB 1R×4 PC3-8500P-8-10-C0	
IMSH2GP02A1F1C-13G	2GB 1R×4 PC3-10600P-8-10-C0	
IMSH2GP02A1F1C-13H	2GB 1R×4 PC3-10600P-9-10-C0	



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Qimonda Product Type	Compliance Code	Description
4-GByte Registered DIMM IMSH4GP23A1F1C		
IMSH4GP23A1F1C-10F	4GB 4Rx8 PC3-8500P-7-10-H0	240-pin 4-GByte DDR3 registered DIMM with four ranks and on-DIMM thermal sensor. Each memory rank consists of nine DDR3 components in x4 organization. Standard reference card H is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128-Mbit x 8 Address Bits (Row/Column/Bank): 14/10/3
IMSH4GP23A1F1C-10G	4GB 4Rx8 PC3-8500P-8-10-H0	
IMSH4GP23A1F1C-13G	4GB 4Rx8 PC3-10600P-8-10-H0	
IMSH4GP23A1F1C-13H	4GB 4Rx8 PC3-10600P-9-10-H0	
4-GByte Registered DIMM IMSH4GP12A1F1C		
IMSH4GP12A1F1C-10F	4GB 2Rx4 PC3-8500P-7-10-E0	240-pin 4-GByte DDR3 registered DIMM with two ranks and on-DIMM thermal sensor. Each memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card E is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-02A1F1C Density: 1-Gbit Organization: 256-Mbit x 4 Address Bits (Row/Column/Bank): 14/11/3
IMSH4GP12A1F1C-10G	4GB 2Rx4 PC3-8500P-8-10-E0	
IMSH4GP12A1F1C-13G	4GB 2Rx4 PC3-10600P-8-10-E0	
IMSH4GP12A1F1C-13H	4GB 2Rx4 PC3-10600P-9-10-E0	

TABLE 4
Product Information for Modules with Heat Spreader

Qimonda Product Type	Compliance Code	Description
1-GByte Registered DIMM IMHH1GP03A1F1C		
IMHH1GP03A1F1C-10F	1GB 1Rx8 PC3-8500P-7-10-A0	240-pin 1-GByte DDR3 registered DIMM with one rank and on-DIMM thermal sensor. The memory rank consists of nine DDR3 components in x8 organization. Standard reference card A is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128-Mbit x 8 Address Bits (Row/Column/Bank): 14/10/3
IMHH1GP03A1F1C-10G	1GB 1Rx8 PC3-8500P-8-10-A0	
IMHH1GP03A1F1C-13G	1GB 1Rx8 PC3-10600P-8-10-A0	
IMHH1GP03A1F1C-13H	1GB 1Rx8 PC3-10600P-9-10-A0	
2-GByte Registered DIMM IMHH2GP13A1F1C		
IMHH2GP13A1F1C-10F	2GB 2Rx8 PC3-8500P-7-10-B0	240-pin 2-GByte DDR3 registered DIMM with two ranks and on-DIMM thermal sensor. Each memory rank consists of nine DDR3 components in x8 organization. Standard reference card B is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128-Mbit x 8 Address Bits (Row/Column/Bank): 14/10/3
IMHH2GP13A1F1C-10G	2GB 2Rx8 PC3-8500P-8-10-B0	
IMHH2GP13A1F1C-13G	2GB 2Rx8 PC3-10600P-8-10-B0	
IMHH2GP13A1F1C-13H	2GB 2Rx8 PC3-10600P-9-10-B0	



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Qimonda Product Type	Compliance Code	Description
2-GByte Registered DIMM IMHH2GP02A1F1C		
IMHH2GP02A1F1C-10F	2GB 1R×4 PC3-8500P-7-10-C0	240-pin 2-GByte DDR3 registered DIMM with one rank and on-DIMM thermal sensor. The memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card C is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-02A1F1C Density: 1-Gbit Organization: 256-Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMHH2GP02A1F1C-10G	2GB 1R×4 PC3-8500P-8-10-C0	
IMHH2GP02A1F1C-13G	2GB 1R×4 PC3-10600P-8-10-C0	
IMHH2GP02A1F1C-13H	2GB 1R×4 PC3-10600P-9-10-C0	
4-GByte Registered DIMM IMHH4GP23A1F1C		
IMHH4GP23A1F1C-10F	4GB 4R×8 PC3-8500P-7-10-H0	240-pin 4-GByte DDR3 registered DIMM with four ranks and on-DIMM thermal sensor. Each memory rank consists of nine DDR3 components in x4 organization. Standard reference card H is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-03A1F1C Density: 1-Gbit Organization: 128-Mbit × 8 Address Bits (Row/Column/Bank): 14/10/3
IMHH4GP23A1F1C-10G	4GB 4R×8 PC3-8500P-8-10-H0	
IMHH4GP23A1F1C-13G	4GB 4R×8 PC3-10600P-8-10-H0	
IMHH4GP23A1F1C-13H	4GB 4R×8 PC3-10600P-9-10-H0	
4-GByte Registered DIMM IMHH4GP12A1F1C		
IMHH4GP12A1F1C-10F	4GB 2R×4 PC3-8500P-7-10-E0	240-pin 4-GByte DDR3 registered DIMM with two ranks and on-DIMM thermal sensor. Each memory rank consists of eighteen DDR3 components in x4 organization. Standard reference card E is used on this assembly Used DDR3 SDRAM Component Product Type: IDSH1G-02A1F1C Density: 1-Gbit Organization: 256-Mbit × 4 Address Bits (Row/Column/Bank): 14/11/3
IMHH4GP12A1F1C-10G	4GB 2R×4 PC3-8500P-8-10-E0	
IMHH4GP12A1F1C-13G	4GB 2R×4 PC3-10600P-8-10-E0	
IMHH4GP12A1F1C-13H	4GB 2R×4 PC3-10600P-9-10-E0	



2 Configuration

2.1 Pin Configuration

TABLE 5

Pin Configuration of DDR3 RDIMM - 240 Pins

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
Clock Signals					
CK0	ck0_t	184	I	SSTL	Differential Clock Inputs [1:0]
$\overline{\text{CK0}}$	ck0_c	185	I	SSTL	
CK1	ck1_t	63	I	SSTL	
$\overline{\text{CK1}}$	ck1_c	64	I	SSTL	
Control Signals					
CKE0	cke0	50	I	SSTL	Clock Enable [1:0]
CKE1	cke1	169	I	SSTL	
ODT0	odt0	195	I	SSTL	On-Die Termination [1:0]
ODT1	odt1	77	I	SSTL	
$\overline{\text{S0}}$	s0_n	193	I	SSTL	Chip Select [3:0]
$\overline{\text{S1}}$	s1_n	76	I	SSTL	
$\overline{\text{S2}}$	s2_n	79	I	SSTL	
$\overline{\text{S3}}$	s3_n	198	I	SSTL	
Command Signals					
$\overline{\text{RAS}}$	ras_n	192	I	SSTL	Row Address Strobe
$\overline{\text{CAS}}$	cas_n	74	I	SSTL	Column Address Strobe
$\overline{\text{WE}}$	we_n	73	I	SSTL	Write Enable
Bank Address Signals					
BA0	ba0	71	I	SSTL	Bank Address Bus[2:0]
BA1	ba1	190	I	SSTL	
BA2	ba2	52	I	SSTL	
Address Signals					
A0	a0	188	I	SSTL	Address Bus [15:0]
A1	a1	181	I	SSTL	
A2	a2	61	I	SSTL	
A3	a3	180	I	SSTL	
A4	a4	59	I	SSTL	



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function	
A5	a5	58	I	SSTL	Address Bus [15:0]	
A6	a6	178	I	SSTL		
A7	a7	56	I	SSTL		
A8	a8	177	I	SSTL		
A9	a9	175	I	SSTL		
A10/AP	a10	70	I	SSTL		
A11	a11	55	I	SSTL		
A12/BC	a12	174	I	SSTL		
A13	a13	196	I	SSTL		
A14	a14	172	I	SSTL		
A15	a15	171	I	SSTL		
Data Signals						
DQ0	dq0	3	I/O	SSTL		Data Bus [63:0]
DQ1	dq1	4	I/O	SSTL		
DQ2	dq2	9	I/O	SSTL		
DQ3	dq3	10	I/O	SSTL		
DQ4	dq4	122	I/O	SSTL		
DQ5	dq5	123	I/O	SSTL		
DQ6	dq6	128	I/O	SSTL		
DQ7	dq7	129	I/O	SSTL		
DQ8	dq8	12	I/O	SSTL		
DQ9	dq9	13	I/O	SSTL		
DQ10	dq10	18	I/O	SSTL		
DQ11	dq11	19	I/O	SSTL		
DQ12	dq12	131	I/O	SSTL		
DQ13	dq13	132	I/O	SSTL		
DQ14	dq14	137	I/O	SSTL		
DQ15	dq15	138	I/O	SSTL		
DQ16	dq16	21	I/O	SSTL		
DQ17	dq17	22	I/O	SSTL		
DQ18	dq18	27	I/O	SSTL		
DQ19	dq19	28	I/O	SSTL		
DQ20	dq20	140	I/O	SSTL		
DQ21	dq21	141	I/O	SSTL		
DQ22	dq22	146	I/O	SSTL		
DQ23	dq23	147	I/O	SSTL		
DQ24	dq24	30	I/O	SSTL		
DQ25	dq25	31	I/O	SSTL		
DQ26	dq26	36	I/O	SSTL		
DQ27	dq27	37	I/O	SSTL		



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
DQ28	dq28	149	I/O	SSTL	Data Bus [63:0]
DQ29	dq29	150	I/O	SSTL	
DQ30	dq30	155	I/O	SSTL	
DQ31	dq31	156	I/O	SSTL	
DQ32	dq32	81	I/O	SSTL	
DQ33	dq33	82	I/O	SSTL	
DQ34	dq34	87	I/O	SSTL	
DQ35	dq35	88	I/O	SSTL	
DQ36	dq36	200	I/O	SSTL	
DQ37	dq37	201	I/O	SSTL	
DQ38	dq38	206	I/O	SSTL	
DQ39	dq39	207	I/O	SSTL	
DQ40	dq40	90	I/O	SSTL	
DQ41	dq41	91	I/O	SSTL	
DQ42	dq42	96	I/O	SSTL	
DQ43	dq43	97	I/O	SSTL	
DQ44	dq44	209	I/O	SSTL	
DQ45	dq45	210	I/O	SSTL	
DQ46	dq46	215	I/O	SSTL	
DQ47	dq47	216	I/O	SSTL	
DQ48	dq48	99	I/O	SSTL	
DQ49	dq49	100	I/O	SSTL	
DQ50	dq50	105	I/O	SSTL	
DQ51	dq51	106	I/O	SSTL	
DQ52	dq52	218	I/O	SSTL	
DQ53	dq53	219	I/O	SSTL	
DQ54	dq54	224	I/O	SSTL	
DQ55	dq55	225	I/O	SSTL	
DQ56	dq56	108	I/O	SSTL	
DQ57	dq57	109	I/O	SSTL	
DQ58	dq58	114	I/O	SSTL	
DQ59	dq59	115	I/O	SSTL	
DQ60	dq60	227	I/O	SSTL	
DQ61	dq61	228	I/O	SSTL	
DQ62	dq62	233	I/O	SSTL	
DQ63	dq63	234	I/O	SSTL	
CB0	cb0	39	I/O	SSTL	Check Bit [7:0]
CB1	cb1	40	I/O	SSTL	
CB2	cb2	45	I/O	SSTL	
CB3	cb3	46	I/O	SSTL	



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
CB4	cb4	158	I/O	SSTL	Check Bit [7:0]
CB5	cb5	159	I/O	SSTL	
CB6	cb6	164	I/O	SSTL	
CB7	cb7	165	I/O	SSTL	
DQS0	dqs0_t	7	I/O	SSTL	Data Strobe Signals [17:0] and Complementary Data Strobe Signals [17:0]
$\overline{\text{DQS0}}$	dqs0_c	6	I/O	SSTL	
DQS1	dqs1_t	16	I/O	SSTL	
$\overline{\text{DQS1}}$	dqs1_c	15	I/O	SSTL	
DQS2	dqs2_t	25	I/O	SSTL	
$\overline{\text{DQS2}}$	dqs2_c	24	I/O	SSTL	
DQS3	dqs3_t	34	I/O	SSTL	
$\overline{\text{DQS3}}$	dqs3_c	33	I/O	SSTL	
DQS4	dqs4_t	85	I/O	SSTL	
$\overline{\text{DQS4}}$	dqs4_c	84	I/O	SSTL	
DQS5	dqs5_t	94	I/O	SSTL	
$\overline{\text{DQS5}}$	dqs5_c	93	I/O	SSTL	
DQS6	dqs6_t	103	I/O	SSTL	
$\overline{\text{DQS6}}$	dqs6_c	102	I/O	SSTL	
DQS7	dqs7_t	112	I/O	SSTL	
$\overline{\text{DQS7}}$	dqs7_c	111	I/O	SSTL	
DQS8	dqs8_t	43	I/O	SSTL	
$\overline{\text{DQS8}}$	dqs8_c	42	I/O	SSTL	
(T)DQS9	dqs9_t	125	I/O	SSTL	
$\overline{\text{(T)DQS9}}$	dqs9_c	126	I/O	SSTL	
(T)DQS10	dqs10_t	134	I/O	SSTL	
$\overline{\text{(T)DQS10}}$	dqs10_c	135	I/O	SSTL	
(T)DQS11	dqs11_t	143	I/O	SSTL	
$\overline{\text{(T)DQS11}}$	dqs11_c	144	I/O	SSTL	
(T)DQS12	dqs12_t	152	I/O	SSTL	
$\overline{\text{(T)DQS12}}$	dqs12_c	153	I/O	SSTL	
(T)DQS13	dqs13_t	203	I/O	SSTL	
$\overline{\text{(T)DQS13}}$	dqs13_c	204	I/O	SSTL	
(T)DQS14	dqs14_t	212	I/O	SSTL	
$\overline{\text{(T)DQS14}}$	dqs14_c	213	I/O	SSTL	
(T)DQS15	dqs15_t	221	I/O	SSTL	
$\overline{\text{(T)DQS15}}$	dqs15_c	222	I/O	SSTL	
(T)DQS16	dqs16_t	230	I/O	SSTL	
$\overline{\text{(T)DQS16}}$	dqs16_c	231	I/O	SSTL	
(T)DQS17	dqs17_t	161	I/O	SSTL	
$\overline{\text{(T)DQS17}}$	dqs17_c	162	I/O	SSTL	



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
EEPROM and Thermal Sensor					
SCL	scl	118	I	CMOS	Serial Bus Clock
SDA	sda	238	I/O	OD	Serial Data Bus
SA0	sa0	117	I	CMOS	Serial Address Select Bus [2:0]
SA1	sa1	237	I	CMOS	
SA2	sa2	119	I	CMOS	
Power Supply					
V _{DD}	vdd	51, 54, 57, 60, 62, 65, 66, 69, 72, 75, 78, 170, 173, 176, 179, 182, 183, 186, 189, 191, 194, 197	PWR	-	Power Supply
V _{SS}	vss	2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 80, 83, 86, 89,92,95, 98, 101, 104, 107, 110, 113, 116, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 199, 202, 205, 208, 211, 214, 217, 220, 223, 226, 229, 232, 235, 239	GND	-	Ground
V _{REF,DQ}	vrefdq	1	AI	-	Reference Voltage



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Pin Name	EDA Signal Name ¹⁾	Pin No.	Pin Type	Buffer Type	Function
V _{REF.CA}	vrefca	67	AI	-	Reference Voltage
V _{TT}	vtt	48, 49, 120, 240	PWR	-	Termination Voltage
V _{DDSPD}	vddspd	236		-	EEPROM and Thermal Sensor Power Supply
Other Pins					
<u>RESET</u>	reset_n	168	I		Asynchronous Reset
<u>Err_Out</u>	err_out_n	53	O	OD	Err_Out
<u>Par_In</u>	par_in	68	I		Par_In
<u>EVENT</u>	event_n	187	O	OD	EVENT
NC	nc	79, 126, 135, 144, 153, 162, 167, 198, 204, 213, 222, 231,	-	-	Not Connected

1) The EDA (Electronic Design Automation) Signal Name is used in Qimonda Simulation Models such as EBD (Electronic Board Description).

TABLE 6
Abbreviations for Pin Type

Abbreviation	Description
I	Standard Input pin only. Digital levels.
O	Standard Output pin only - Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input - Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

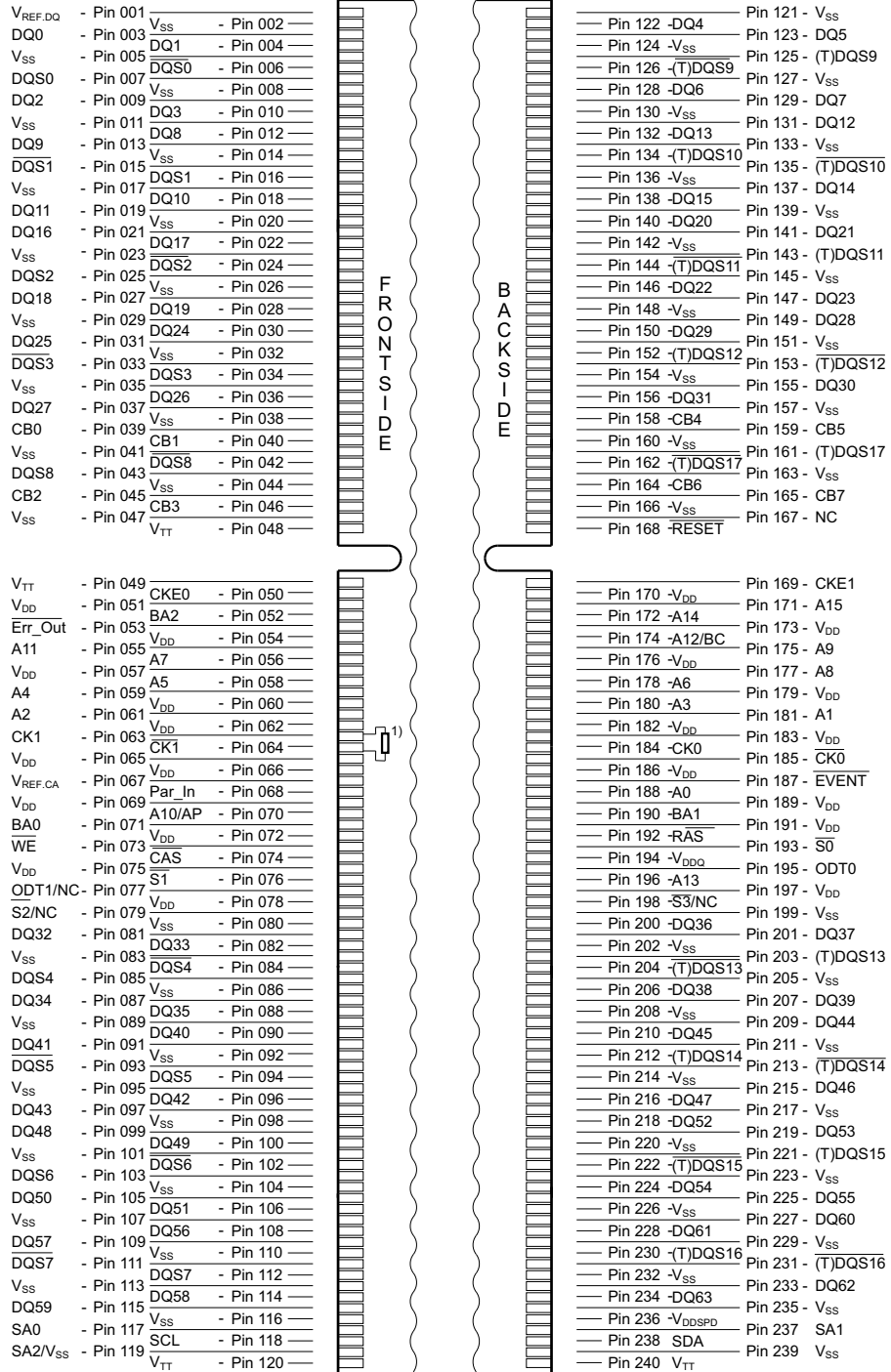
TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

FIGURE 1
Pin Configuration RDIMM - 240 Pin



1) Pin 63 and Pin 64 terminated with 120 Ω

(T) : For x8 DRAM only



3 Operating Conditions

3.1 Absolute Maximum Ratings

TABLE 8
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4	+1.975	V	1)
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4	+1.975	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	+1.975	V	

1) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REFDQ} and V_{REFCA} must not be greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REFDQ} and V_{REFCA} may be equal or less than 300 mV.

TABLE 9
Environmental Parameters

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Operating Temperature	T_{OPR}	-	-	°C	1)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Temperature	T_{STG}	-50	+100	°C	2)
Storage Humidity (without condensation)	H_{STG}	5	95	%	
Barometric Pressure (Operating and Storage)	P_{Bar}	69	105	KPascal	3)

1) Device designer must meet the case temperature specification for individual module components.

2) Storage Temperature is the case surface temperature on the center/top side of the SDRAM mentioned in Qimonda component datasheet.

3) Up to 9850 ft.

Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



TABLE 10

DRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Normal Operating Temperature Range	T_{OPER}	0	85	°C	1)2)
Extended Temperature Range		85	95	°C	1)3)

- 1) Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM mentioned..
- 2) The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.
- 3) Some application require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C operating temperature. For more details please refer to Qimonda Component datasheet.

3.2 Recommended DC Operating Conditions

TABLE 11

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1)2)
Supply Voltage for EEPROM and Thermal Sensor	$V_{DD.SPD}$	3.0	3.3	3.6	V	1)2)
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
Terminal Voltage	V_{TT}	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	
External Calibration Resistor connected from ZQ pin to ground	R_{ZQ}	237.6	240.0	242.4	Ω	5)

- 1) V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together
- 2) Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- 3) The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than $\pm 1\% V_{DD}$ (for reference: approx. ± 15 mV).
- 4) For reference: approx. $V_{DD}/2 \pm 15$ mV.
- 5) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.



4 Speed Bins and Timing Parameters

AC timings are provided with $\overline{CK}/\overline{CK}$ and $\overline{DQS}/\overline{DQS}$ differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength. The $\overline{CK}/\overline{CK}$ input reference level (for timing referenced to $\overline{CK}/\overline{CK}$) is the point at which \overline{CK} and \overline{CK} cross. The $\overline{DQS}/\overline{DQS}$ reference level (for timing referenced to $\overline{DQS}/\overline{DQS}$) is the point at which \overline{DQS} and \overline{DQS}

cross. Inputs are not recognized as valid until V_{REF} stabilizes. During the period before $V_{REF,CA}$ and $V_{REF,DQ}$ stabilizes, $\overline{CKE} = 0.2 \times V_{DDQ}$ is recognized as low. The output timing reference voltage level is V_{TT} . For details of all relevant AC timing parameters see the QIMONDA DDR3 component datasheet.

4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK,AVG,MIN}$ and $t_{CK,AVG,MAX}$ requirements. When making a selection of $t_{CK,AVG}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting
- $t_{CK,AVG,MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be provided. An application should use the next smaller standard $t_{CK,AVG}$ value (2.5, 1.875, 1.5, 1.25, 1.07, or 0.935 ns) when calculating $CL [nCK] = t_{AA} [ns] / t_{CK,AVG} [ns]$, rounding up to the next 'Supported CL'
- $t_{CK,AVG,MAX}$ limits: Calculate $t_{CK,AVG} = t_{AA,MAX} / CL_{SELECTED}$ and round the resulting $t_{CK,AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.935 ns). This result is $t_{CK,AVG,MAX}$ corresponding to CLSELECTED
- 'Reserved' settings are not allowed. User must program a different value
- Downbinning support for DDR3-1333H and DDR3-1600K parts: The minimum tAA / tRCD / tRP supported by DDR3-1333H and DDR3-1600K devices is 13.125ns. Therefore,

The absolute specification for all speed bins is T_{OPER} and $V_{DD} = V_{DDQ} = 1.5 \text{ V} \pm 0.075 \text{ V}$. In addition the following general notes apply.

- in module application, tAA / tRCD / tRP should be programmed with minimum supported values. For example, DDR3-1333H supporting down-shift to DDR3-1066F should program SPD as 13.125ns for tAA.MIN (Byte16)/tRCD.MIN (Byte18) / tRP (Byte20). DDR3-1600K supporting down-shift to DDR3-1333H and to DDR3-1066F should program SPD as 13.125ns for tAA.MIN (Byte16)/tRCD.MIN (Byte18) / tRP (Byte20)
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization



TABLE 12

DDR3-1333 Speed Bins and Operating Conditions

Speed Bin		DDR3-1333G		DDR3-1333H		Unit	Note
CL-nRCD-nRP		8-8-8		9-9-9			
QAG Product Type Extension		-13G		-13H			
Parameter	Symbol	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	12.0	20.0	13.125	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.0	—	13.125	—	ns	1)
PRE command period	t_{RP}	12.0	—	13.125	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.0	—	49.125	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10		6,7,8, 9, 10		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7		5, 6, 7		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	ns	1)2)

- 1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
- 2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.



TABLE 13

DDR3-1066 Speed Bins and Operating Conditions

Speed Bin		DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL-nRCD-nRP		6-6-6		7-7-7		8-8-8			
QAG Product Type Extension		-10E		-10F		-10G			
Parameter	Symbol	Min.	Max.	Min.	Max.	Min.	Max.		
Internal read command to first data	t_{AA}	11.25	20.0	13.125	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	11.25	—	13.125	—	15.0	—	ns	1)
PRE command period	t_{RP}	11.25	—	13.125	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.75	—	50.625	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6		5, 6		5, 6		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.

2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.



5 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 14 “IMSH1GP03A1F1C” on Page 20
- Table 15 “IMSH2GP02A1F1C” on Page 24
- Table 16 “IMSH2GP13A1F1C” on Page 28
- Table 17 “IMSH4GP12A1F1C” on Page 32
- Table 18 “IMSH4GP23A1F1C” on Page 36
- Table 19 “IMHH1GP03A1F1C” on Page 40
- Table 20 “IMHH2GP02A1F1C” on Page 44
- Table 21 “IMHH2GP13A1F1C” on Page 48
- Table 22 “IMHH4GP12A1F1C” on Page 52
- Table 23 “IMHH4GP23A1F1C” on Page 56

TABLE 14
IMSH1GP03A1F1C

Product Type		IMSH1GP03A1F1C-10F	IMSH1GP03A1F1C-10G	IMSH1GP03A1F1C-13G	IMSH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		x72	x72	x72	x72
		1 Rank (x8)	1 Rank (x8)	1 Rank (x8)	1 Rank (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	01	01	01	01



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH1GP03A1F1C-10F	IMSH1GP03A1F1C-10G	IMSH1GP03A1F1C-13G	IMSH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH1GP03A1F1C-10F	IMSH1GP03A1F1C-10G	IMSH1GP03A1F1C-13G	IMSH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	00	00	00	00
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	00	00	00	00
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength,Command/Address	00	00	00	00
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength,Control and Clock	00	00	00	00
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	64	07	A0	B0
127	Cyclical Redundancy Code MSB	58	AD	D7	48
128	Product Type, Char 1	49	49	49	49



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH1GP03A1F1C-10F	IMSH1GP03A1F1C-10G	IMSH1GP03A1F1C-13G	IMSH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		x72	x72	x72	x72
		1 Rank (x8)	1 Rank (x8)	1 Rank (x8)	1 Rank (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	31	31	31	31
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	30	30	30	30
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	5x	4x	5x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 15
IMSH2GP02A1F1C

Product Type		IMSH2GP02A1F1C-10F	IMSH2GP02A1F1C-10G	IMSH2GP02A1F1C-13G	IMSH2GP02A1F1C-13H
Organization		2 GByte ×72 1 Rank (×4)	2 GByte ×72 1 Rank (×4)	2 GByte ×72 1 Rank (×4)	2 GByte ×72 1 Rank (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	12	12	12	12
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	00	00	00	00
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP02A1F1C-10F	IMSH2GP02A1F1C-10G	IMSH2GP02A1F1C-13G	IMSH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		1 Rank (x4)	1 Rank (x4)	1 Rank (x4)	1 Rank (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	02	02	02	02
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	00	00	00	00
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP02A1F1C-10F	IMSH2GP02A1F1C-10G	IMSH2GP02A1F1C-13G	IMSH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		1 Rank (x4)	1 Rank (x4)	1 Rank (x4)	1 Rank (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	20	43	E4	F4
127	Cyclical Redundancy Code MSB	49	BC	C6	59
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	32	32	32	32
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	30	30	30	30
136	Product Type, Char 9	32	32	32	32
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP02A1F1C-10F	IMSH2GP02A1F1C-10G	IMSH2GP02A1F1C-13G	IMSH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×4)	1 Rank (×4)	1 Rank (×4)	1 Rank (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	4x	4x	5x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 16
IMSH2GP13A1F1C

Product Type		IMSH2GP13A1F1C-10F	IMSH2GP13A1F1C-10G	IMSH2GP13A1F1C-13G	IMSH2GP13A1F1C-13H
Organization		2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	09	09	09	09
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP13A1F1C-10F	IMSH2GP13A1F1C-10G	IMSH2GP13A1F1C-13G	IMSH2GP13A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	01	01	01	01
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	00	00	00	00
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP13A1F1C-10F	IMSH2GP13A1F1C-10G	IMSH2GP13A1F1C-13G	IMSH2GP13A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	00	00	00	00
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	96	F5	52	42
127	Cyclical Redundancy Code MSB	30	C5	BF	20
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	32	32	32	32
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	31	31	31	31
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH2GP13A1F1C-10F	IMSH2GP13A1F1C-10G	IMSH2GP13A1F1C-13G	IMSH2GP13A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	4x	4x	5x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 17
IMSH4GP12A1F1C

Product Type		IMSH4GP12A1F1C-10F	IMSH4GP12A1F1C-10G	IMSH4GP12A1F1C-13G	IMSH4GP12A1F1C-13H
Organization		4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	12	12	12	12
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	08	08	08	08
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP12A1F1C-10F	IMSH4GP12A1F1C-10G	IMSH4GP12A1F1C-13G	IMSH4GP12A1F1C-13H
Organization		4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	04	04	04	04
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	09	09	09	09
64	Reserved Thermal Heat Spreader Solution	00	00	00	00
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP12A1F1C-10F	IMSH4GP12A1F1C-10G	IMSH4GP12A1F1C-13G	IMSH4GP12A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	27	44	E3	F3
127	Cyclical Redundancy Code MSB	49	BC	C6	59
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	34	34	34	34
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	31	31	31	31
136	Product Type, Char 9	32	32	32	32
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP12A1F1C-10F	IMSH4GP12A1F1C-10G	IMSH4GP12A1F1C-13G	IMSH4GP12A1F1C-13H
Organization		4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	4x	4x	5x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 18
IMSH4GP23A1F1C

Product Type		IMSH4GP23A1F1C-10F	IMSH4GP23A1F1C-10G	IMSH4GP23A1F1C-13G	IMSH4GP23A1F1C-13H
Organization		4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	19	19	19	19
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP23A1F1C-10F	IMSH4GP23A1F1C-10G	IMSH4GP23A1F1C-13G	IMSH4GP23A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	11	11	11	11
62	Raw Card used	07	07	07	07
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	09	09	09	09
64	Reserved Thermal Heat Spreader Solution	00	00	00	00
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP23A1F1C-10F	IMSH4GP23A1F1C-10G	IMSH4GP23A1F1C-13G	IMSH4GP23A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	11	72	D5	C5
127	Cyclical Redundancy Code MSB	FB	0E	74	EB
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	53	53	53	53
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	34	34	34	34
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	32	32	32	32
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMSH4GP23A1F1C-10F	IMSH4GP23A1F1C-10G	IMSH4GP23A1F1C-13G	IMSH4GP23A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 19
IMHH1GP03A1F1C

Product Type		IMHH1GP03A1F1C-10F	IMHH1GP03A1F1C-10G	IMHH1GP03A1F1C-13G	IMHH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	01	01	01	01
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH1GP03A1F1C-10F	IMHH1GP03A1F1C-10G	IMHH1GP03A1F1C-13G	IMHH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	33	33	33	33
62	Raw Card used	00	00	00	00
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	80	80	80	80
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	00	00	00	00



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH1GP03A1F1C-10F	IMHH1GP03A1F1C-10G	IMHH1GP03A1F1C-13G	IMHH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×8)	1 Rank (×8)	1 Rank (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	00	00	00	00
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	21	42	E5	F5
127	Cyclical Redundancy Code MSB	A4	51	2B	B4
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	48	48	48	48
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	31	31	31	31
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	30	30	30	30
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH1GP03A1F1C-10F	IMHH1GP03A1F1C-10G	IMHH1GP03A1F1C-13G	IMHH1GP03A1F1C-13H
Organization		1 GByte	1 GByte	1 GByte	1 GByte
		x72	x72	x72	x72
		1 Rank (x8)	1 Rank (x8)	1 Rank (x8)	1 Rank (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 20
IMHH2GP02A1F1C

Product Type		IMHH2GP02A1F1C-10F	IMHH2GP02A1F1C-10G	IMHH2GP02A1F1C-13G	IMHH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×4)	1 Rank (×4)	1 Rank (×4)	1 Rank (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	12	12	12	12
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	00	00	00	00
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP02A1F1C-10F	IMHH2GP02A1F1C-10G	IMHH2GP02A1F1C-13G	IMHH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		1 Rank (x4)	1 Rank (x4)	1 Rank (x4)	1 Rank (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	33	33	33	33
62	Raw Card used	02	02	02	02
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	80	80	80	80
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP02A1F1C-10F	IMHH2GP02A1F1C-10G	IMHH2GP02A1F1C-13G	IMHH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		1 Rank (x4)	1 Rank (x4)	1 Rank (x4)	1 Rank (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	65	06	A1	B1
127	Cyclical Redundancy Code MSB	B5	40	3A	A5
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	48	48	48	48
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	32	32	32	32
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	30	30	30	30
136	Product Type, Char 9	32	32	32	32
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP02A1F1C-10F	IMHH2GP02A1F1C-10G	IMHH2GP02A1F1C-13G	IMHH2GP02A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		1 Rank (x4)	1 Rank (x4)	1 Rank (x4)	1 Rank (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 21
IMHH2GP13A1F1C

Product Type		IMHH2GP13A1F1C-10F	IMHH2GP13A1F1C-10G	IMHH2GP13A1F1C-13G	IMHH2GP13A1F1C-13H
Organization		2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	09	09	09	09
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP13A1F1C-10F	IMHH2GP13A1F1C-10G	IMHH2GP13A1F1C-13G	IMHH2GP13A1F1C-13H
Organization		2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	33	33	33	33
62	Raw Card used	01	01	01	01
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	05	05	05	05
64	Reserved Thermal Heat Spreader Solution	80	80	80	80
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP13A1F1C-10F	IMHH2GP13A1F1C-10G	IMHH2GP13A1F1C-13G	IMHH2GP13A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		×72	×72	×72	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	00	00	00	00
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	D3	B0	17	07
127	Cyclical Redundancy Code MSB	CC	39	43	DC
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	48	48	48	48
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	32	32	32	32
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	31	31	31	31
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH2GP13A1F1C-10F	IMHH2GP13A1F1C-10G	IMHH2GP13A1F1C-13G	IMHH2GP13A1F1C-13H
Organization		2 GByte	2 GByte	2 GByte	2 GByte
		x72	x72	x72	x72
		2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)	2 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 22
IMHH4GP12A1F1C

Product Type		IMHH4GP12A1F1C-10F	IMHH4GP12A1F1C-10G	IMHH4GP12A1F1C-13G	IMHH4GP12A1F1C-13H
Organization		4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)	4 GByte ×72 2 Ranks (×4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	12	12	12	12
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	08	08	08	08
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP12A1F1C-10F	IMHH4GP12A1F1C-10G	IMHH4GP12A1F1C-13G	IMHH4GP12A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	33	33	33	33
62	Raw Card used	04	04	04	04
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	09	09	09	09
64	Reserved Thermal Heat Spreader Solution	80	80	80	80
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP12A1F1C-10F	IMHH4GP12A1F1C-10G	IMHH4GP12A1F1C-13G	IMHH4GP12A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	62	01	A6	B6
127	Cyclical Redundancy Code MSB	B5	40	3A	A5
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	48	48	48	48
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	34	34	34	34
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	31	31	31	31
136	Product Type, Char 9	32	32	32	32
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP12A1F1C-10F	IMHH4GP12A1F1C-10G	IMHH4GP12A1F1C-13G	IMHH4GP12A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)	2 Ranks (x4)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

TABLE 23
IMHH4GP23A1F1C

Product Type		IMHH4GP23A1F1C-10F	IMHH4GP23A1F1C-10G	IMHH4GP23A1F1C-13G	IMHH4GP23A1F1C-13H
Organization		4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
0	# of SPD bytes utilized / # of bytes in SPD / CRC	92	92	92	92
1	SPD Revision	10	10	10	10
2	SDRAM technology key byte	0B	0B	0B	0B
3	DIMM module type	01	01	01	01
4	SDRAM density and banks	02	02	02	02
5	SDRAM addressing	11	11	11	11
6	Module Nominal Voltage, VDD	00	00	00	00
7	Module organization	19	19	19	19
8	Module memory bus width	0B	0B	0B	0B
9	Fine time base (FTB) dividend and divisor	52	52	52	52
10	Medium time base (MTB) dividend	01	01	01	01
11	Medium time base (MTB) divisor	08	08	08	08
12	Minimum SDRAM cycle time ($t_{CK.MIN}$)	0F	0F	0C	0C
13	Reserved	00	00	00	00
14	CAS Latencies Supported - LSB	1C	14	7E	7C
15	CAS Latencies Supported - MSB	00	00	00	00
16	Minimum CAS Latency Time ($t_{CK.MIN}$)	69	78	60	69
17	Minimum Write Recovery Time ($t_{WR.MIN}$)	78	78	78	78
18	Minimum RAS# toCAS# Delay Time ($t_{RCD.MIN}$)	69	78	60	69
19	Minimum Row Active to Row Active Delay Time ($t_{RRD.MIN}$)	3C	3C	30	30
20	Minimum Row PrechargeTime ($t_{RP.MIN}$)	69	78	60	69
21	Upper Nibbles for t_{RAS} and t_{RC}	11	11	11	11



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP23A1F1C-10F	IMHH4GP23A1F1C-10G	IMHH4GP23A1F1C-13G	IMHH4GP23A1F1C-13H
Organization		4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)	4 GByte ×72 4 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
22	Minimum Active to Precharge Time ($t_{RAS.MIN}$), LSB	2C	2C	20	20
23	Minimum Active to Active/Refresh Time ($t_{RC.MIN}$), LSB	95	A4	80	8C
24	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), LSB	70	70	70	70
25	Minimum Refresh Recovery Time ($t_{RFC.MIN}$), MSB	03	03	03	03
26	Minimum Internal Write to Read Command Delay Time ($t_{WTR.MIN}$)	3C	3C	3C	3C
27	Minimum Internal Read to Precharge Command Delay Time ($t_{RTP.MIN}$), MSB	3C	3C	3C	3C
28	Upper Nibble for t_{FAW}	01	01	00	00
29	Minimum Four Activate Window Delay Time ($t_{FAW.MIN}$)	2C	2C	F0	F0
30	SDRAM Optional Features	02	02	02	02
31	SDRAM Thermal and Refresh Options	81	81	81	81
32	Module Thermal Sensor	80	80	80	80
33	SDRAM Device Type	00	00	00	00
34 - 59	Reserved	00	00	00	00
60	Module Nominal Height	10	10	10	10
61	Module Maximum Thickness	33	33	33	33
62	Raw Card used	07	07	07	07
63	Address Mapping from Edge Connector to DRAM DIMM Module Attributes	09	09	09	09
64	Reserved Thermal Heat Spreader Solution	80	80	80	80
65 - 69	Reserved	00	00	00	00
70	Reserved RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50	50	50	50



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP23A1F1C-10F	IMHH4GP23A1F1C-10G	IMHH4GP23A1F1C-13G	IMHH4GP23A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		×72	×72	×72	×72
		4 Ranks (×8)	4 Ranks (×8)	4 Ranks (×8)	4 Ranks (×8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
71	Reserved RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	55	55	55	55
72 - 116	Reserved	00	00	00	00
117	DIMM Manufacturer's ID Code LSB	85	85	85	85
118	DIMM Manufacturer's ID Code MSB	51	51	51	51
119	Module Manufacturing Location	xx	xx	xx	xx
120 - 121	Module Manufacturing Date	xx	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx	xx
126	Cyclical Redundancy Code LSB	54	37	90	80
127	Cyclical Redundancy Code MSB	07	F2	88	17
128	Product Type, Char 1	49	49	49	49
129	Product Type, Char 2	4D	4D	4D	4D
130	Product Type, Char 3	48	48	48	48
131	Product Type, Char 4	48	48	48	48
132	Product Type, Char 5	34	34	34	34
133	Product Type, Char 6	47	47	47	47
134	Product Type, Char 7	50	50	50	50
135	Product Type, Char 8	32	32	32	32
136	Product Type, Char 9	33	33	33	33
137	Product Type, Char 10	41	41	41	41
138	Product Type, Char 11	31	31	31	31
139	Product Type, Char 12	46	46	46	46
140	Product Type, Char 13	31	31	31	31
141	Product Type, Char 14	43	43	43	43



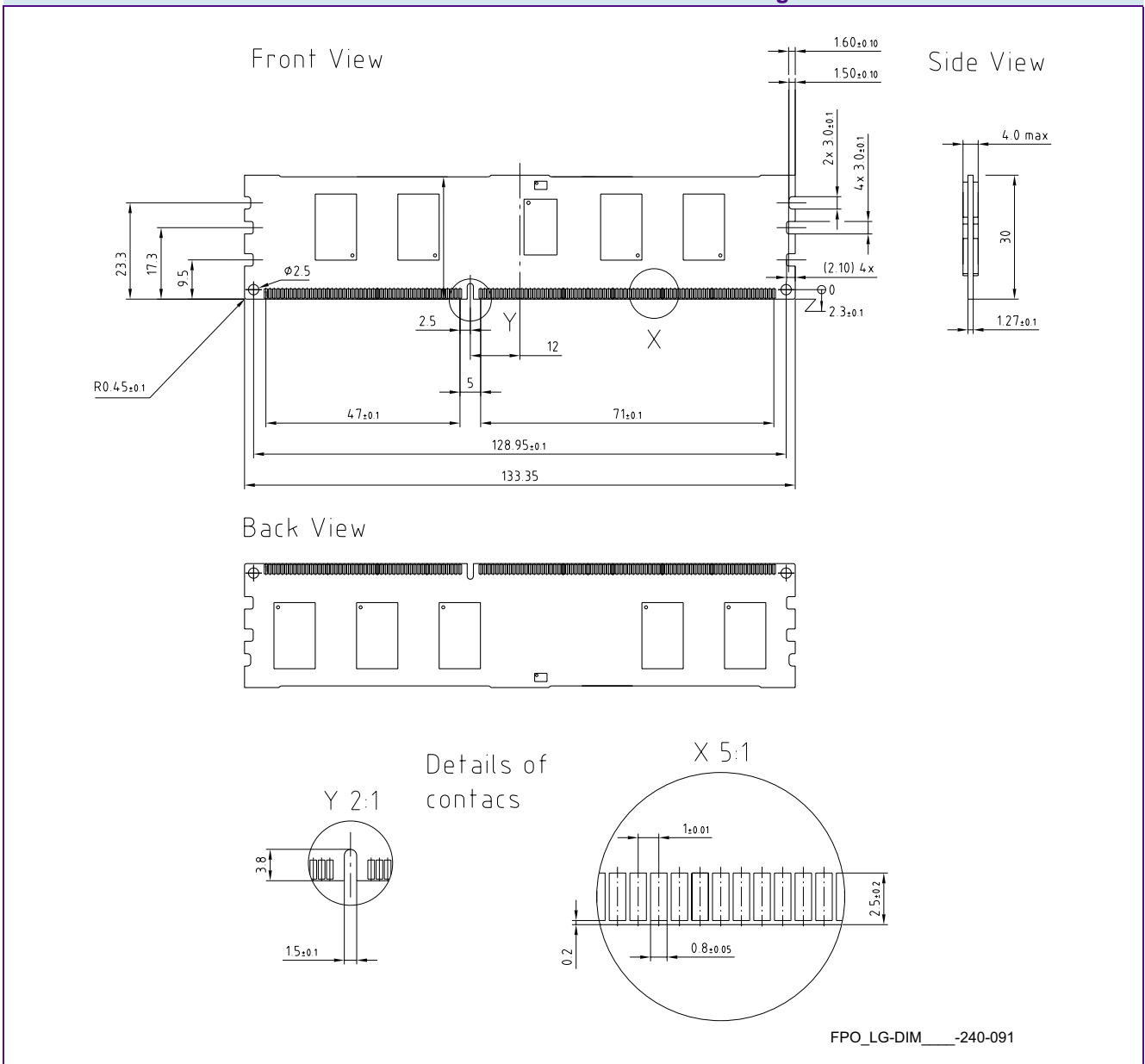
DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Product Type		IMHH4GP23A1F1C-10F	IMHH4GP23A1F1C-10G	IMHH4GP23A1F1C-13G	IMHH4GP23A1F1C-13H
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		x72	x72	x72	x72
		4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)	4 Ranks (x8)
Label Code		PC3-8500P-7	PC3-8500P-8	PC3-10600P-8	PC3-10600P-9
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
142	Product Type, Char 15	2D	2D	2D	2D
143	Product Type, Char 16	31	31	31	31
144	Product Type, Char 17	30	30	33	33
145	Product Type, Char 18	46	47	47	48
146	Module Revision Code, LSB	3x	3x	4x	4x
147	Module Revision Code, MSB	xx	xx	xx	xx
148	DRAM Manufacturer's ID Code, LSB	85	85	85	85
149	DRAM Manufacturer's ID Code, MSB	51	51	51	51
150 - 175	Manufactures's Specific Data	00	00	00	00
176 - 255	Blank for Customer Use	FF	FF	FF	FF



6 Package Outline Diagrams

FIGURE 2
Package Outline LG-DIM-240-091 R/C A

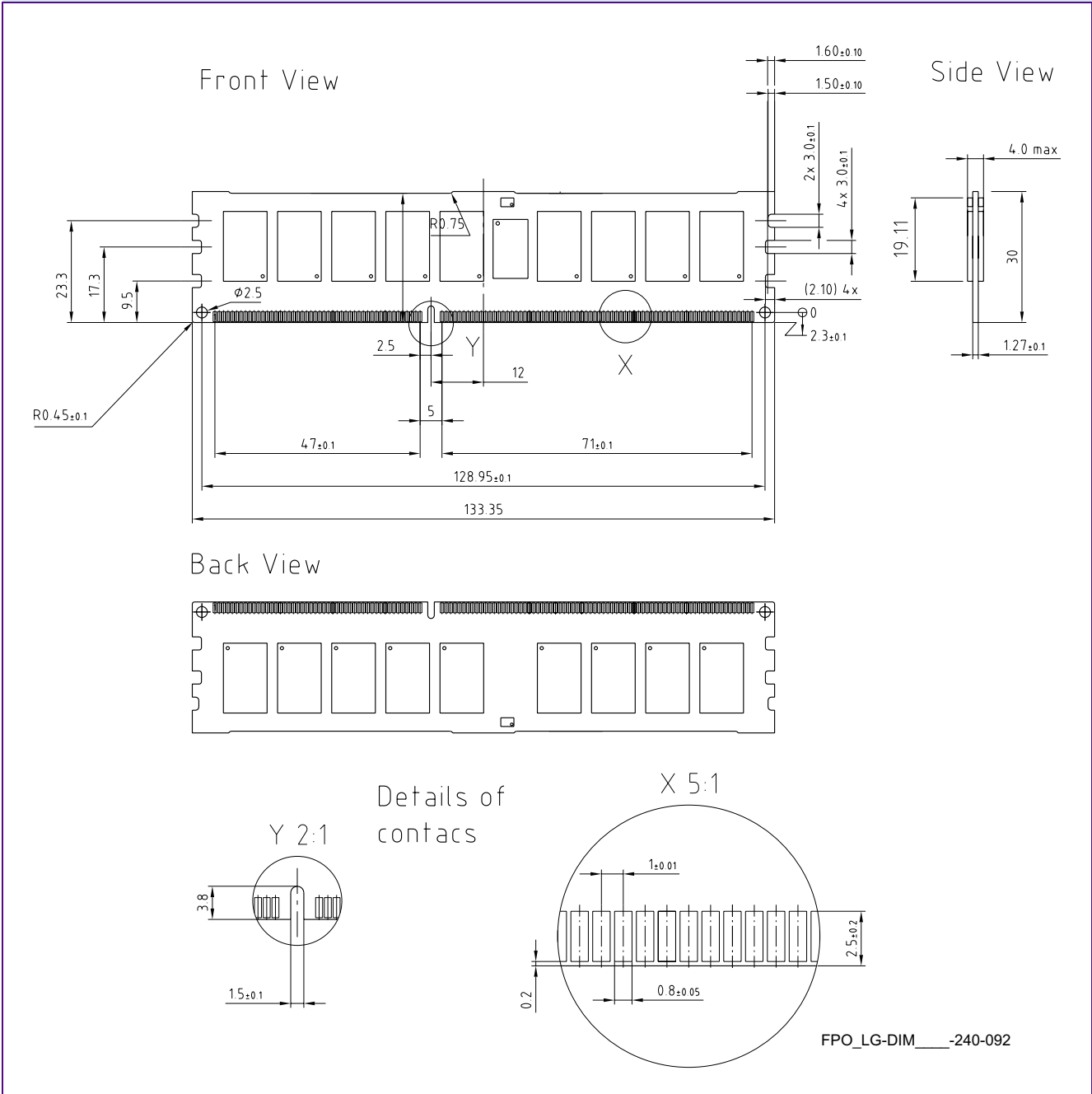


Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

FIGURE 3
Package Outline LG-DIM-240-092 R/C B

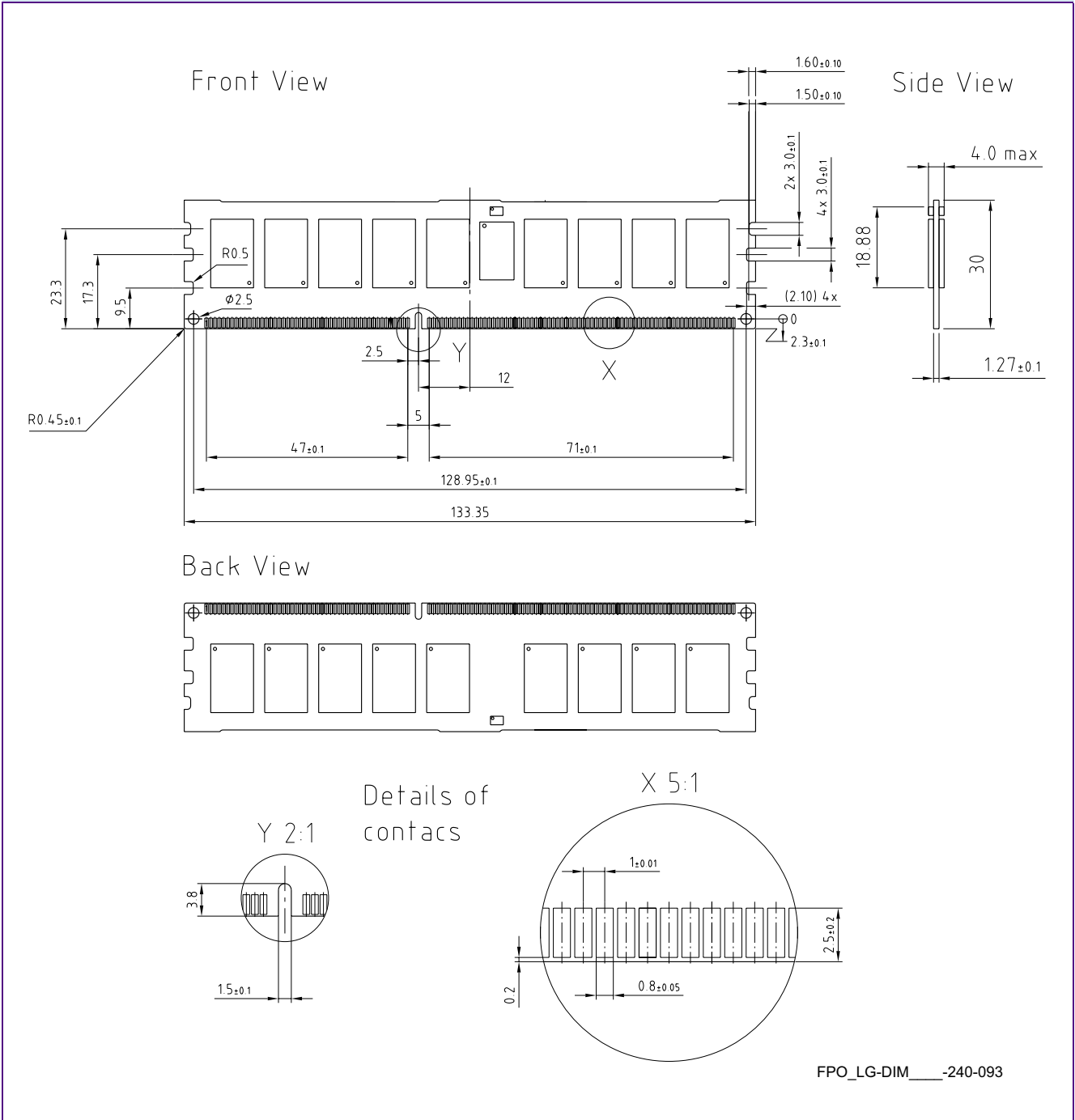


Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

FIGURE 4
Package Outline LG-DIM-240-093 R/C C



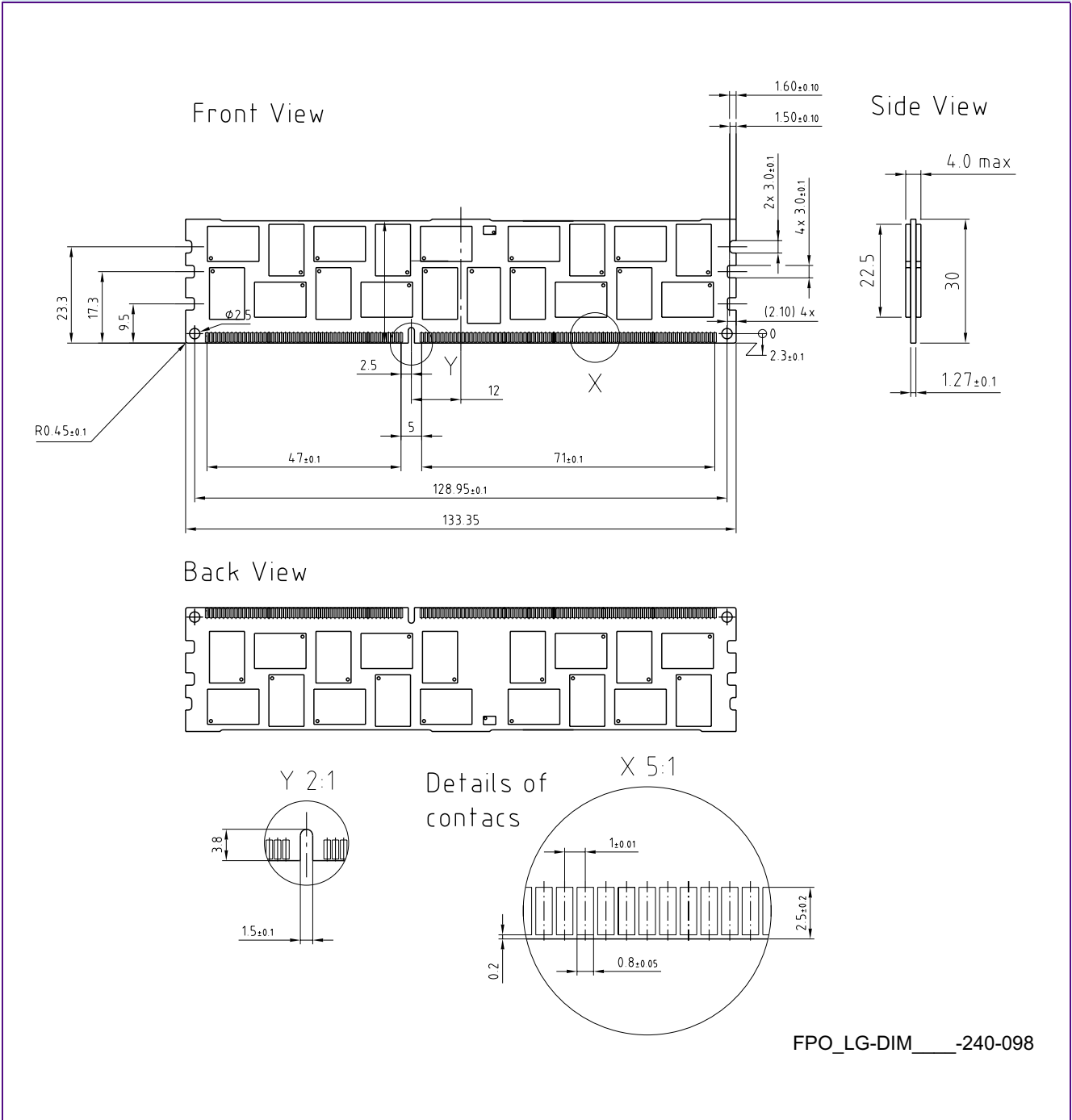
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Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

FIGURE 6
Package Outline LG-DIM-240-098 R/C H



Note: SDRAM component outlines are symbolic representation of the device placement. For actual SDRAM outline details please refer to SDRAM Component Data Sheet.



7 Product Type Nomenclature

For reference the applicable Qimonda DDR3 DIMM module nomenclature is listed in this chapter.

TABLE 24

Example: DDR3 1GByte Registered Module

Field Number	1+2	3	4	5+6	7	8	9	10+11	12+13	14	15	16+17	18
Qimonda Product Type	IM	S	H	4G	P	1	2	A1	F2	C	–	08	E

TABLE 25

DDR3 DIMM Nomenclature

Field	Description	Value	Coding
1+2	Qimonda Identifier	IM	Qimonda Memory modules
3	Power or Application	S	Standard
		H	Heat Spreader
		L	Low Power
4	Product Family	H	DDR3
5+6	Density	51	512 MBytes
		1G	1024 MBytes
		2G	2048 MBytes
		4G	4096 MBytes
7	Module Type / ECC Support	U	240 pin unbuffered DIMMs - Non-ECC
		E	240 pin unbuffered DIMMs - ECC
		S	204 pin Small Outline DIMMs - Non-ECC
		R	240 pin Registered DIMMs - ECC
		P	240 pin Registered DIMMs with Parity Bit - ECC
8	Number of Ranks	0	One Rank of SDRAMs
		1	Two Ranks of SDRAMs
		2	Four Ranks of SDRAMs
9	DRAM Device Number of IOs	2	x4 components (2 ²)
		3	x8 components (2 ³)
		4	x16 components (2 ⁴)
10+11	Die Revision	A1	First
12+13	Package	F1	Planar FBGA, lead- and halogen-free
		F2	Dual Die FBGA, lead- and halogen-free
14	Temperature Range	C	Commercial (0 °C - 95 °C)
15	Thermal Sensor	T	Modules with Thermal Sensor

DDR3 Registered DIMM
IM[S/H]H[1G/2G/4G]PxxA1F1C

Field	Description	Value	Coding
16+17	Band Width	08	PC3-6400, 6.4 GB/s, $t_{CK} = 2.5$ ns, $f_{CK} = 400$ MHz
		10	PC3-8500, 8.5 GB/s, $t_{CK} = 1.875$ ns, $f_{CK} = 533$ MHz
		13	PC3-10600, 10,66 GB/s, $t_{CK} = 1.5$ ns, $f_{CK} = 667$ MHz
		16	PC3-12800, 12,8 GB/s, $t_{CK} = 1.25$ ns, $f_{CK} = 800$ MHz
18	Latencies	D	CL-RCD-RP = 5-5-5
		E	CL-RCD-RP = 6-6-6
		F	CL-RCD-RP = 7-7-7
		G	CL-RCD-RP = 8-8-8
		H	CL-RCD-RP = 9-9-9
		J	CL-RCD-RP = 10-10-10



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