Military Products

Preliminary

32K x 8 RADIATION-HARDENED STATIC RAM-SOI HX6856

FEATURES

RADIATION

- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.8 µm Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^{11}$ rad(Si)/s
- Soft Error Rate of $<1x10^{-11}$ upsets/bit-day
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/s
- Latchup Free

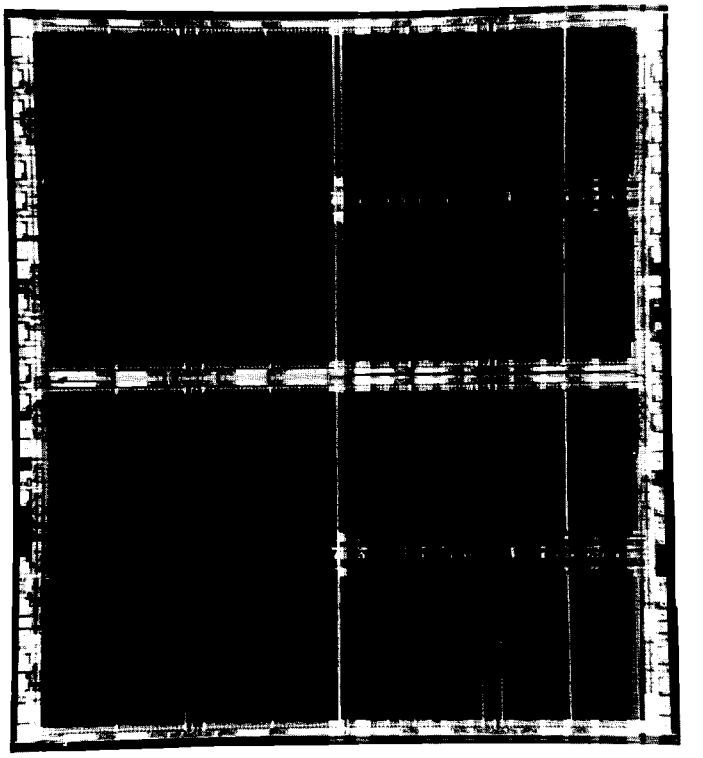
OTHER

- Read/Write Cycle Times
  ≤ 25 ns (-55 to 125°C)
- Optional Architectures
  - 64K x 4, 256Kx1
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Low Operating Power
- Packaging Options
  - 36-Lead Flat Pack (0.630 in. x 0.650 in.)
  - 28-Lead Flat Pack (0.530 in. x 0.720 in.)
  - 28-Lead DIP, MIL-STD-1835, CDIP2-T28

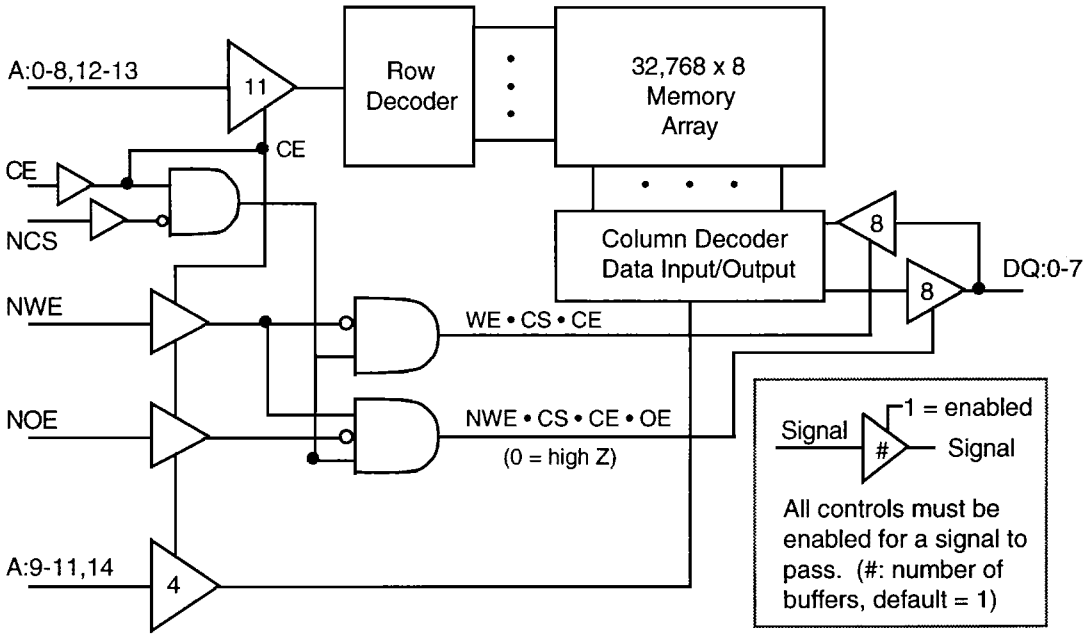
GENERAL DESCRIPTION

The 32K x 8 Radiation-Hardened Static RAM is a high performance 32,768 word x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation-hardened technology, and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. The RAM is available with either TTL or CMOS compatible I/O. Power consumption is typically less than 20 mW/MHz in operation, and less than 5 mW in the low power disabled mode. The RAM read operation is fully asynchronous, with an associated typical access time of 13 ns.

Honeywell's enhanced SOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ IV process is a 5-volt, SIMOX CMOS technology with a 150 Å gate oxide and a minimum feature size of 0.8 µm. Additional features include tungsten via plugs, Honeywell's proprietary SHARP planarization process, and a lightly doped drain (LDD) structure for improved short channel reliability. Cross-coupled Miller capacitors have been incorporated into the memory cell design for single event upset hardening.



FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-14 Address input pins which select a particular eight-bit word within the memory array.

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS Negative chip select, when at a low level allows normal read or write operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables the data input buffers only. If this signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level NWE allows normal read operation.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If this signal is not used it must be connected to VSS.

CE Chip enable, when at a high level allows normal operation. When at a low level CE forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE	NWE	NOE	MODE	DQ
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In
H	X	X	X	Deselected	High Z
X	L	XX	XX	Disabled	High Z

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications over the entire operating temperature range after a total ionizing radiation dose of $1x10^6$ rad(SiO_2). All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤1 µs duration up to $1x10^{11}$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), stiffening capacitance can be placed on the package between the package (chip) VDD and VSS, with the inductance between the package (chip) and stiffening capacitance kept to a minimum. If there are no operate-through or valid stored data requirements, typical de-coupling capacitors should be mounted on the circuit board as close as possible to each device.

The SRAM will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to $1x10^{12}$ rad(Si)/s, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The HX6856 SRAM has a soft error rate (SER) performance of $<1x10^{-11}$ upsets/bit-day, under recommended operating conditions. This hardness level is defined by the Adams 10% worst case cosmic ray environment.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate with its oxide isolation ensure latchup immunity.

RADIATION-HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1x10^6$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset	$\geq 1x10^{11}$	rad(Si)/s	Pulse width ≤1 µs
Transient Dose Rate Survivability	$\geq 1x10^{12}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.6 V, T_A=25°C
Soft Error Rate	$<1x10^{-11}$	upsets/bit-day	T_A=125°C, Adams 10% worst case environment
Neutron Fluence	$\geq 1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Positive Supply Voltage (2)		-0.5	6.5	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (3)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage (4)		2000		V
ΘJC	Thermal Resistance (Jct-to-Case)	28 FP/ 36 FP		2	°C/W
		28 DIP		10	
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

(2) Voltage referenced to VSS.

(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.

(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical (1)	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance			6	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance			8	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
VDR	Data Retention Voltage (3)		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current			500	µA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.

(2) Worst case operating conditions: TA= -55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.

(3) To maintain valid data storage during transient radiation, VDD must be held within the recommended operating range.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
IDDSB1	Static Supply Current				2.0	mA	VIH=VDD IO=0 VIL=VSS Inputs Stable
IDDSB2	Static Supply Current with Chip Disabled				2.0	mA	CE=VSS or NCS=VDD IO=0 VSS≤VI≤VDD (3)
IDDSEIL	Static Supply Current per Enabled Input*-Low				30	µA	VDD=5.5V, VIL=0.5V (3)
IDDSEIH	Static Supply Current per Enabled Input*-High				30	µA	VDD=5.5V, VIH=VDD-0.5V (3)
IDDOPW	Dynamic Supply Current, Selected (Write)				6.5	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (4)
IDDOPR	Dynamic Supply Current, Selected (Read)				5.0	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (4)
IDDOP1	Dynamic Supply Current, Deselected				400	µA	f=1 MHz, IO=0, VIL=VSS NCS=CE=VIH=VDD (4)
IDDOP2	Dynamic Supply Current, Disabled				20	µA	f=1 MHz, IO=0, VIH=VDD NCS=CE=VIL=VSS (4)
II	Input Leakage Current			-5	+5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current			-10	10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage	CMOS TTL			0.3xVDD 0.8	V V	March Pattern VDD = 4.5V
VIH	High-Level Input Voltage	CMOS TTL		0.7xVDD 2.2		V V	March Pattern VDD = 5.5V
VOL	Low-Level Output Voltage				0.4 0.05	V V	VDD = 4.5V, IOL = 10 mA VDD = 4.5V, IOL = 200 µA
VOH	High-Level Output Voltage			4.2 VDD-0.05		V V	VDD = 4.5V, IOH = -5 mA VDD = 4.5V, IOH = -200 µA

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.

(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.

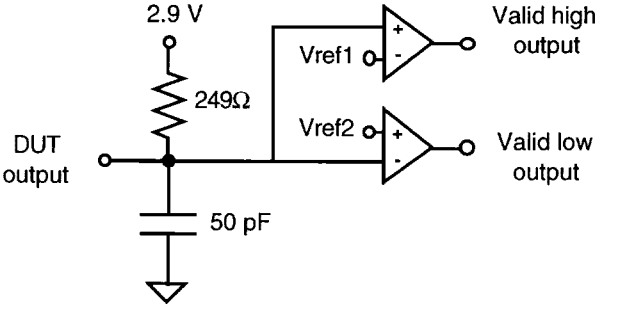
(3) Guaranteed but not tested

(4) All inputs switching. DC average current.

* ENABLED INPUT PINS TRUTH TABLE

CE	NCS	NWE	# of enabled input pins
H	L	L	28
H	L	H	20
H	H	X	20
L	X	X	2

X: VI = VIH OR VIL

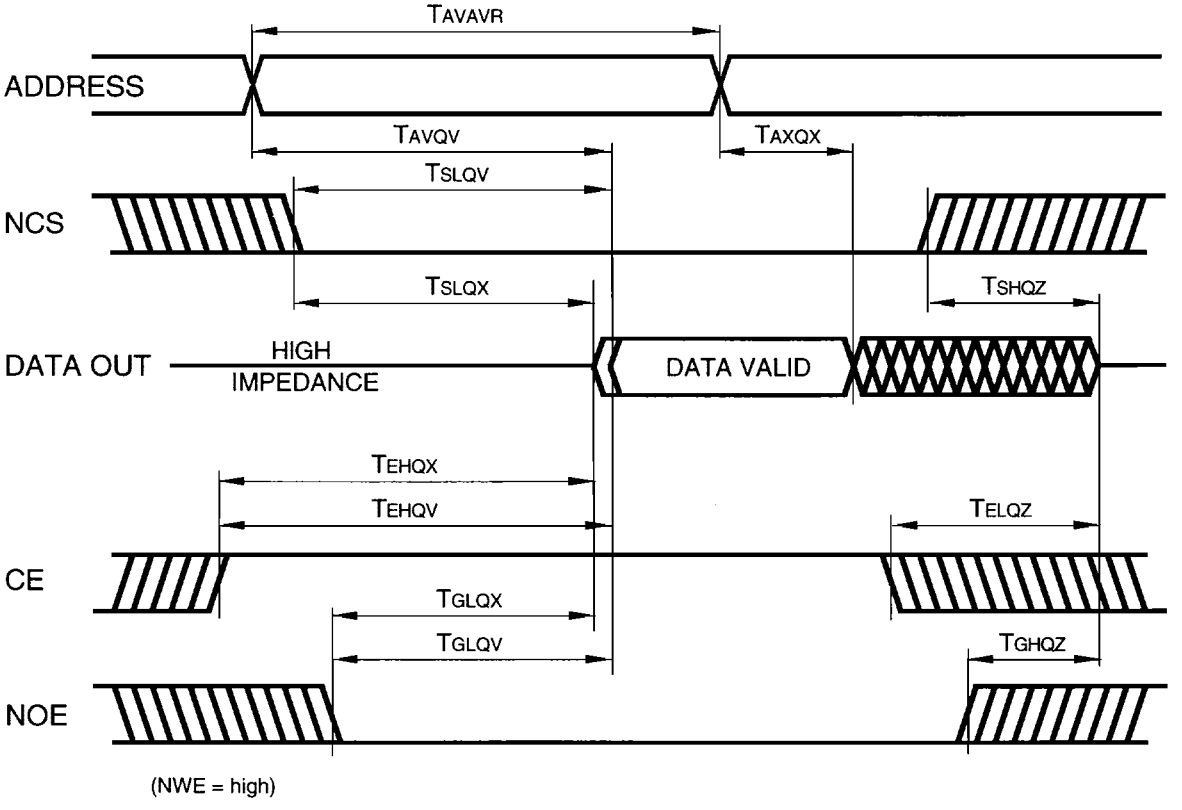


Tester Equivalent Load Circuit

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAV	Address Read Cycle Time		25		ns
TAVQV	Address Access Time			25	ns
TAXQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			25	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			10	ns
TEHQV	Chip Enable Access Time			28	ns
TEHQX	Chip Enable Output Enable Time		5		ns
TELQZ	Chip Enable Output Disable Time			10	ns
TGLQV	Output Enable Access Time			9	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			9	ns

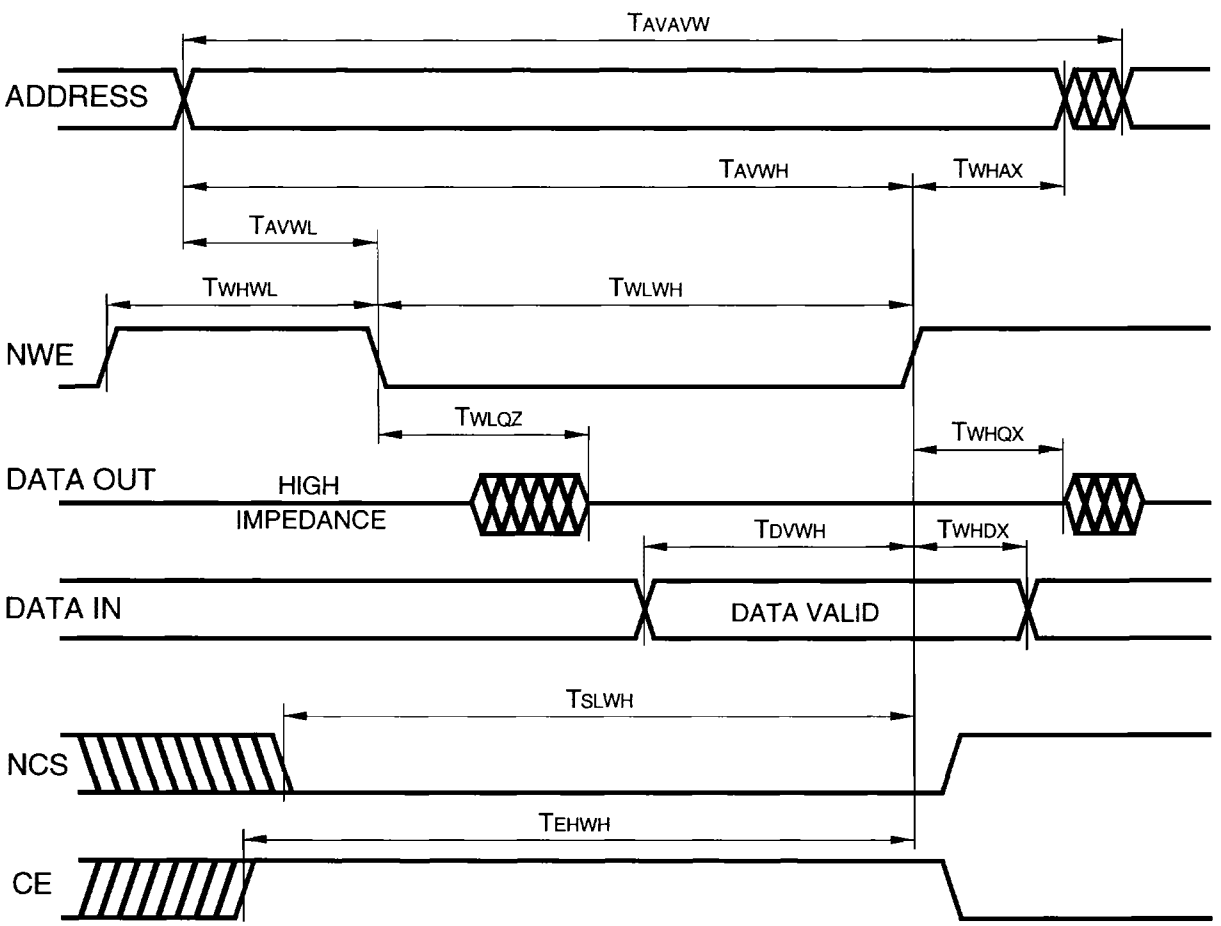
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading C_L=50 pF. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through 1x10^6 rad(SiO_2) at 25°C.



WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Max	Units
TAVAV	Write Cycle Time (4)		25		ns
TWLWH	Write Enable Write Pulse Width		20		ns
TSLWH	Chip Select to End of Write Time		20		ns
TDVWH	Data Valid to End of Write Time		15		ns
TAVWH	Address Valid to End of Write Time		20		ns
TWHDX	Data Hold Time after End of Write Time		0		ns
TAVWL	Address Valid Setup to Start of Write Time		0		ns
TWHAX	Address Valid Hold after End of Write Time		0		ns
TWLQZ	Write Enable to Output Disable Time		0	9	ns
TWHQX	Write Disable to Output Enable Time		5		ns
TWHWL	Write Disable to Write Enable Pulse Width		5		ns
TEHWH	Chip Enable to End of Write Time		23		ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading=50 pF.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, total dose through $1x10^6$ rad(SiO_2) at 25°C.
(4) TAVAV = TWLWH + TWHWL



DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

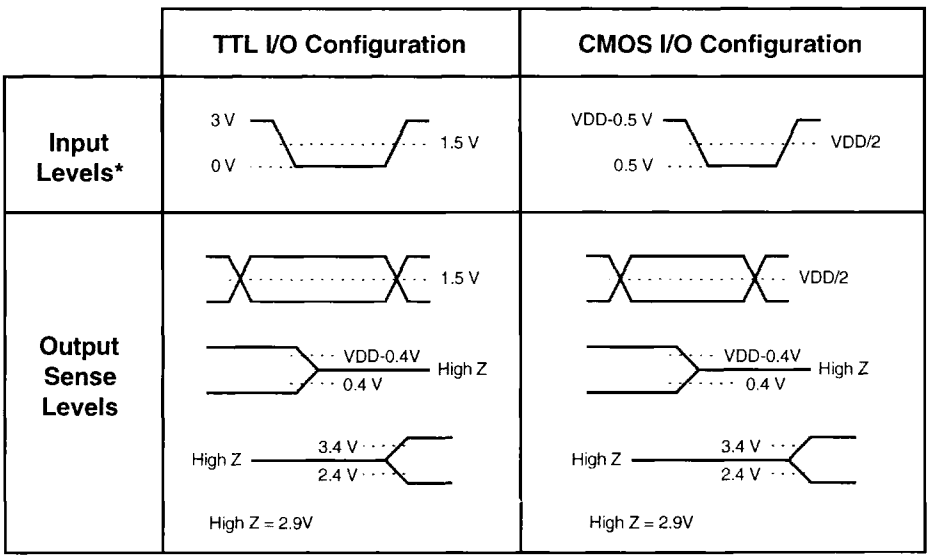
Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. NCS differs from CE in that it does not dissable the input buffers. However, both CE and NCS fully disable the RAM decode logic for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity. However, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times <5 ns

QUALITY AND RADIATION-HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," a computer data base process performance tracking system, and a radiation-hardness assurance strategy.

The radiation-hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883C TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. "Engineering Devices" are available with varying degrees of limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883.

RELIABILITY

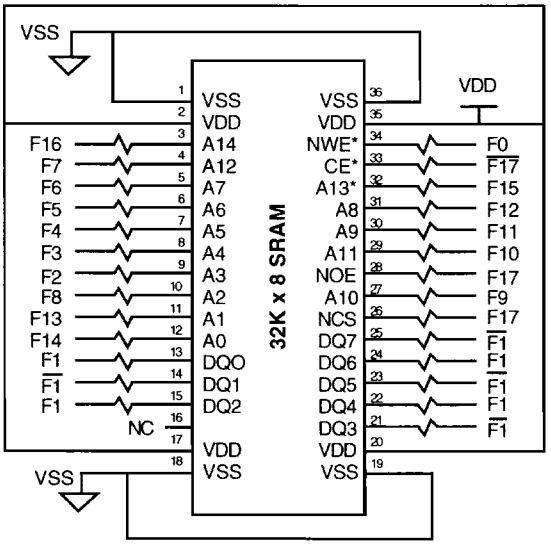
Honeywell understands the exceptional reliability requirements for space and defense systems and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883C, TM 5005, class S. The product is qualified by following a screening and testing flow to meet the customer's requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

HONEYWELL STANDARD ASSEMBLY AND SCREENING PROCEDURE

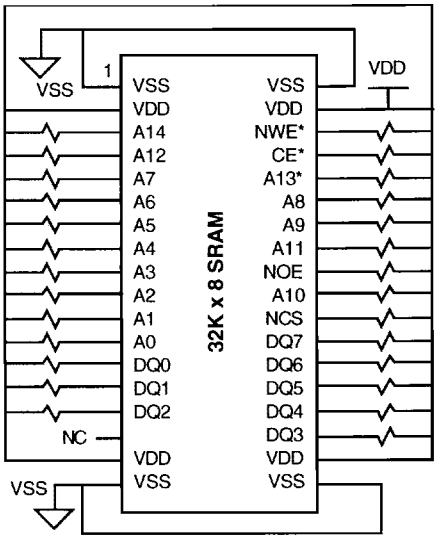
Procedure	Engineering Device	Honeywell Level S*
Die Attach	X	X
Die Adhesion Test, M2019		X
Destructive Wire Bond Pull Test, M2011		X
Non-Destructive Wire Bond Pull-Test, M2023		X
Q.A. Pre-Cap Visual, M2010 Condition A	Commercial	X
Clean, Bake, Lid Seal	X	X
Package Marking/Serialization	X	X
Temperature Cycle, M1010 Condition C		X
Constant Acceleration, M2001 Condition E		X
PIND, M2020 Condition A		X
Radiography, M2012		X
Lead Trim	X	X
Pre-Conditioning Electrical Test, -55, 25, 125°C	X	X
Pre-Conditioning Burn-in, M1015 Cond D, 24 hrs, 6.5V, 125°C	X	X
Post-Conditioning Burn-In Electrical Test, -55, 25, 125°C	ED3 & 4 @25°C only	X
Static Burn-In, M1015 Cond C, 72 hrs, 5.5V, 150°C		X
Interim Electrical Test, 25°C		X
Dynamic Burn-In, M1015 Condition D, 240 hrs, 6.5V, 125°C		X
Final Electrical Test, -55, 25, 125°C		Within 96 hrs at 25°C
PDA		X
Leak Check, M1014, Fine-Cond A1, Gross-Cond C1		X
QA External Visual, M2009	Commercial	X
QCI, M5005		As Requested

* Product is fabricated and screened to Class S intent. Responsibility for DPA resides with the customer. Screening and QCI flow charts are available upon request. European flow based on ESA/SCC 9000 level B or other program specific screening flow is available upon request.



DYNAMIC BURN-IN DIAGRAM

VDD = 6.5V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.



STATIC BURN-IN DIAGRAM

VDD = 5.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

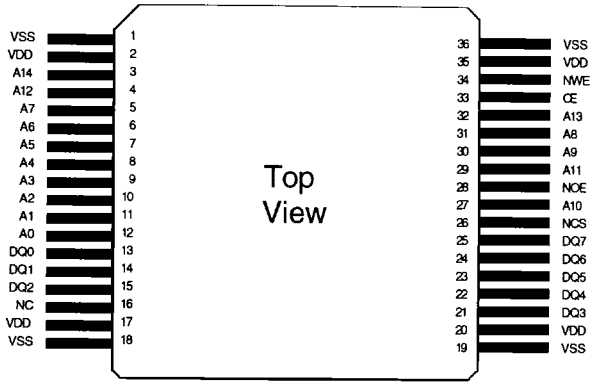
NOTE - *Denotes package pinout option dependent
(28-Lead DIP/FP diag. not shown but has similar connections)

PACKAGING

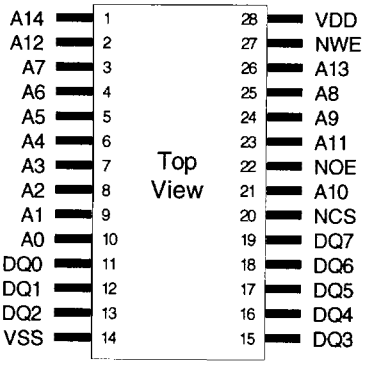
The 32K x 8 SOI SRAM is offered in a custom 36-lead FP, 28-lead FP, or standard 28-lead DIP. Both packages are constructed of multilayer ceramic (Al_2O_3) and feature internal power and ground planes. The 36-lead FP also features a non-conductive ceramic tie bar on the lead frame. The purpose of the tie bar is to allow electrical testing of the device, while preserving the lead integrity during shipping and handling, up to the point of lead forming and insertion.

Optional capacitors can be mounted to the package to maximize supply noise decoupling and increase board packing density. These capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either VDD, VSS or an active driver to prevent charge build up in the radiation environment. (NC = no connect)

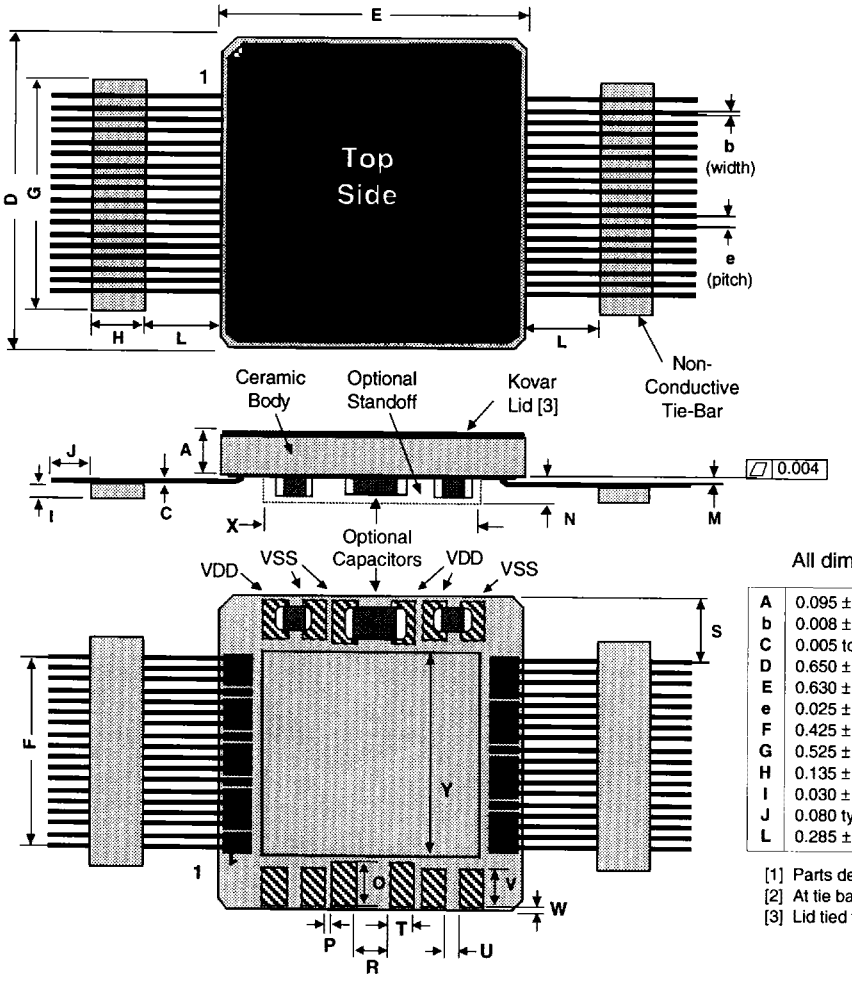
36-LEAD FLAT PACK PINOUT



28-LEAD DIP &FP PINOUT



36-LEAD FLAT PACK



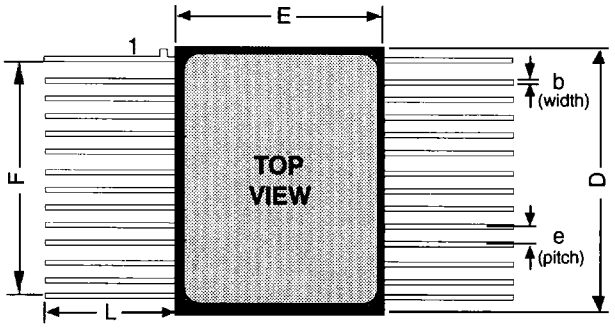
All dimensions are in inches [1]

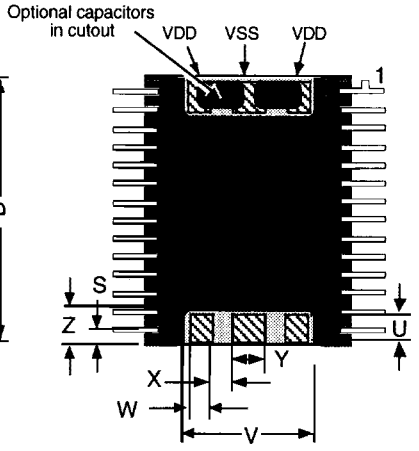
A	0.095 ± 0.010	M	0.008 ± 0.003
b	0.008 ± 0.002	N	0.050 ± 0.010
C	0.005 to 0.0075	O	0.090 ref
D	0.650 ± 0.010	P	0.015 ref
E	0.630 ± 0.007	R	0.075 ref
e	0.025 ± 0.002 [2]	S	0.113 ± 0.010
F	0.425 ± 0.005 [2]	T	0.050 ref
G	0.525 ± 0.005	U	0.030 ref
H	0.135 ± 0.005	V	0.080 ref
I	0.030 ± 0.005	W	0.005 ref
J	0.080 typ.	X	0.450 ref
L	0.285 ± 0.015	Y	0.400 ref

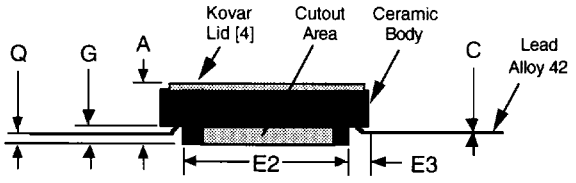
[1] Parts delivered with leads unformed
[2] At tie bar
[3] Lid tied to VSS

HX6856

28-LEAD FLAT PACK







All dimensions in inches

A	0.135 ± 0.015
b	0.015 ± 0.002
C	0.004 to 0.009
D	0.720 ± 0.008
e	0.050 ± 0.005 [1]
E	0.530 ± 0.008
E2	0.420 ± 0.008
E3	0.055 ref
F	0.650 ± 0.005 [2]
G	0.050 ± 0.005
L	0.295 min [3]
Q	0.026 to 0.045
S	0.035 ± 0.010
U	0.065 ref
V	0.300 ref
W	0.050 ref
X	0.030 ref
Y	0.100 ref
Z	0.080 ref

[1] BSC - Basic lead spacing between centers
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid connected to VSS

28-LEAD DIP

For 28-Lead DIP description, see MIL-STD-1835, Type CDIP2-T28, Config. C, Dimensions D-10

ORDERING INFORMATION

H — **SOURCE**
H=HONEYWELL

X — **PROCESS**
X=SIMOX

6856/1 — **PART NUMBER**
Pinout options (2)

X — **PACKAGE DESIGNATION**
W=36-Lead FP
X=36-Lead FP, with standoff
Y=36-Lead FP, with standoff & caps
N=28-Lead FP
P=28-Lead FP, with caps
R=28-Lead DIP
S=28-Lead DIP, with caps
- = Bare die (No Package) (3)

S — **SCREEN LEVEL**
S=Level S (1)
B=Level B (3)
1=ED1
2=ED2
3=ED3
4=ED4
(4)

H — **TOTAL DOSE HARDNESS**
H=1x10^6 rad(SiO$_2$)
R=2x10^5 rad(SiO$_2$)
N=No Level Guaranteed

Y — **SOFT ERROR RATE**
Y = <1x10^{-11} upsets/bit-day
- = No SER Guaranteed

C — **INPUT BUFFER TYPE**
C=CMOS Level
T=TTL Level

(1) Refer to Standard Assembly and Screening Procedure section for Honeywell's screening procedures.
(2) Pinout options:

	36-Lead FP			28-Lead FP & DIP
	pin 32	pin 33	pin 34	
HX6856/1	A13	CE	NWE	JEDEC Pinout
HX6856/2	CE	NWE	A13	N/A

(3) Contact factory for availability.
(4) Engineering Device (ED) code descriptions:
ED1: -55 to 125°C limits, Total Dose not guaranteed but SER guaranteed
ED2: -55 to 125°C limits, Total Dose & SER specification not guaranteed
ED3: 25°C limits, meets Total Dose & SER specification
ED4: 25°C limits, Total Dose & SER specification not guaranteed

Honeywell

Helping You Control Your World