Quint Line Receiver with Differential I/O

Description

The CXB1103Q is an ultra high speed monolithic ECL IC, which contains five differential line receivers with a built-in reference voltage supply (V_{BB}). With V_{BB} tied to one of the input pins of each differential input pair, each gate can be used as a single input line receiver.

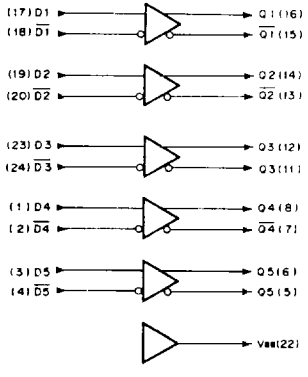
Features

- Typical AC characteristics T_{pd}=430ps, T_{TLH}=220ps, T_{THL}=170ps
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential I/O

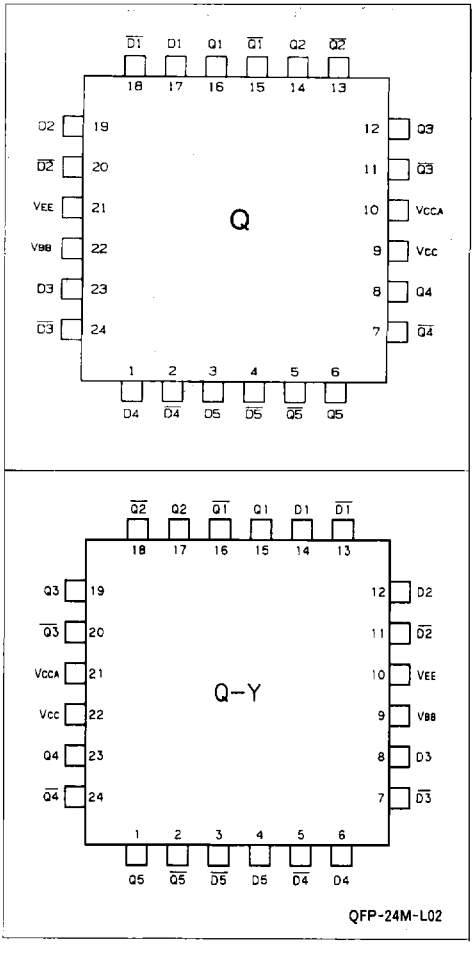
Pin Names

Dn, $\overline{Dn}$	Data inputs
Qn, $\overline{Qn}$	Data outputs
V_{BB}	Reference voltage output
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment



DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−154	−113	−79	mA
Min. differential input voltage*1	Vp-p			50		mVpp

Note: Other DC characteristics; See pages 3-3 and 3-4.

*1: Minimum voltage required to obtain full logic swing on output

AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	Dn	Qn		310	410	520	ps
	T_{PHL}				320	430	540	
Gate-to-Gate skew	$T_{SG\cdot G}$					50	90	
Rise time	T_{TLH}			20% to 80%		220	280	
Fall time	T_{THL}					170	220	

Note: AC test circuit; See page 4-3.

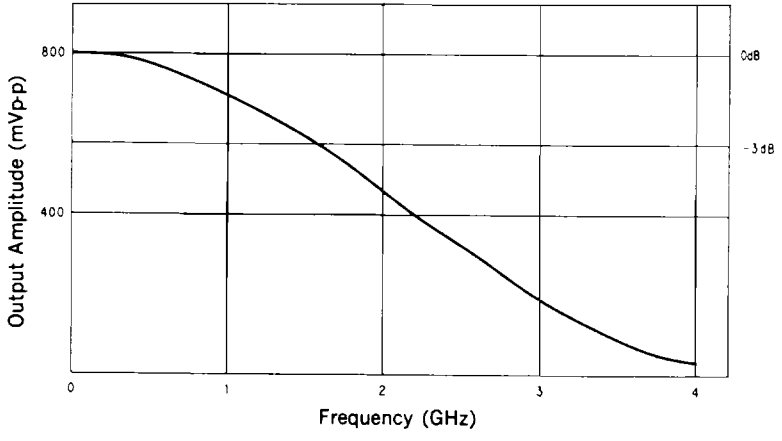


Figure 1. Frequency characteristics