Integrated Device Technology, Inc.

R3000 CPU MODULES FOR HIGH PERFORMANCE AND MULTIPROCESSOR SYSTEMS

IDT7RS107

FEATURES:

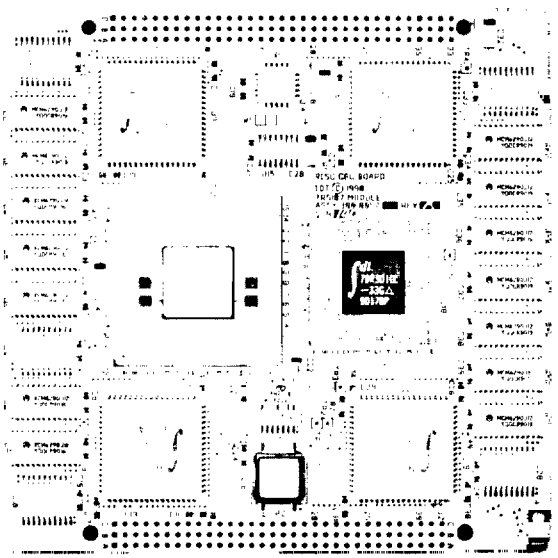
- **Cache Size: 64K Instruction, 64K Data**
- **Processor Speeds up to 33 MHz**
- **Includes R3010 Floating Point Accelerator**
- **1-word Read Buffer; 4-word Write Buffer**
- **Supports R3000 Multiprocessor Features**
- **Entire I-Cache can be invalidated with external cache reset signal**
- **Eight-word block refills**
- **On-board oscillator, delay line, and reset circuitry**
- **100% burn-in and functional test at rated speed**

R3000 MODULE FOR HIGH PERFORMANCE CPUs AND MULTIPROCESSOR SYSTEMS:

The IDT7RS107 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 64 Kbytes each of data and instruction cache memory, a single word read buffer and a four-word write buffer. Clock generation, reset, control and interrupt functions are included on the module to simplify the remainder of the system design.

The 107 module is designed to support the R3000's multiprocessor features. Data in the D-cache can be invalidated by the R3000 CPU. It is also possible to invalidate the entire contents of the I-cache in a single cycle by using an external cache reset signal.

The module is constructed using surface mount devices on a 5.2" by 5.2" epoxy laminate board, and is connected to the user's system via 195 pins located in two pin row regions on the board.



7RS107 Module. Actual Size 5.2" x 5.2 "

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ARCHITECTURAL HIGHLIGHTS

Uses R3020 Write Buffers

R3020 chips are used on the module to provide a "smart" four-deep write buffer between the CPU and external memory. These devices store data and addresses for up to four write requests to main memory, and handle the handshaking with the memory controller. The R3020s support features such as byte gathering (combining multiple byte writes to the same address in the buffer into a single write) and address matching (a read or write to an address already in the write buffer will be detected so the user software can take appropriate action). The R3020's Match signals are OR'ed on the module to produce a single output, labeled CONFLICT.

Resettable Instruction Cache

The 7RS107 module permits invalidation of the entire instruction cache via a "cache reset" pin on the module. This feature is used to wipe the cache clean when the a block of instructions in main memory have been changed by a DMA operation. It is usually much faster than invalidating each affecting tag individually.

Multiprocessor Invalidate In Data Cache

The module supports the R3000's multiprocessor cache invalidate feature, so that data cache coherency can be maintained when data held in the cache is altered externally. The R3000's MP Stall and MP Invalidate signals are available as pins on the module. The user's system stalls the processor and then provides an address to the module while signaling MP Invalidate. The module stores the address in a latch and applies it to the cache at the right time for the R3000 to invalidate the referenced tag.

Eight-Word Block Refill

The module refills both the instruction and data caches from memory in eight-word blocks. Following a cache miss, the processor will request a memory read at the missed address and wait for a data ready acknowledgement. When an acknowledge is received, the processor will load eight words into cache on eight successive clock cycles. The memory interface must supply the correct eight words (address A4A3A2 = 0 to 7) at the processor's speed, 40 ns intervals for a 25 MHz system. Interleaved memory is usually the best way to support this requirement. The processor's CPC0 pin, available as a pin on the module, can be used to over-ride the block refill on data, but instructions refills must always be in 8-word blocks. The processor performs instruction streaming during the refill.

On-board Oscillator and Delay Line

All the clock generation circuitry required by the R3000 system is on the module. A jumper can be used to select between the on-board crystal oscillator or an external oscillator input. A delay line on the module is used to set the timing for register strobes and other critical signals relative to the R3000 clock. The R3000 clock output "SYSOUT" is made available to the user system through eight pins on the module, each independently buffered.

R3000 Reset and Initialization Logic

The initialization logic for the R3000 CPU is contained on the module. A "Cold Reset" pin on the module starts the required 15 ms reset signal to the CPU, and then provides the initialization vectors during the last few cycles. A second reset pin is provided to reinitialize the CPU without repeating the 15 ms delay. The R3000 is initialized to "Big-Endian" operation.

Five User Interrupt Lines

Five pins on the module are used for user interrupt inputs. The user interrupts are synchronized in registers on the module before being sent to the R3000. Interrupt 2 is used for the Floating Point Accelerator, if present.

External R3000 Condition Code Pin

The R3000 input CPC0 is available as a pin on the module. During initialization, this pin is programmed as a Condition Code test pin, so the R3000 can do a Test and Branch in a single cycle based on its state. During read stalls, the pin determines whether a single word or 8 words will be read. Reads into the instruction cache must always be block refills.

TYPICAL APPLICATIONS

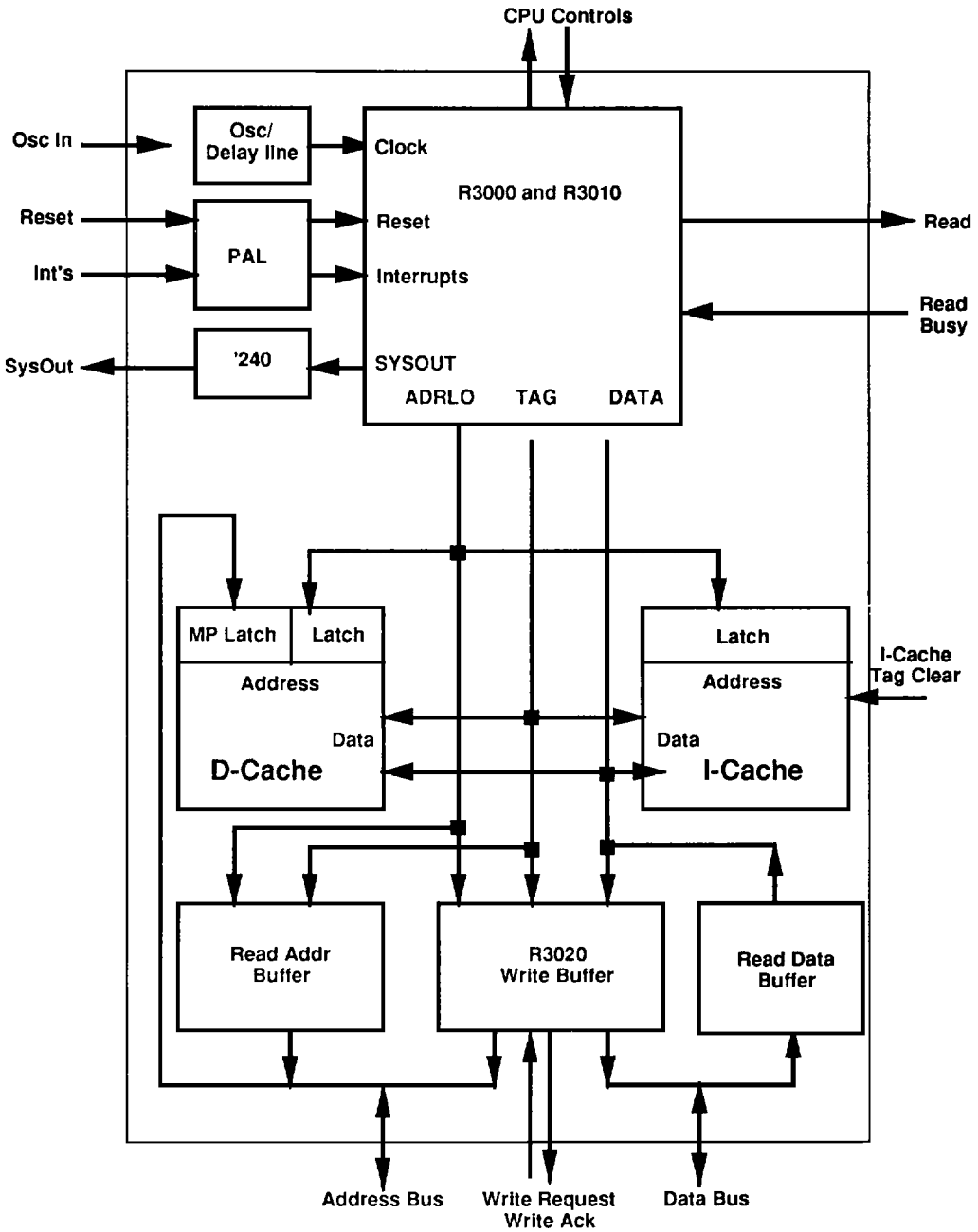
The 7RS107 module is designed for applications that run complex operating systems, such as UNIX™, or that need outside control of cache memory contents, such as multiprocessor systems.

The module supports the R3000's ability to invalidate entries in the data cache, allowing multiple processor systems to maintain cache coherency.

The module is offered with the maximum possible cache sizes (64K each) that can be supported by the R3000 in a multiprocessor configuration. These sizes are well suited to running UNIX at very high instruction rates as well.

The R3020 Write Buffer is used to provide a four-word deep write buffer, which is ideal for most UNIX systems.

FUNCTIONAL BLOCK DIAGRAM



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SIGNALS PROVIDED ON MODULE PINS

Signal Name	Type	Description
MA0...MA31	I/O	32-bit address from the module to external memory. This is an output from the 3020 Write Buffer except during the MP Invalidate function, when it is the input to the MP cache address latch.
MD0...MD31	I/O	32-bit data bus between the module and external memory. Driven from the 3020 Write Buffer during writes; input to the Read Data Buffer during reads.
BACT0,1,2	O	The three R3000 AccType status signals, driven from the 3020 Write Buffer during writes and from a latch during reads.
MDP0...MDP3	I/O	The four parity bits for the MD data. Output during writes and input during reads.
CP_CpCond0, 2, 3	I	The three flag inputs to the R3000 CPU. CPC0 is used during read stalls to control block refill of the data cache. (The instruction cache must always be block refilled.) CPC2 and CPC3 are the MP stall and invalidate controls.
ALOE	I	Data Cache Address Latch Output Enable When LOW, enables the output of the latch holding the data cache address supplied by the R3000. It should be LOW at all times except when the MP Latch is being used to invalidate a cache address.
MPALOE	I	Data Cache MP Address Latch Output Enable. This input is used to enable the output of the latch holding the address supplied by the user system during an MP stall cycle. It should be enabled (LOW) only during the MP invalidate operation.
BSYSOUT2...9	O	Eight buffered inverted copies of the R3000 signal "SYSOUT" for use in the user's system.
UINT0,1,3,4,5	I	Interrupt inputs to the R3000. These signals are synchronized to SYSOUT on the module. R3000 interrupt 2 is used for the Floating Point Accelerator.
BRESET	O	Buffered copy of the reset signal created on the module to reset the CPU. LOW during Reset.
WB_WbFull	O	Write Busy. Status signal created by the R3020 write buffer. Goes LOW to indicate the buffer is full.
CPU_BusError	I	Input to the R3000 indicating a bus error has occurred.
RESETC	I	Cold Reset to the module. The module creates a 15 ms long reset to the R3000 and executes the R3000 initialization sequence when this pin goes LOW.
FP_FpPresent	O	This signal can be used to detect the presence of an FPA on the module. To be used, it must be connected to a 4.7K pullup resistor. The pin will be LOW if the FPA is present.
RESETI	I	Active LOW asynchronous clear to the I-Cache Tag RAMS. Sets the entire I-Cache invalid.
WB_OutEn	I	Write Buffer Output Enable. When LOW, turns on the outputs of the R3020 write buffers.
WB_Request	O	Output from the R3020 to indicate that there is data in the buffer to be written to memory. Active LOW
WB_Acknowledge	I	Input to the R3020 to indicate data has been written into memory.
CONFLICT	O	The OR of all the R3020 Match signals; indicates the address on the R3020 inputs matches one of the addresses currently in the write buffer.
RABOE	I	Read Address Buffer Output Enable. When LOW, turns on outputs of the buffers containing the read address.
RDBCE	I	Read Data Buffer Clock Enable. When LOW, enables the clock (SYSOUT) to the Read Data Buffers.
READ	O	Status signal output. LOW during reads.
RABLE	I	Read Address Buffer Latch Enable. When HIGH, enables the Read Address Buffer latches.
WB_LatchErrAddr	I	Latch Error Address input to the R3020.
WB_EnErrAddr	I	Enable Error Address input to R3020.
CP_MemRd	O	R3000 output signal. When LOW, there is a request for a read from external memory.
CP_RdBusy	I	Read Busy. Input to the R3000 to indicate acknowledgment of the MEMRD request.
RESETX	I	Additional Reset command. Same as RESETC, but does not go through the 15 ms delay. Can be used to re-initialize the R3000 when power is on.

RELATED PRODUCTS

Prototyping System

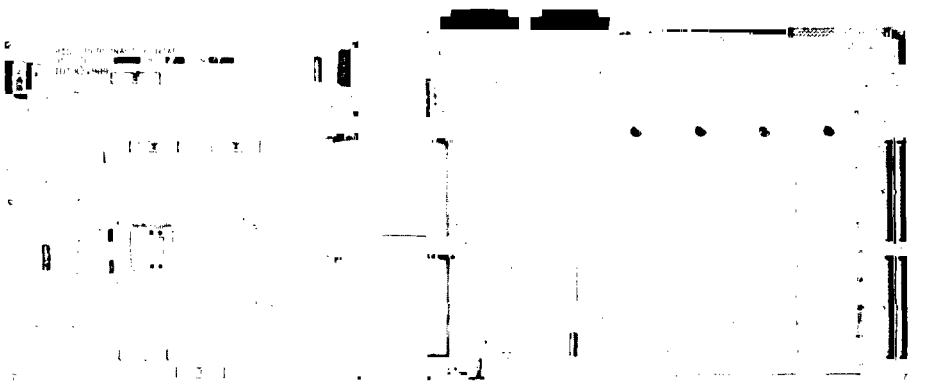
The 7RS107 module can be placed into immediate service using our flexible 7RS307 Prototyping Platform. The system includes two boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1Mb of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's Software Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP 16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



A Module Prototyping Platform.
The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

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ORDERING INFORMATION

Ordering Part Number	CPU	FPA	I-cache	D-cache	Speed	Other
7RS107N66A16A	R3000A	NONE	64K	64K	16 MHz	
7RS107N66A20A	R3000A	NONE	64K	64K	20 MHz	
7RS107N66A25A	R3000A	NONE	64K	64K	25 MHz	
7RS107N66A33A	R3000A	NONE	64K	64K	33 MHz	
7RS107F66A16A	R3000A	R3010A	64K	64K	16 MHz	
7RS107F66A20A	R3000A	R3010A	64K	64K	20 MHz	
7RS107F66A25A	R3000A	R3010A	64K	64K	25 MHz	
7RS107F66A33A	R3000A	R3010A	64K	64K	33 MHz	

CUSTOM OPTIONS

Some features of the 7RS107 can be modified by special order. Contact your IDT sales office for details.

Software modifications include: initialization mode for the R3000, endian option, size of block refill, instruction streaming option.

Manufacturing options include pin length, style, and plating; special marking; additional burn-in, and socketing of the CPU and/or FPA.