

Summary of Virtex[®]-II Features

- Industry First Platform FPGA solution IP-Immersion[™] architecture
 - Densities from 40K to 10M system gates
 - 420 MHz internal clock speed (Advance Data)
 - 840+ Mb/s I/O (Advance Data)
- SelectRAM[™] Memory Hierarchy
 - 3.5 Mb of True Dual-Port[™] RAM in 18-Kbit block SelectRAM resources
 - Up to 1.9 Mb of distributed SelectRAM resources
 - High-performance interfaces to external memory
 - 400 Mb/s DDR-SDRAM interface (Advance Data)
 - 400 Mb/s FCRAM interface (Advance Data)
 - 333 Mb/s QDR[™]-SRAM interface (Advance Data)
 - 600 Mb/s Sigma RAM interface (Advance Data)
- Arithmetic Functions
 - Dedicated 18-bit x 18-bit multiplier blocks
 - Fast look-ahead carry logic chains
- Flexible Logic Resources
 - Up to 122,880 internal registers / latches with Clock Enable
 - Up to 122,880 look-up tables (LUTs) or cascadable 16-bit shift registers
 - Wide multiplexers and wide-input function support
 - Horizontal cascade chain and Sum-of-Products support
 - Internal 3-state bussing
- High-Performance Clock Management Circuitry
 - Up to 12 DCM (Digital Clock Manager) modules
 - Precise clock de-skew
 - Flexible frequency synthesis
 - High-resolution phase shifting
 - EMI reduction
 - 16 global clock multiplexer buffers
- Active Interconnect[™] Technology
 - Fourth generation segmented routing structure
 - Predictable, fast routing delay, independent of fanout
- SelectI/O-Ultra[™] Technology
 - Up to 1,108 user I/Os
 - 19 single-ended standards and six differential standards
 - Programmable sink current (2 mA to 24 mA) per I/O
- XCITE[™] Digital Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
- PCI-X @ 133 MHz, PCI @ 66 MHz and 33 MHz compliance
- Differential Signaling
 - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
 - Bus LVDS I/O
 - Lightning Data Transport (LDT) I/O with current driver buffers
 - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
 - Built-in DDR Input and Output registers
- Proprietary high-performance SelectLink[™] Technology
 - High-bandwidth data path
 - Double Data Rate (DDR) link
 - Web-based HDL generation methodology
- Supported by Xilinx Foundation[™] and Alliance[™] Series Development Systems
 - Integrated VHDL and Verilog design flows
 - Compilation of 10M system gates designs
 - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
 - Fast SelectMAP[™] configuration
 - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
 - IEEE1532 support
 - Partial reconfiguration
 - Unlimited re-programmability
 - Readback capability
- Power-Down Mode
- 0.15 μ m 8-Layer Metal process with 0.12 μ m high-speed transistors
- 1.5 V (V_{CCINT}) core power supply, dedicated 3.3 V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 compatible boundary-scan logic support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) packages in three standard fine pitches (0.80mm, 1.00mm, and 1.27mm)
- 100% factory tested

Table 1: Virtex-II Field-Programmable Gate Array Family Members

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18-Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108
XC2V10000	10M	128 x 120	61,440	1,920	192	192	3,456	12	1,108

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15µm / 0.12µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 12 members, ranging from 40K to 10M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80mm, 1.00mm, and 1.27mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-Chip construction offers the combination of high pin count with high thermal capacity.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 41 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: Maximum Number of User I/O Pads

Device	Wire-Bond	Flip-Chip
XC2V40	88	
XC2V80	120	
XC2V250	200	
XC2V500	264	
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	456	624
XC2V3000	516	720
XC2V4000		912
XC2V6000		1,104
XC2V8000		1,108
XC2V10000		1,108

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in [Figure 1](#), the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

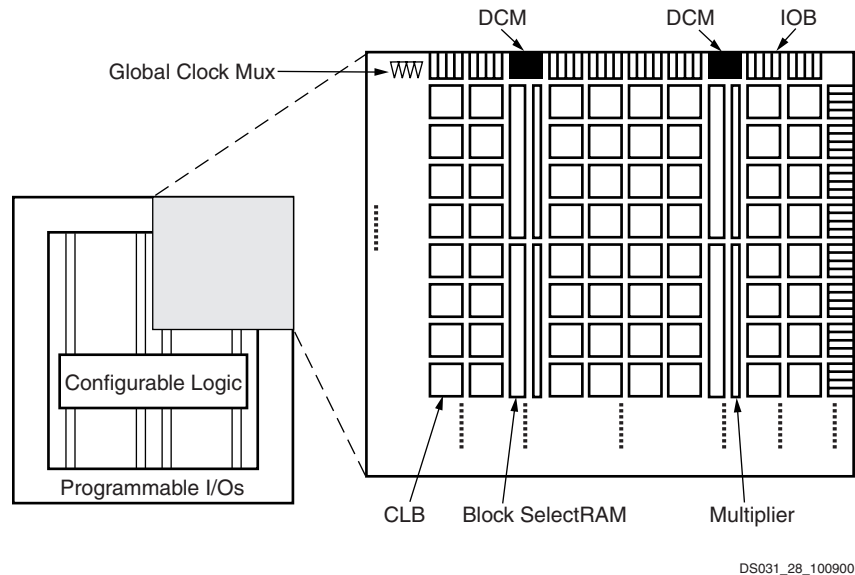


Figure 1: Virtex-II Architecture Overview

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18-Kbit storage elements of True Dual-Port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse and fine-grained clock phase shifting, and electromagnetic interference (EMI) reduction.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the

general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bi-directional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS (3.3 V, 2.5 V, 1.8 V, and 1.5 V)
- PCI-X at 133 MHz, PCI (3.3 V at 33 MHz and 66 MHz)

- GTL and GTLP
- HSTL (Class I, II, III, and IV)
- SSTL (3.3 V and 2.5 V, Class I and II)
- AGP-2X

The digital controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in [Table 3](#).

Table 3: Dual-Port And Single-Port Configurations

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where $1 \leq M \leq 4096$ and $1 \leq D \leq 4096$. For the exact timing parameters, see "[Virtex-II Electrical Characteristics](#)" on page 76.

Virtex-II devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 - 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II devices are configured by loading data into internal configuration memory, using the following five modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Integrated Logic Analyzer (ILA) core and software provides a complete solution for accessing and verifying Virtex-II devices.

Power-Down Mode

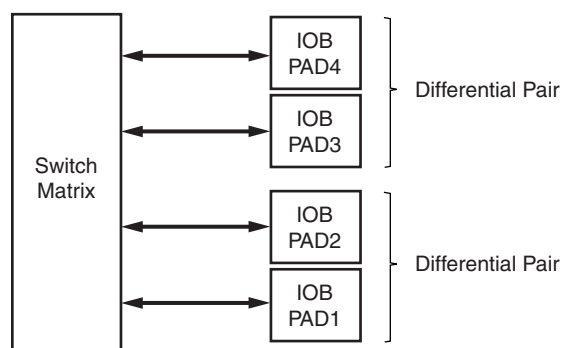
Activated by the power-down input, this mode reduces supply current and retains the Virtex-II device configuration.

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in **Figure 2**.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.



DS031_30_101600

Figure 2: Virtex-II Input/Output Tile

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage ($V_{CCINT} = 1.5V$), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see [Table 4](#)). An auxiliary supply voltage ($V_{CCAUX} = 3.3V$) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see ["DC Input and Output Levels"](#) on page 78.

Table 4: Supported Single-Ended I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVC MOS33	3.3	3.3	N/A	N/A
LVC MOS25	2.5	2.5	N/A	N/A
LVC MOS18	1.8	1.8	N/A	N/A
LVC MOS15	1.5	1.5	N/A	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
PCI-X	3.3	3.3	N/A	N/A
GTL	N/A	N/A	0.8	1.2
GTL P	N/A	N/A	1.0	1.5
HSTL_I	1.5	N/A	0.75	0.75
HSTL_II	1.5	N/A	0.75	0.75
HSTL_III	1.5	N/A	0.9	1.5
HSTL_IV	1.5	N/A	0.9	1.5
SSTL2_I	2.5	N/A	1.25	1.25
SSTL2_II	2.5	N/A	1.25	1.25
SSTL3_I	3.3	N/A	1.5	1.5
SSTL3_II	3.3	N/A	1.5	1.5
AGP-2X/AGP	3.3	N/A	1.32	N/A

Table 5: Supported Differential Signal I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/A	N/A	$V_{CCO} - 1.025$ to $V_{CCO} - 1.64$
LDT_25	2.5	N/A	N/A	0.430 - 0.670
LVDS_33	3.3	N/A	N/A	0.250 - 0.400
LVDS_25	2.5	N/A	N/A	0.250 - 0.400
LVDS EXT_33	3.3	N/A	N/A	0.330 - 0.700
LVDS EXT_25	2.5	N/A	N/A	0.330 - 0.700
BLVDS_25	2.5	N/A	N/A	0.250 - 0.450
ULVDS_25	2.5	N/A	N/A	0.430 - 0.670

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. The IOBs are not compatible or compliant with 5 V I/O standards (not 5 V tolerant).

[Table 6](#) lists supported I/O standards with Digital Controlled Impedance. See ["Digital Controlled Impedance \(DCI\)"](#) on page 43.

Table 6: Supported DCI I/O Standards

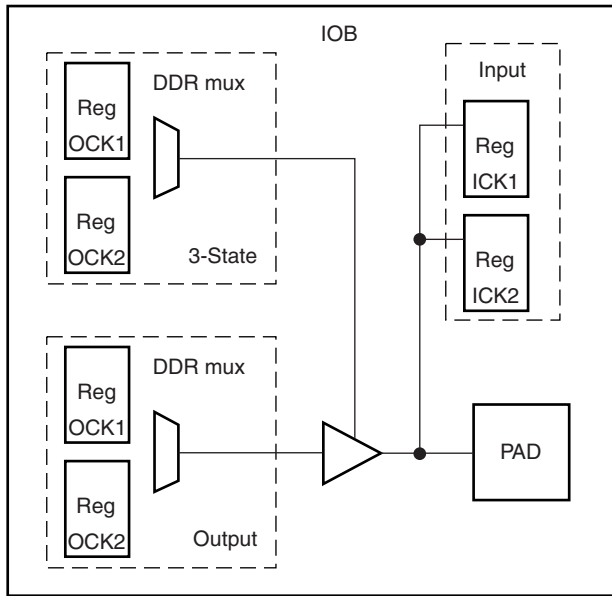
I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33	3.3	3.3	N/A	Series
LVDCI_DV2_33	3.3	3.3	N/A	Series
LVDCI_25	2.5	2.5	N/A	Series
LVDCI_DV2_25	2.5	2.5	N/A	Series
LVDCI_18	1.8	1.8	N/A	Series
LVDCI_DV2_18	1.8	1.8	N/A	Series
LVDCI_15	1.5	1.5	N/A	Series
LVDCI_DV2_15	1.5	1.5	N/A	Series
GTL_DC I	1.2	1.2	0.8	Single
GTL P_DC I	1.5	1.5	1.0	Single
HSTL_I_DC I	1.5	1.5	0.75	Split
HSTL_II_DC I	1.5	1.5	0.75	Split
HSTL_III_DC I	1.5	1.5	0.9	Single
HSTL_IV_DC I	1.5	1.5	0.9	Single
SSTL2_I_DC I ²	2.5	2.5	1.25	Split
SSTL2_II_DC I ²	2.5	2.5	1.25	Split
SSTL3_I_DC I ²	3.3	3.3	1.5	Split
SSTL3_II_DC I ²	3.3	3.3	1.5	Split

Notes:

1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 3.

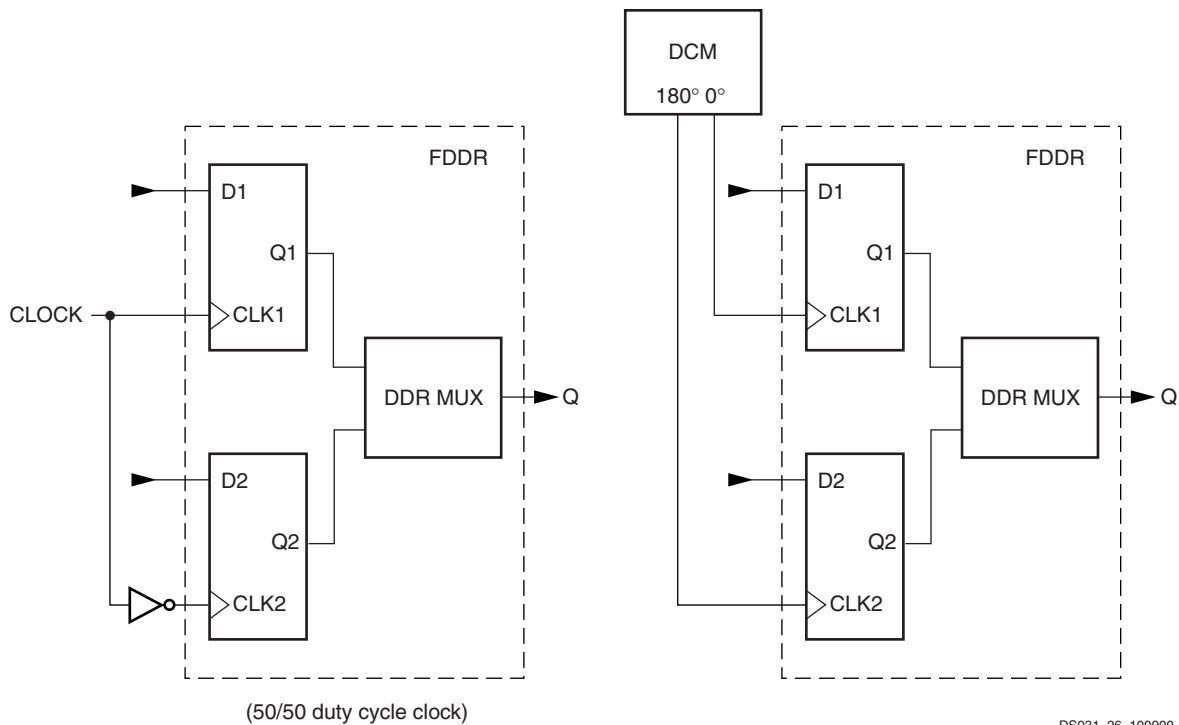


DS031_29_100900

Figure 3: Virtex-II IOB Block

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 4. There are two input, output, and 3-state data signals, each being alternately clocked out.



DS031_26_100900

Figure 4: Double Data Rate Registers

This DDR mechanism can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLow attribute. SRHIGH forces a logic "1". SRLow forces a logic "0". When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default,

the SRLow attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLow, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 5) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

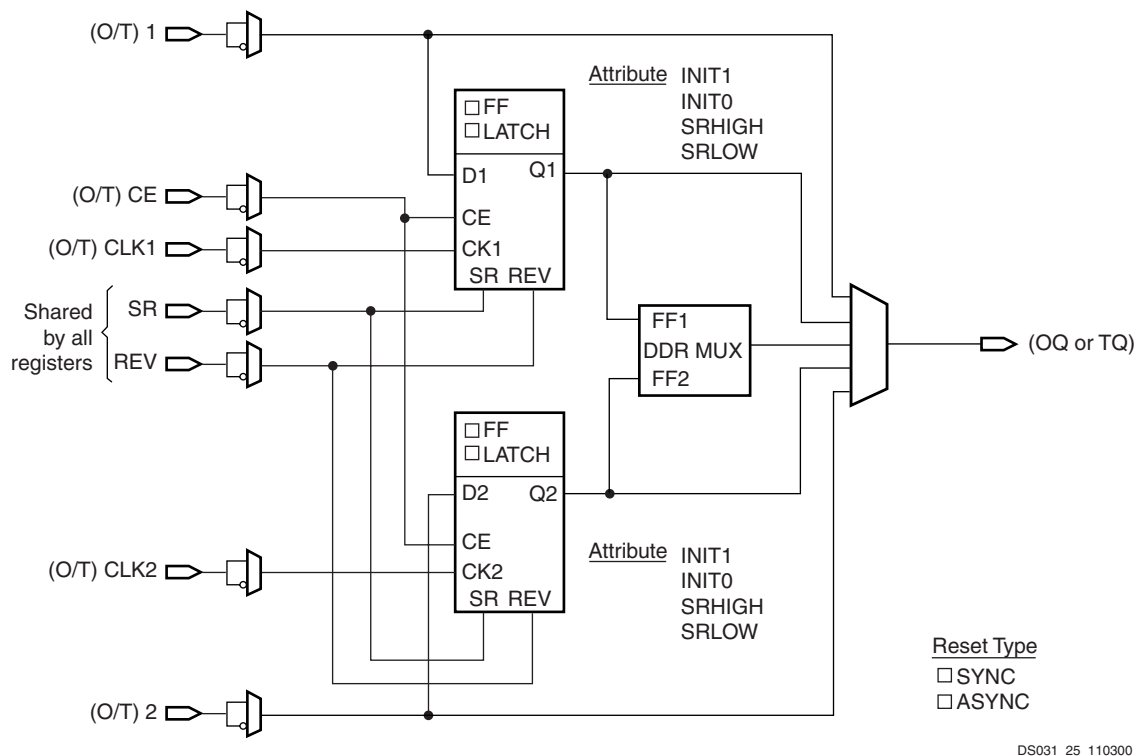


Figure 5: Register / Latch Configuration in an IOB Block

Input/Output Individual Options

Each device pad has optional pull-up, pull-down, and weak-keeper in LVTTL and LVC MOS Select/I/O configurations, as illustrated in Figure 6. Values of the optional pull-up and pull-down resistors are in the range 50 - 100 KΩ.

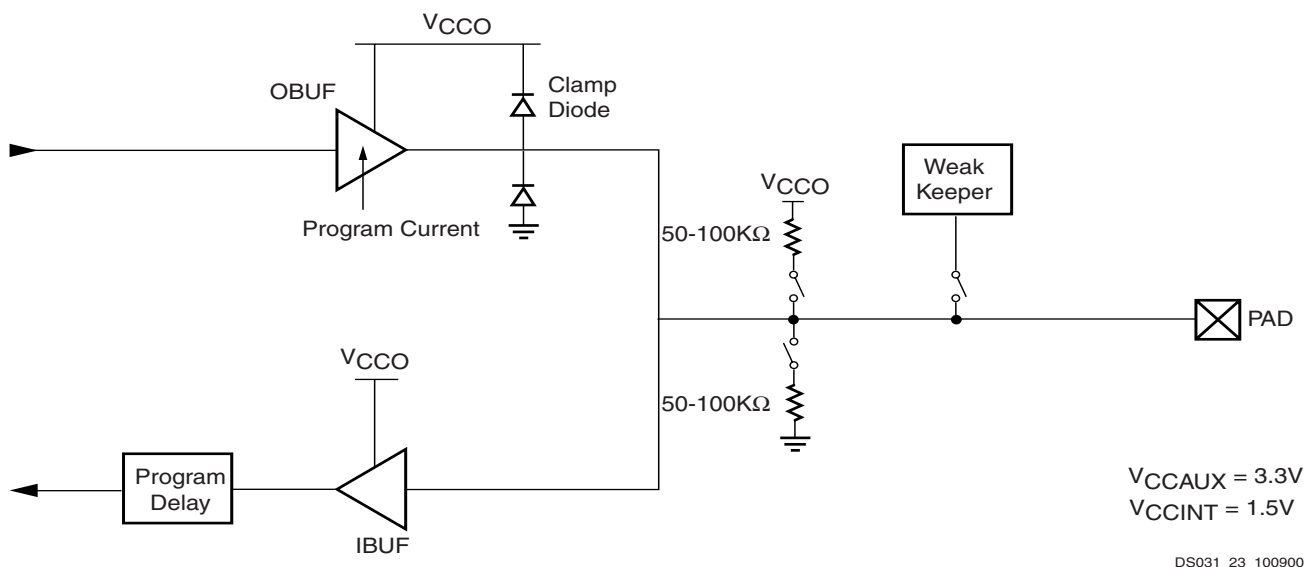


Figure 6: LVTTL, LVC MOS or PCI Select/I/O Standards

The optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter; pull-up or pull-down override the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVC MOS Select/I/O standards (see Table 7). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Table 7: LVTTL and LVC MOS Programmable Currents (Sink and Source)

Select/I/O	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVC MOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 7 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

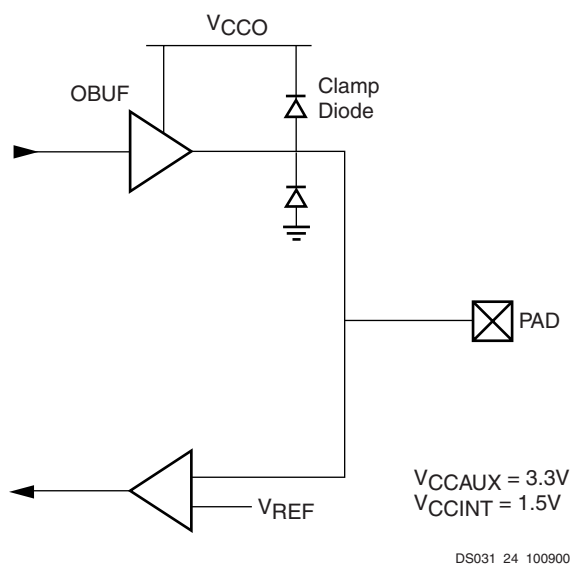


Figure 7: SSTL or HSTL Select I/O Standards

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible boundary scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} . The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

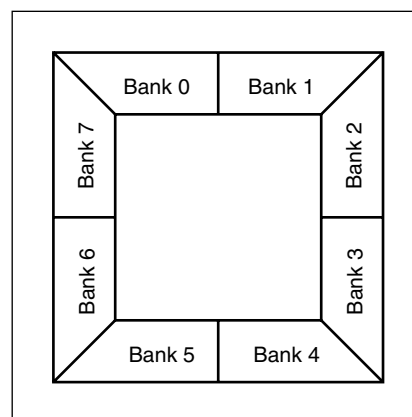
The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 8 and Figure 9. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

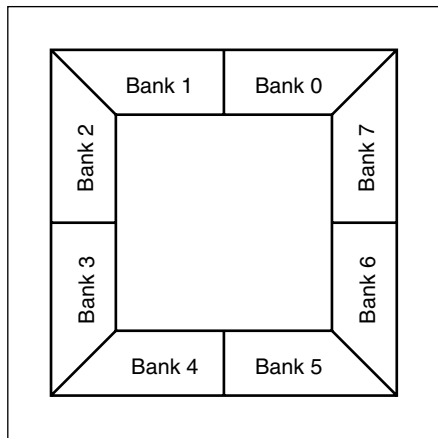


ug002_c2_014_112900

Figure 8: Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS, FG, & BG)

Within a bank, output standards can be mixed only if they use the same V_{CCO} . Compatible standards are shown in Table 8. GTL and GTLP appear under all voltages because their open-drain outputs do not depend on V_{CCO} .

Some input standards require a user-supplied threshold voltage, V_{REF} . In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.



ds031_66_112900

Figure 9: Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)

V_{REF} pins within a bank are interconnected internally, and consequently only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

Table 8: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTTL, SSTL3 (I & II), AGP-2X, LVDS_33, LVDSEXT_33, LVC MOS33, LVDCI_33, LVDCI_DV2_33, SSTL3_DCI (I & II), BLVDS, LVPECL, GTL, GTLP
2.5 V	SSTL2 (I & II), LVC MOS25, GTL, GTLP, LVDS_25, LVDSEXT_25, LVDCI_25, LVDCI_DV2_25, SSTL2_DCI (I & II), LDT, ULVDS, BLVDS
1.8 V	LVC MOS18, GTL, GTLP, LVDCI_18, LVDCI_DV2_18
1.5 V	HSTL (I, II, III, & IV), LVC MOS15, GTL, GTLP, LVDCI_15, LVDCI_DV2_15, GTLP_DCI, HSTL_DCI (I, II, III & IV)
1.2V	GTL_DCI

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to the V_{CCO} voltage to permit migration to a larger device.

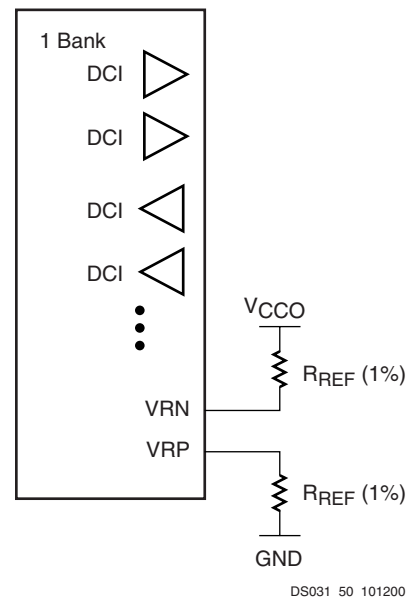
Digital Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II DCI provides controlled impedance drivers and on-chip termination for single-ended I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 10.



DS031_50_101200

Figure 10: DCI in a Virtex-II Bank

When used with a terminated I/O standard, the value of the resistor is specified by the standard (typically 50 Ω). When used with a controlled impedance driver, the resistor sets the output impedance of the driver within the specified range (25 Ω to 150 Ω). The resistors connected to VRN and VRP do not need to be the same value. 1% resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistor, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

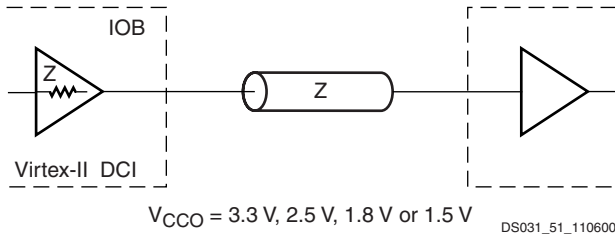


Figure 11: Internal Series Termination

Table 9: SelectI/O Controlled Impedance Buffers

V _{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel Termination)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 10 lists the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 6. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 10: SelectI/O Buffers With On-Chip Parallel Termination

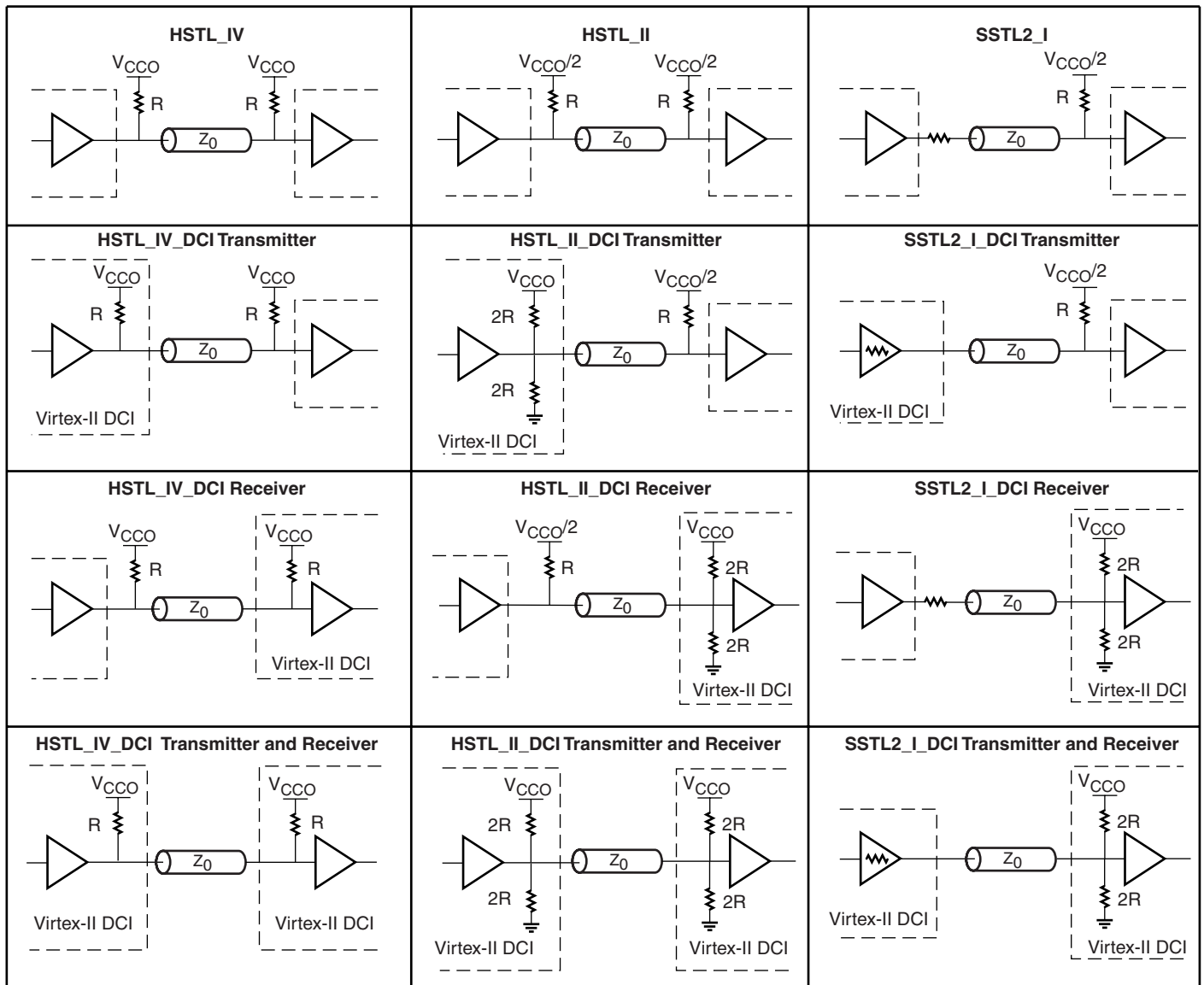
I/O Standard	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI ¹
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI ¹
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI ¹
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI ¹
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:

1. SSTL Compatible

For further details, see the *Virtex-II User Manual*.

Figure 12 provides examples illustrating the use of the HSTL_IV_DCI, HSTL_II_DCI, and SSTL2_DCI I/O standards.



ds031_65_110200

Figure 12: DCI Usage Examples

Configurable Logic Blocks (CLBs)

The Virtex-II configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 13. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

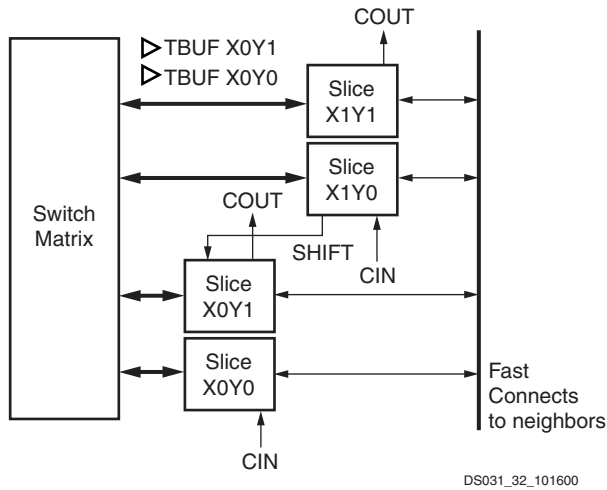


Figure 13: Virtex-II CLB Element

DS031_32_101600

Slice Description

Introduction

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 14, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

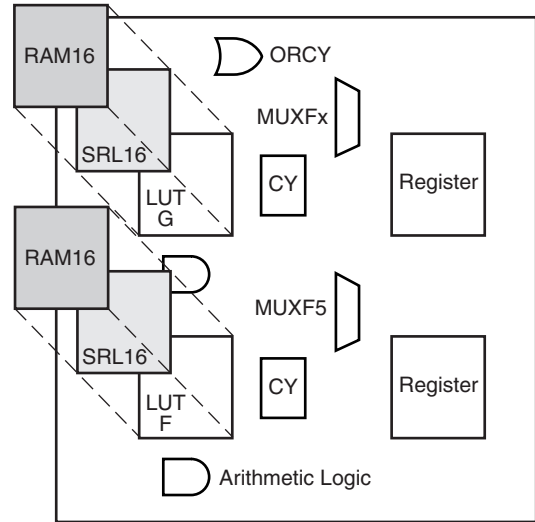


Figure 14: Virtex-II Slice Configuration

DS031_31_100900

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 15 shows a more detailed view of a single slice.

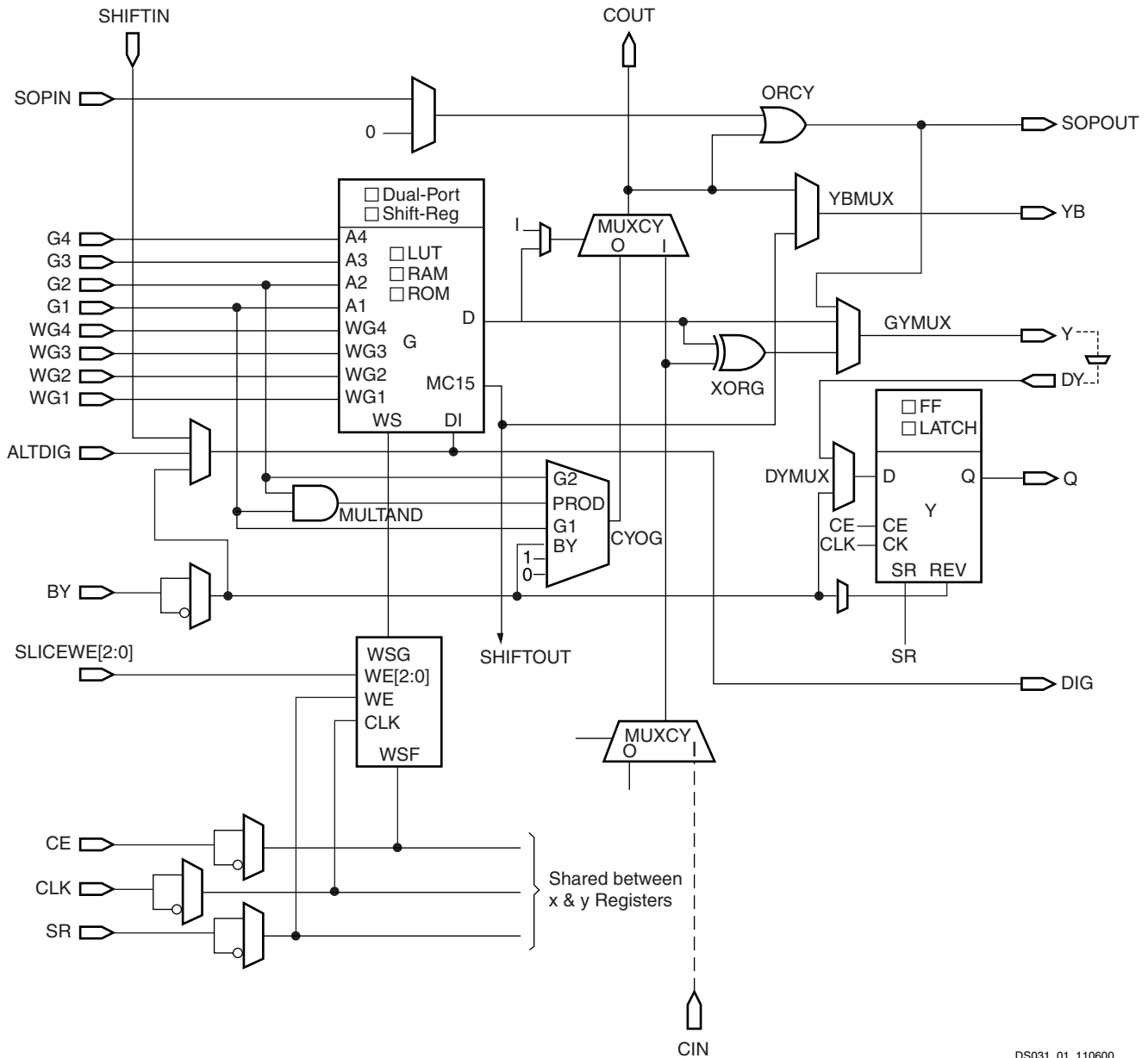


Figure 15: Virtex-II Slice (Top Half)

Configurations

Look-Up Table

Virtex-II function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D

input of the storage element, or go to the MUXF5 (not shown in Figure 15).

In addition to the basic LUTs, the Virtex-II slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX are either MUXF6, MUXF7 or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexers to map any functions of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic “1” when SR is asserted. SRLOW forces a logic “0”. When SR is used, a second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition. (See Figure 16.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 11 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 11: Distributed SelectRAM Configurations

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:

1. S = single-port configuration; D = dual-port configuration

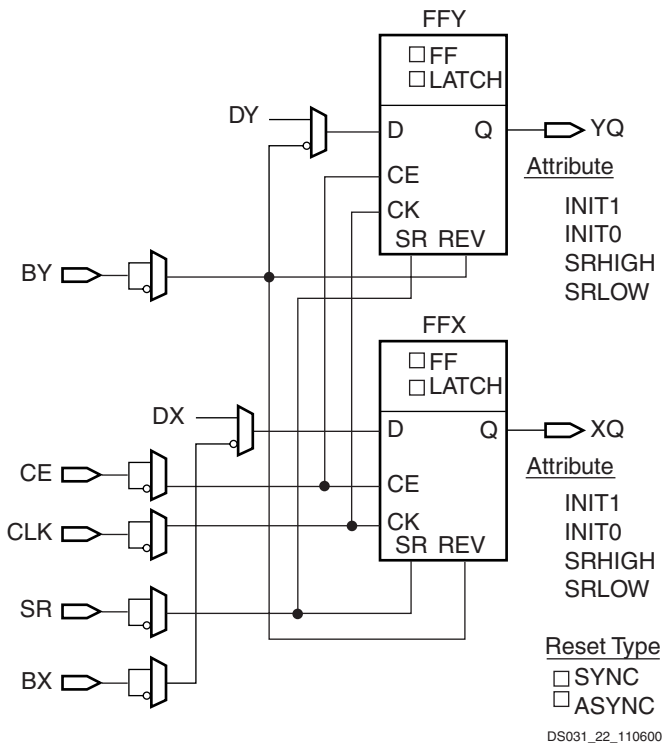


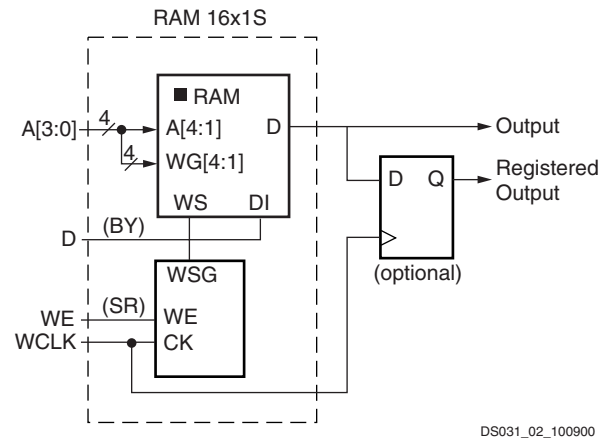
Figure 16: Register / Latch Configuration in a Slice

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

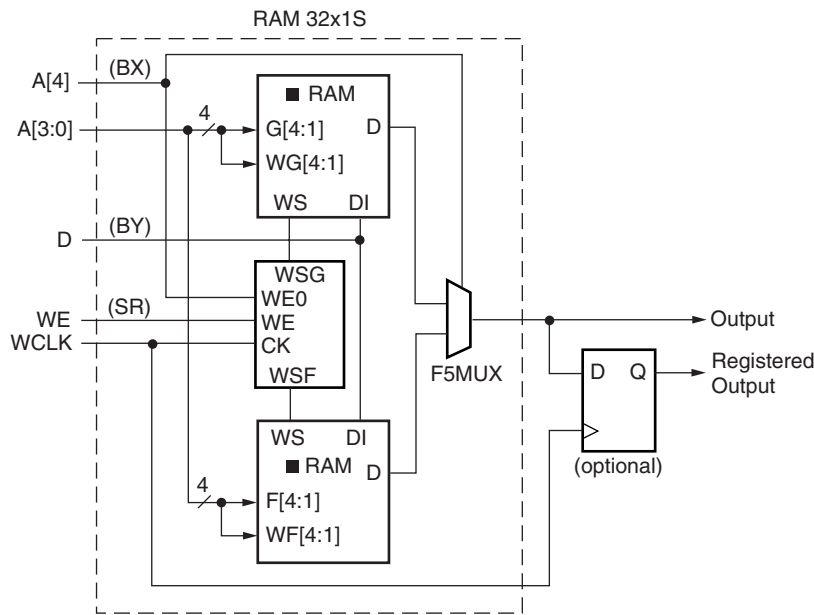
In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Figure 17, Figure 18, and Figure 19 illustrate various example configurations.



DS031_02_100900

Figure 17: Distributed SelectRAM (RAM16x1S)



DS031_03_110100

Figure 18: Single-Port Distributed SelectRAM (RAM32x1S)

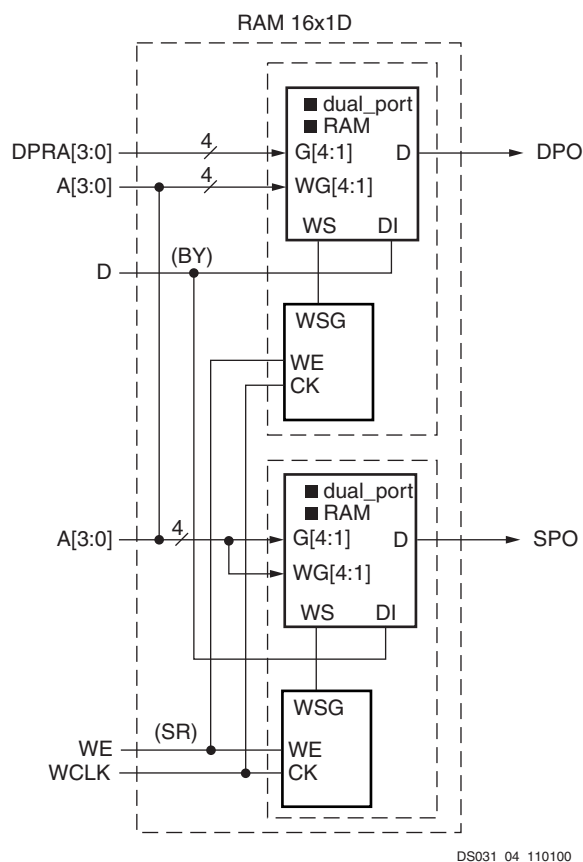


Figure 19: Dual-Port Distributed SelectRAM (RAM16x1D)

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 12 shows the number of LUTs occupied by each configuration.

Table 12: ROM Configuration

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 20. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

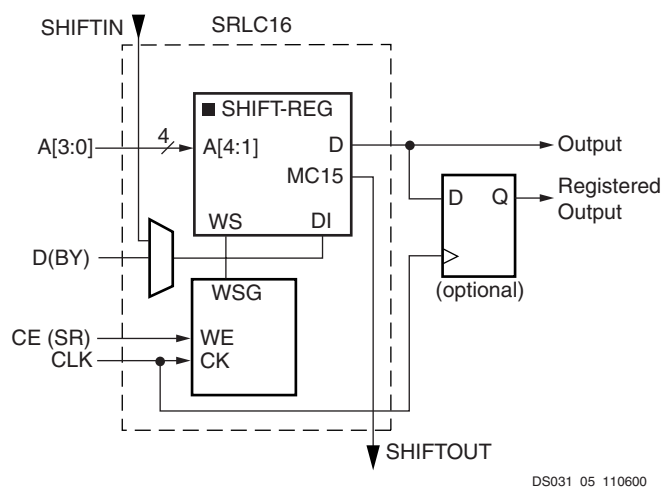


Figure 20: Shift Register Configurations

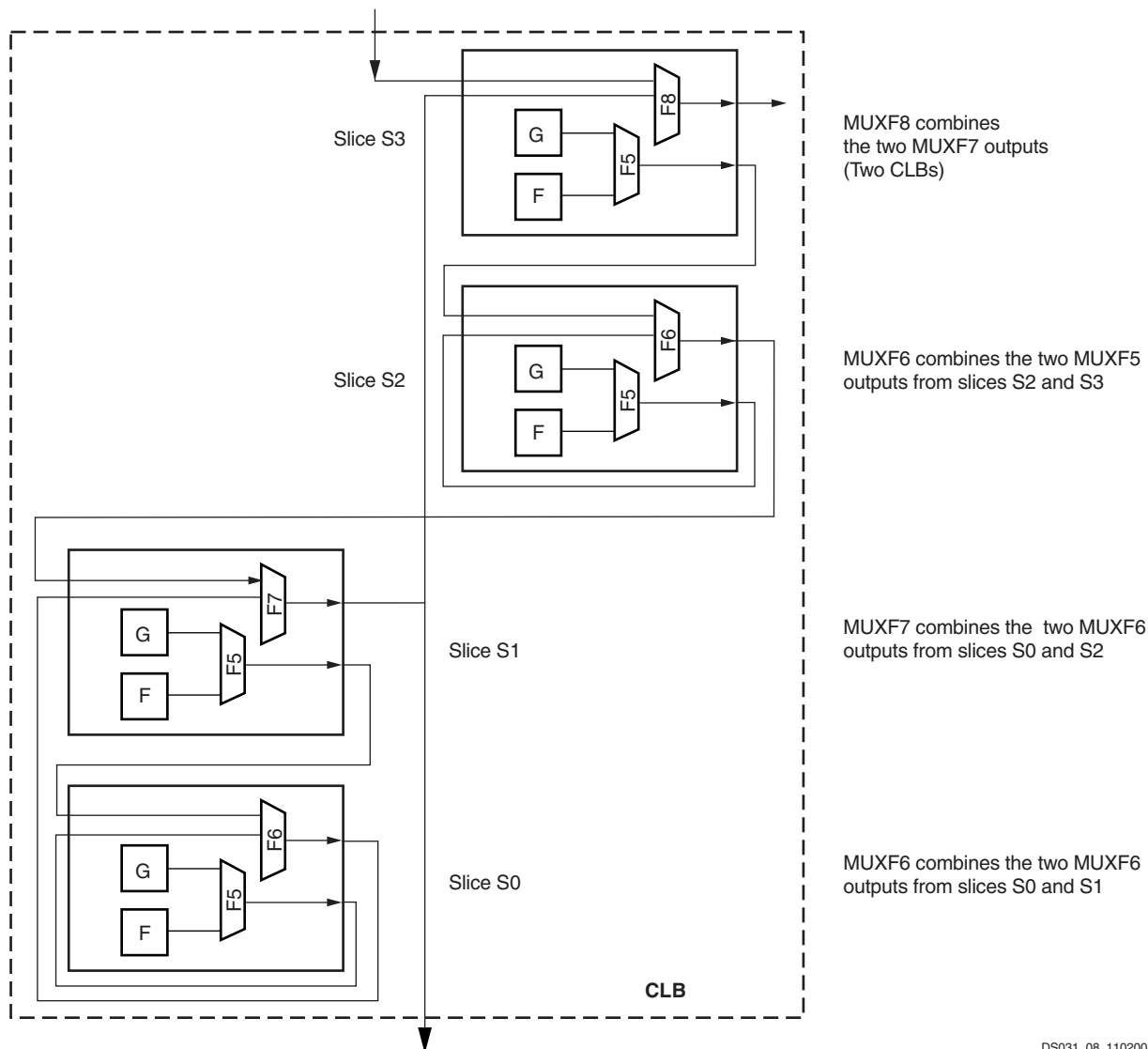
An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 21.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in **Figure 22**. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II User Manual*. Any LUT can implement a 2:1 multiplexer.



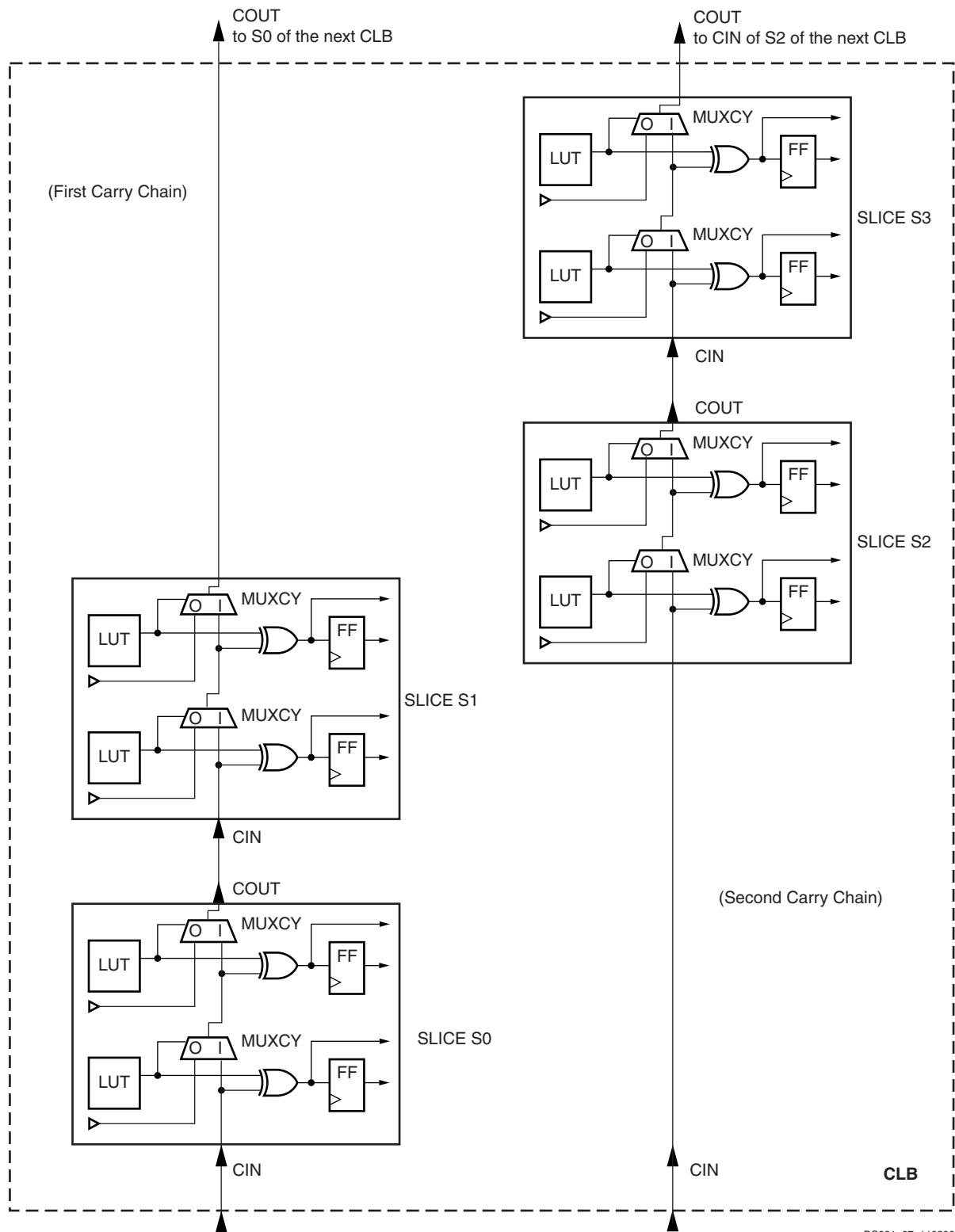
DS031_08_110200

Figure 22: MUXF5 and MUXFX multiplexers

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the **Figure 23**.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.



DS031_07_110200

Figure 23: Fast Carry Logic Path

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 15) improves the efficiency of multiplier implementation.

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 24.

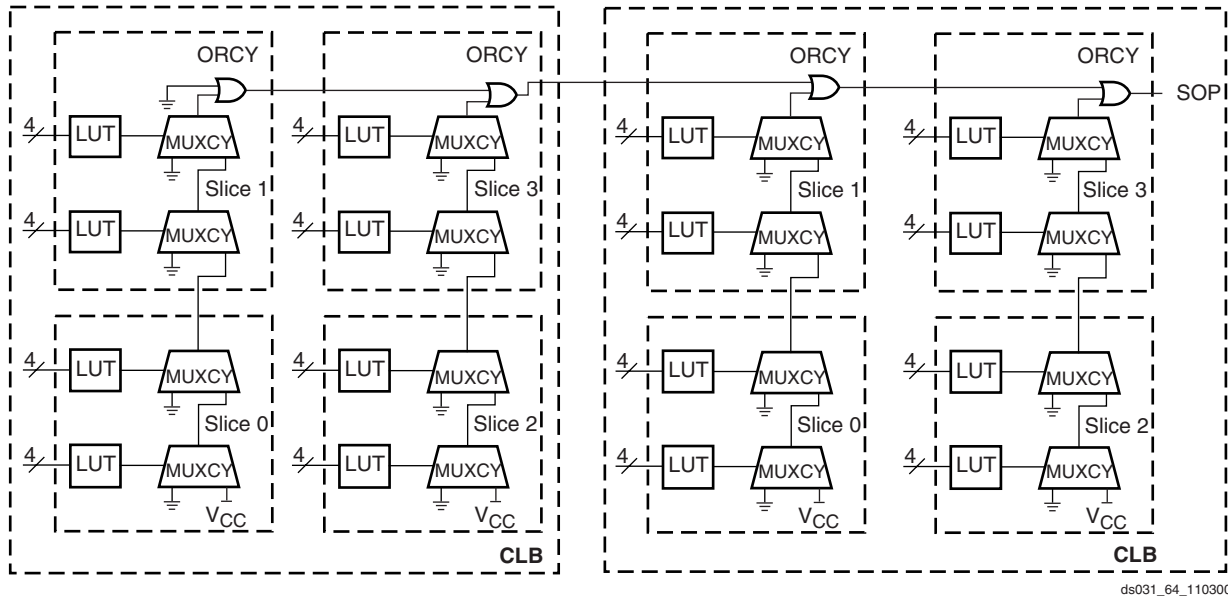


Figure 24: Horizontal Cascade Chain

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 25 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

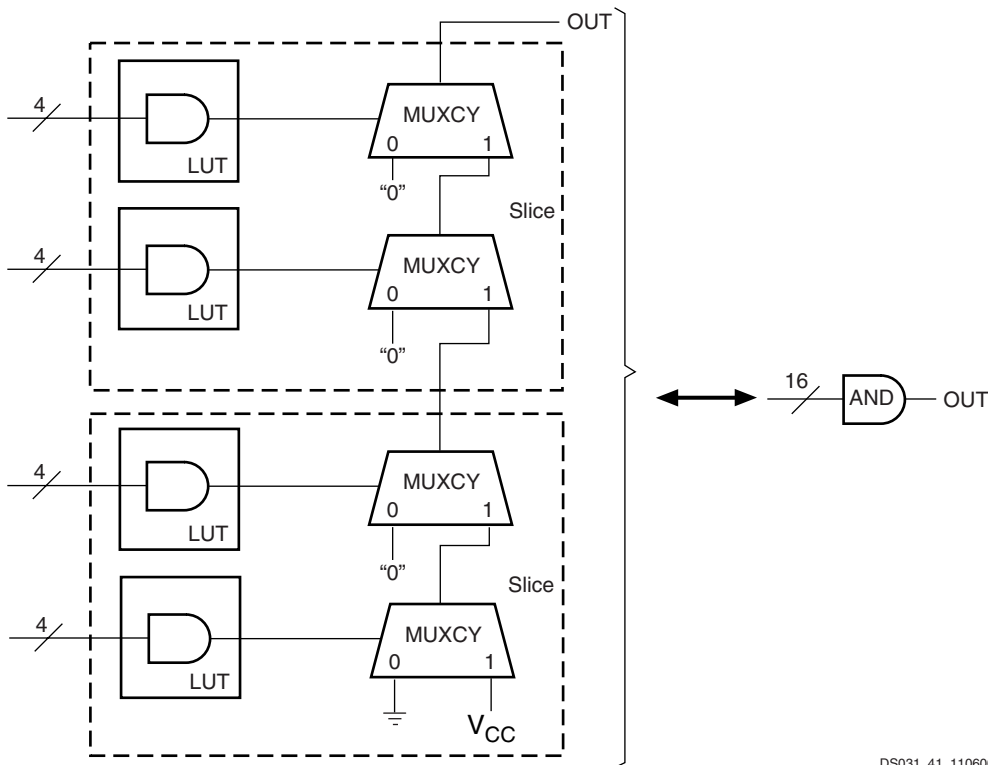


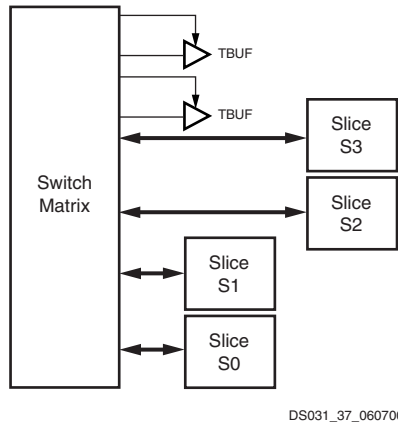
Figure 25: Wide-Input AND Gate (12 Inputs)

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip busses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 26. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state busses.



DS031_37_060700

Figure 26: Virtex-II 3-State Buffers

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

Locations / Organization

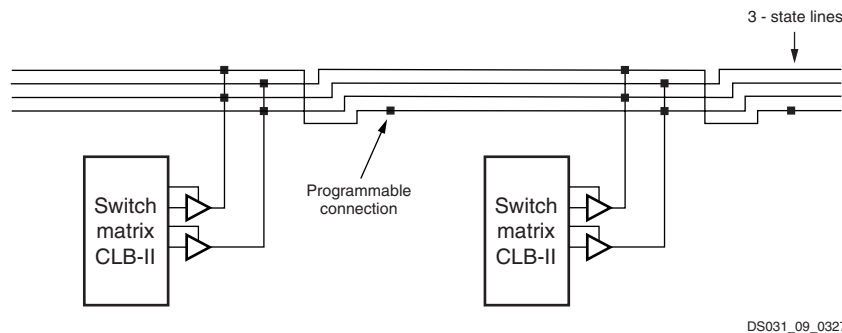
Four horizontal routing resources per CLB are provided for on-chip 3-state busses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 27. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 13 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 13: Virtex-II 3-State Buffers

Device	3-State Buffers per Row	Total Number of 3-State Buffers
XC2V40	16	128
XC2V80	16	256
XC2V250	32	768
XC2V500	48	1,536
XC2V1000	64	2,560
XC2V1500	80	3,840
XC2V2000	96	5,376
XC2V3000	112	7,168
XC2V4000	144	11,520
XC2V6000	176	16,896
XC2V8000	208	23,296
XC2V10000	240	30,720



DS031_09_032700

Figure 27: 3-State Buffer Connection to Horizontal Lines

CLB/Slice Configurations

Table 14 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. **Table 15** shows the available resources in all CLBs.

Table 14: Logic Resources in One CLB

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 15: Virtex-II Logic Resources Available in All CLBs

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains ¹	Number of SOP Chains ¹
XC2V40	8 x 8	256	516	8,192	516	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224
XC2V10000	128 x 120	61,440	122,880	1,966,080	122,880	240	256

Notes:

1. The carry-chains and SOP chains can be split or cascaded.

18-Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18-Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18-Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 16.

Table 16: Dual- and Single-Port Configurations

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18-Kbit memory locations in any of the 2K x 9-bit,

Table 17: Dual-Port Mode Configurations

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

1K x 18-bit, or 512 x 36-bit configurations and to 16-Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 28. Input data bus and output data bus widths are identical.

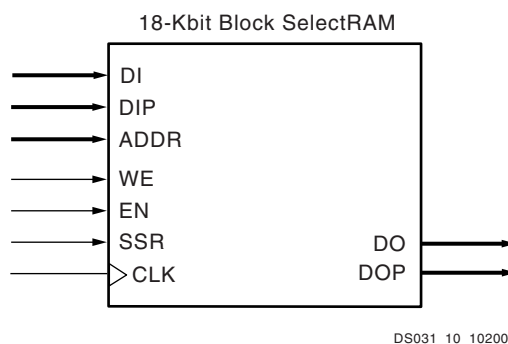


Figure 28: 18-Kbit Block SelectRAM Memory in Single-Port Mode

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18-Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 17 illustrates the different configurations available on ports A & B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18-Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18-Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 29. The two ports have independent inputs and outputs and are independently clocked.

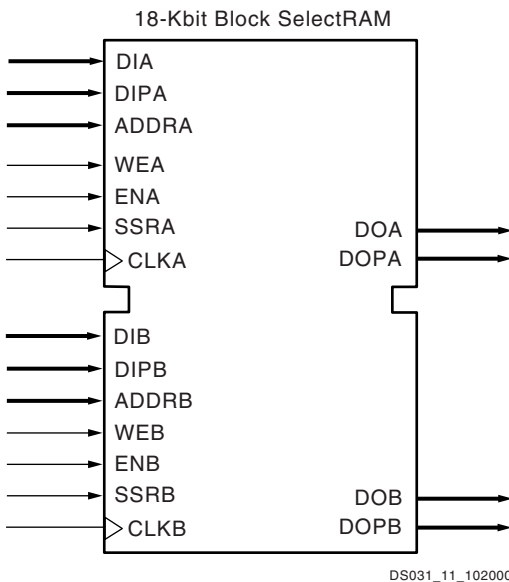


Figure 29: 18-Kbit Block SelectRAM in Dual-Port Mode

Port Aspect Ratios

Table 18 shows the depth and the width aspect ratios for the 18-Kbit block SelectRAM. Virtex-II block SelectRAM also

includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 18: 18-Kbit Block SelectRAM Port Aspect Ratio

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. There are three different options available, each set by configuration:

1. "WRITE_FIRST"

The "WRITE_FIRST" option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 30.

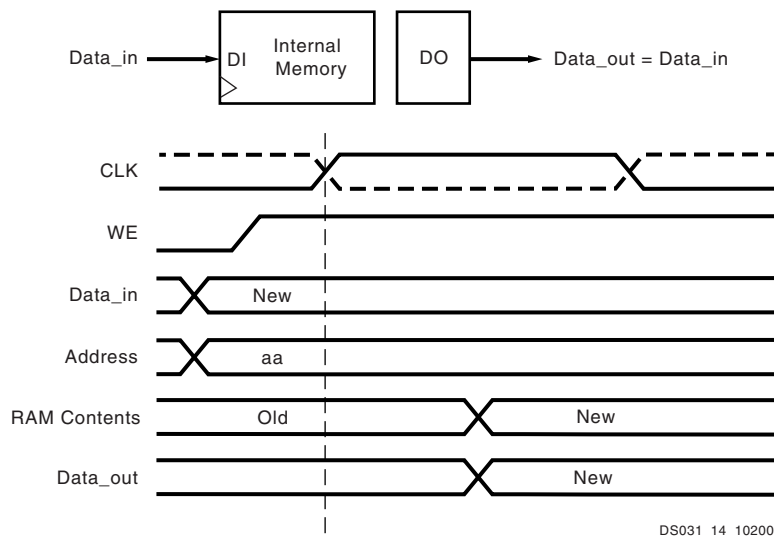


Figure 30: WRITE_FIRST Mode

2. "READ_FIRST"

The "READ_FIRST" option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 31.

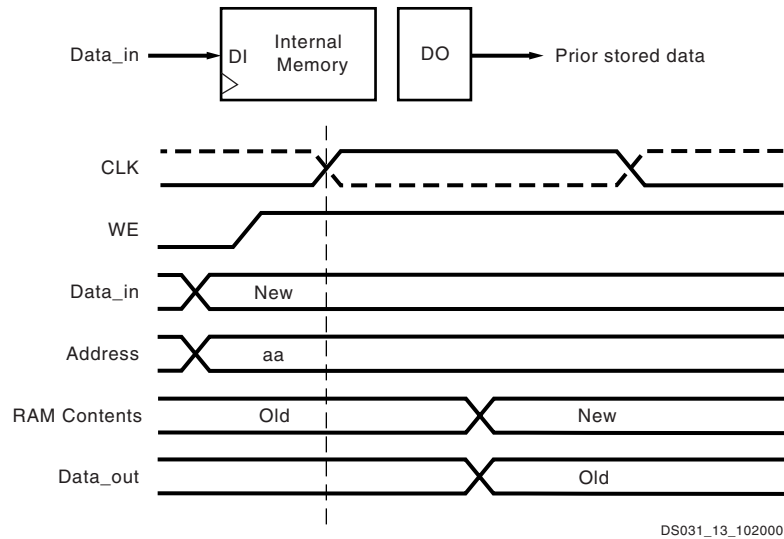


Figure 31: READ_FIRST Mode

3. "NO_CHANGE"

The "NO_CHANGE" option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as "NO_CHANGE", only a read operation loads a new value in the output register DO, as shown in Figure 32.

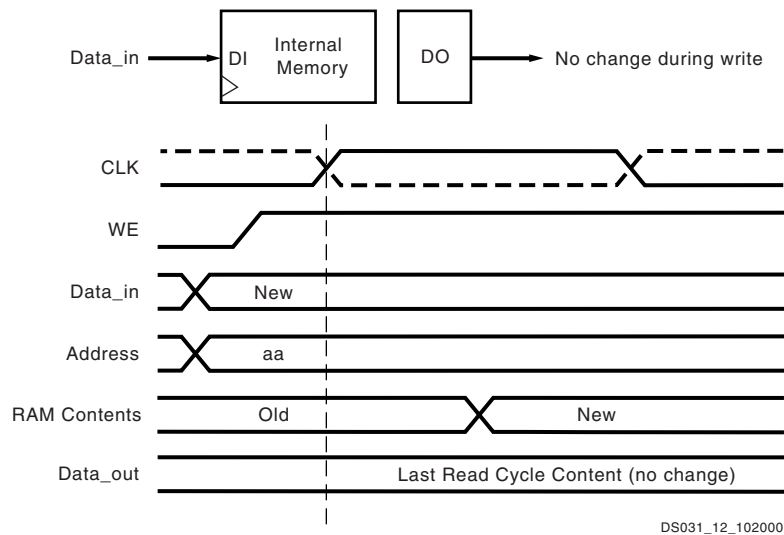


Figure 32: NO_CHANGE Mode

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 19. All control inputs including the clock have an optional inversion.

Table 19: Control Functions

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_{xx} attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are organized in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the

number of CLBs in a column divided by four. Column locations are shown in Table 20.

Table 20: SelectRAM Memory Floor Plan

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168
XC2V10000	6	32	192

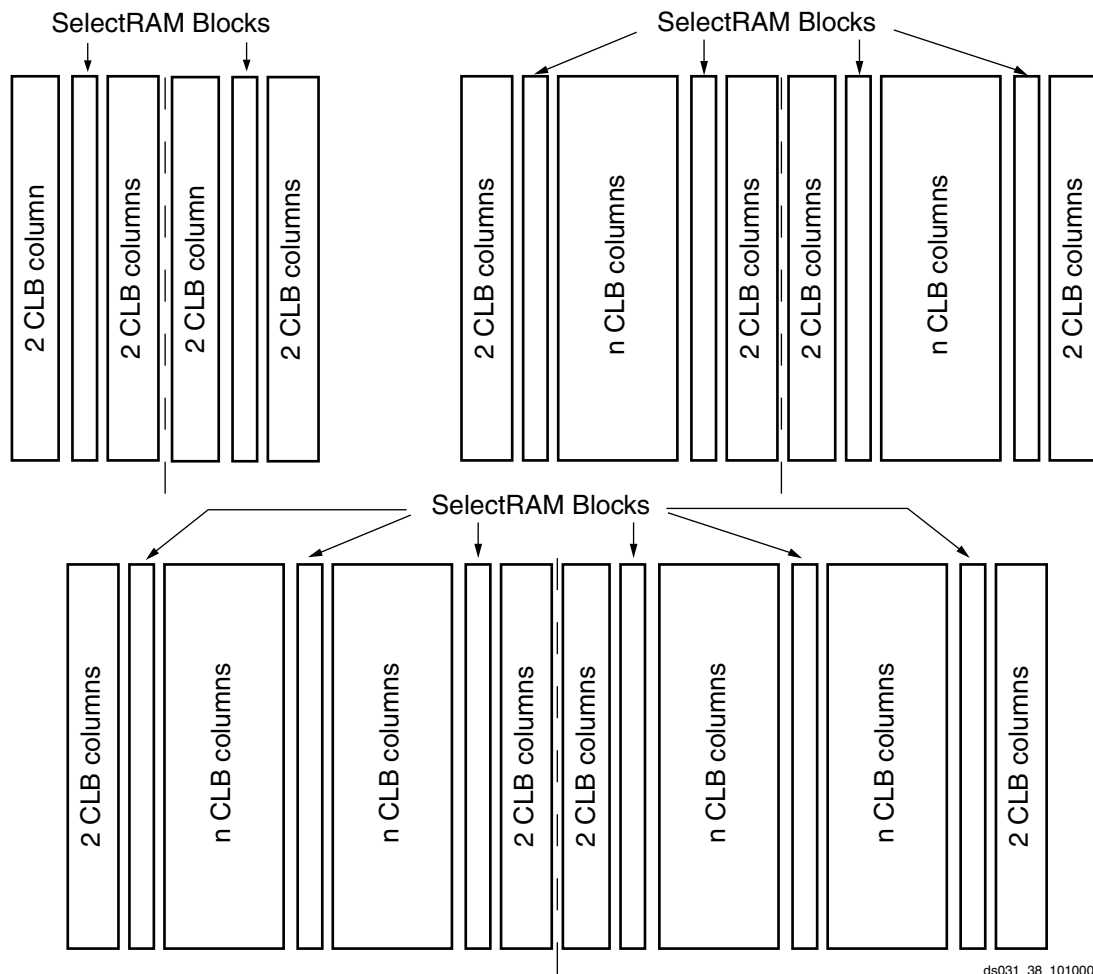


Figure 33: Block SelectRAM (2-column, 4-column, and 6-column)

Total Amount of SelectRAM Memory

Table 21 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18-Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 21: Virtex-II SelectRAM Memory Available

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
XC2V40	4	72	73,728
XC2V80	8	144	147,456
XC2V250	24	432	442,368
XC2V500	32	576	589,824
XC2V1000	40	720	737,280
XC2V1500	48	864	884,736
XC2V2000	56	1,008	1,032,192
XC2V3000	96	1,728	1,769,472
XC2V4000	120	2,160	2,211,840
XC2V6000	144	2,592	2,654,208
XC2V8000	168	3,024	3,096,576
XC2V10000	192	3,456	3,538,944

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18-Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 34.

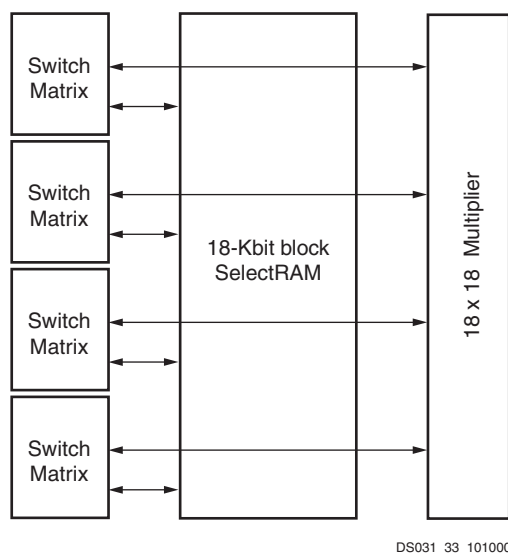


Figure 34: SelectRAM and Multiplier Blocks

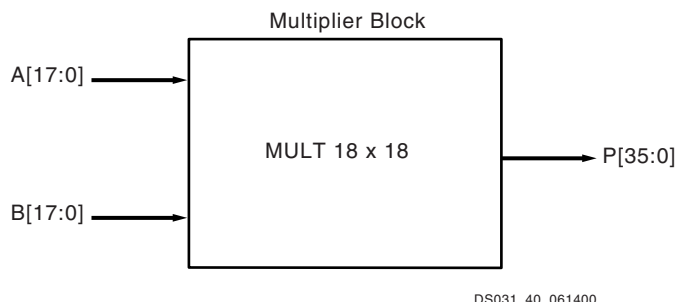
Association With Block SelectRAM Memory

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 35 shows a multiplier block.



DS031_40_061400

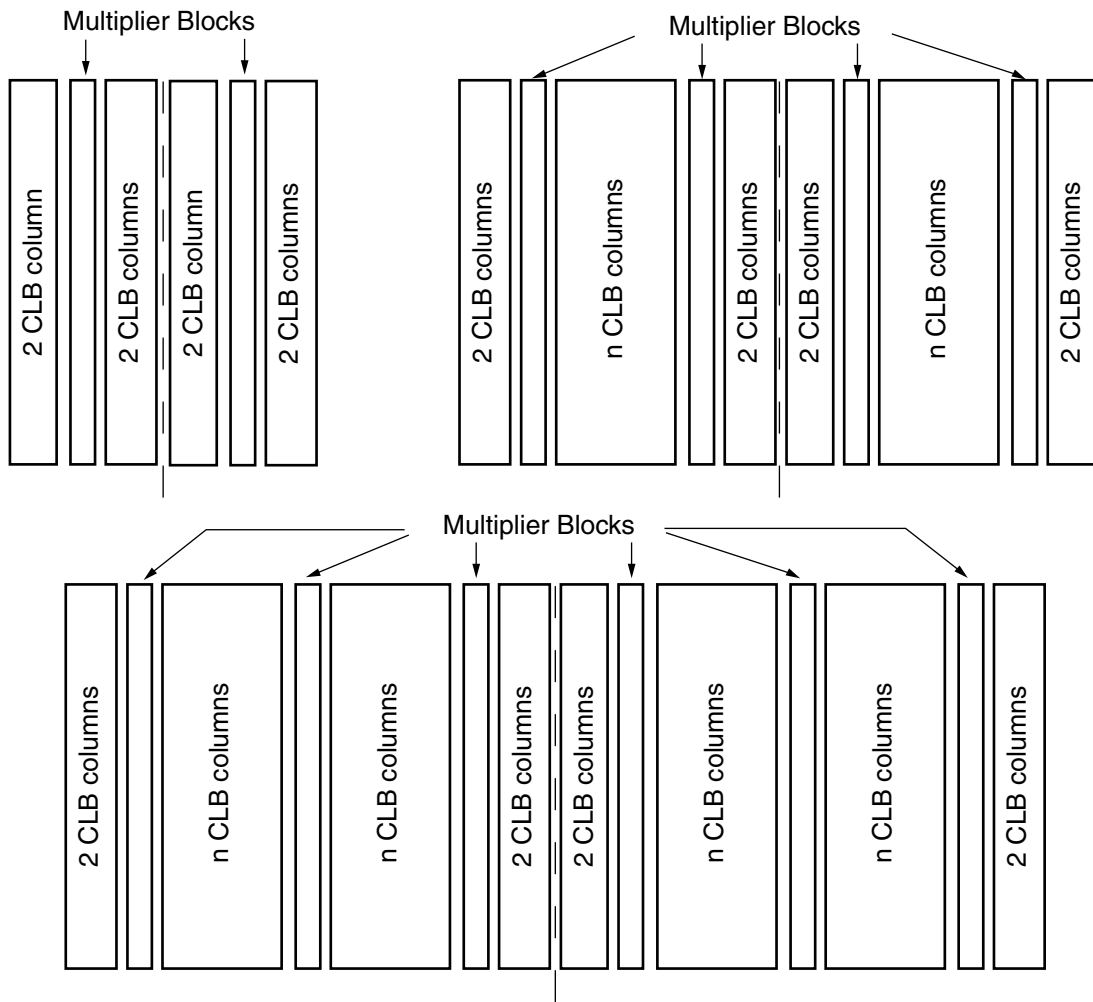
Figure 35: Multiplier Block

Locations / Organization

Multiplier organization is identical to the 18-Kbit SelectRAM organization, because each multiplier is associated with an 18-Kbit block SelectRAM resource.

Table 22: Multiplier Floor Plan

Device	Columns	Multipliers	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168
XC2V10000	6	32	192



DS031_39_101000

Figure 36: Multipliers (4 column vs. 6 column)

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to "Configurable Logic Blocks (CLBs)" on page 46).

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 37.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

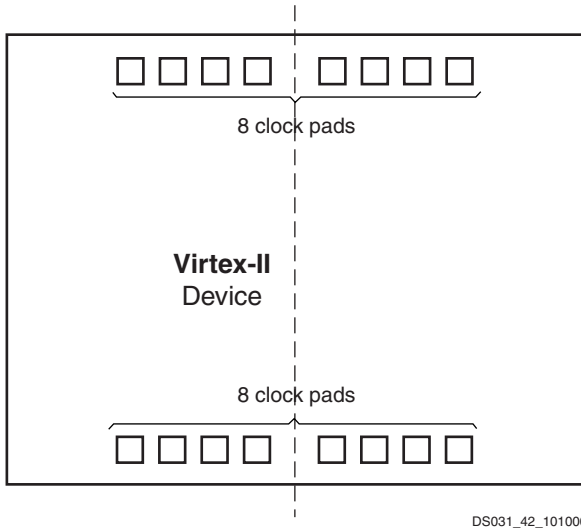


Figure 37: Virtex-II Clock Pads

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in "Digital

Clock Manager (DCM)" on page 66. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 38.

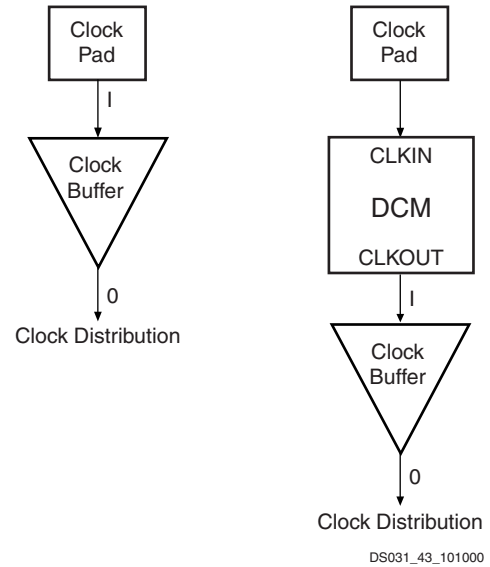


Figure 38: Virtex-II Clock Distribution Configurations

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks).

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distribution detail of the device prior to pin-locking and floorplanning (see the *Virtex-II User Manual*).

Figure 39 shows clock distribution in Virtex-II devices.

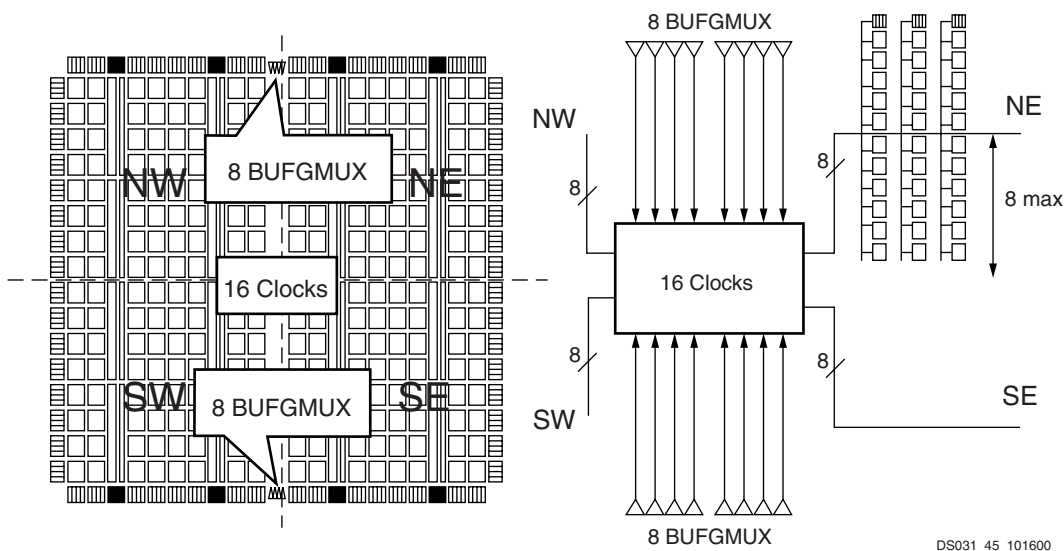


Figure 39: Virtex-II Clock Distribution

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

The global clock multiplexer buffers have two clock inputs, a select input, and a clock output. The select input selects between I_0 and I_1 without generating glitches.

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in [Figure 40](#).

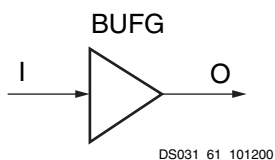


Figure 40: Virtex-II BUFG Function

In [Figure 41](#) the global buffer can also perform a clock enable function (clock gating). The CE input is synchronized inside the BUFG so any change in CE is only effective when the clock input is Low. This eliminates any glitches or runt pulses on the output, even when CE changes asynchronously to the clock.

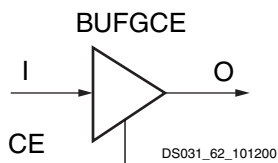


Figure 41: Virtex-II BUFGCE Function

The two clock inputs can be connected to any synchronous or asynchronous clock (from a clock pad or DCM clock output). When the select input (S) is Low, the clock connected to the I_0 input is distributed, as shown in [Figure 42](#). Setting S High, causes the clock connected to the I_1 input to be distributed.

The clock multiplexer can also switch between two unrelated clocks. The S input can be changed asynchronously to both clocks. Internal synchronization switches away for

the present clock when it is low but switches to the new clock only after the subsequent falling edge.

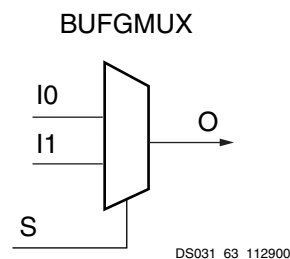


Figure 42: Virtex-II BUFGMUX Function

When S changes state, the transition on the output occurs without creating a runt pulse. The output pulse is never shorter than the I_0 or I_1 input pulse. The S input has a setup requirement.

The global clock multiplexer buffers has two options:

- Transition on Low clock states
- Transition on High clock states

The transition on Low follows different steps, as illustrated in [Figure 43](#).

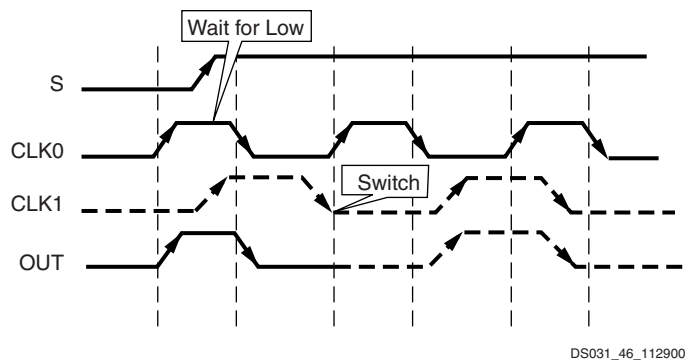


Figure 43: Clock Multiplexer Waveform Diagram

- The current clock is CLK0.
- S is activated High (setup is required before the next negative CLK0 edge).
- If CLK0 is currently High, the multiplexer waits for the next negative edge.
- Once CLK0 is Low, the multiplexer output stays Low, until CLK1 goes Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

The transition on High clock state is similar, with the positive edge of the second clock Low.

All Virtex-II devices have 16 global clock multiplexer buffers.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew:** The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock.
- **Frequency Synthesis:** The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting:** The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.
- **EMI Reduction:** The DCM provides the capability to reduce electromagnetic interference (EMI) by broadening the output clock frequency spectrum.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four DCM clock outputs can drive global clock multiplexer buffer inputs simultaneously (see [Figure 44](#)). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

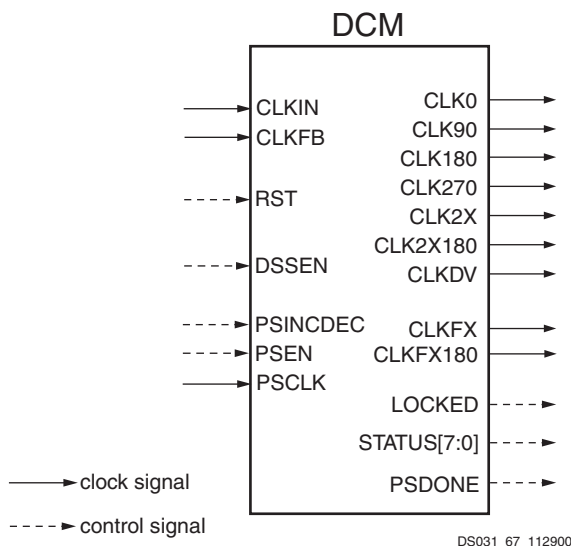


Figure 44: Digital Clock Manager

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in [Table 1](#).

Table 23: DCM Status Pins

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAM synchronous to clock edges arriving at the input. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs can be used to double the clock frequency. The CLKDV output can be used to create divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$\text{FREQ}_{\text{CLKFX}} = (M/D) * \text{FREQ}_{\text{CLKIN}}$$

where M and D are two integers, each between 1 and 4096. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high frequency mode).

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, allowing coarse phase adjustments.

Fine phase adjustment applies to all DCM output clocks when activated. The phase shift between the rising edges of CLKIN and CLKFB is configured to be a specified fraction of the input clock period, and it can be dynamically adjusted with the dedicated signals, PSINCDEC, PSEN, PSCLK, and PSDONE. The phase shift value (PS) is specified as an integer between -255 and +255. The amount of phase shift achieved is given by the equation:

$$\text{Phase shift} = (\text{PS}/256) * \text{PERIOD}_{\text{CLKIN}}$$

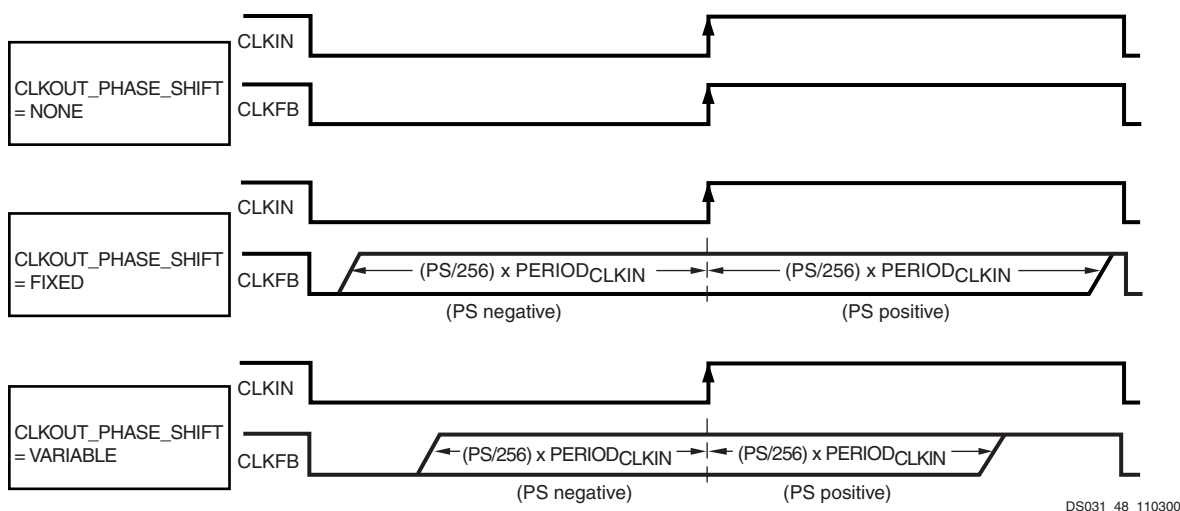


Figure 45: Fine Phase Shifting Effects

EMI Reduction

The DCM offers a Digital Spread Spectrum (DSS) feature that broadens the frequency spectrum of the clock outputs. The spectrum spreading applies directly to the CLK0, CLK90, CLK180, and CLK270 clock outputs when it is active. The other DCM clock outputs are affected to only a small degree. Spreading the spectrum of the clock frequency reduces the electromagnetic interference (EMI), or energy radiation, within the relevant frequency bandwidth window. This technique aids in meeting FCC EMI regulations.

When enabled, spectrum spreading begins immediately after the LOCKED signal goes HIGH. The DSSSEN input can be used to enable/disable the feature during operation.

Table 25 lists available DSS options.

In variable mode, the PS value can be dynamically incremented or decremented according to PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 45 illustrates the effects of fine phase shifting.

Table 24 lists fine phase shifting control pins, when used in variable mode.

Table 24: Fine Phase Shifting Control Pins

Control Pin	Direction	Function
PSINCDEC	in	Increment or decrement
PSEN	in	Enable ± phase shift
PSCLK	in	Clock for phase shift
PSDONE	out	Active when completed

Table 25: DSS Options

Number of Frequencies Added	Mode	Clock Period Range
2	SPREAD_2	± 1 x DCM_TAP
4	SPREAD_4	± 2 x DCM_TAP
6	SPREAD_6	± 3 x DCM_TAP
8	SPREAD_8	± 4 x DCM_TAP

Notes:

1. DCM_TAP value is defined in the AC characteristics section

Operating Modes

The frequency ranges of the DCM input and output clocks depend on the operating mode specified, either low frequency mode or high frequency mode, according to [Table 26](#) (for actual values, see "[Virtex-II Switching Characteristics](#)" on [page 81](#)). The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high frequency mode.

Table 26: DCM Frequency Ranges

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Locations/Organization

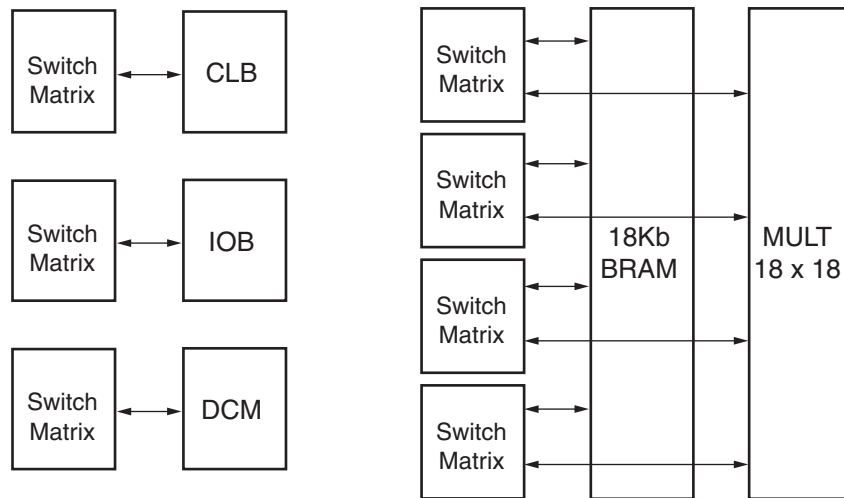
Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in [Table 27](#).

Table 27: DCM Organization

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12
XC2V10000	6	12

Active Interconnect Technology

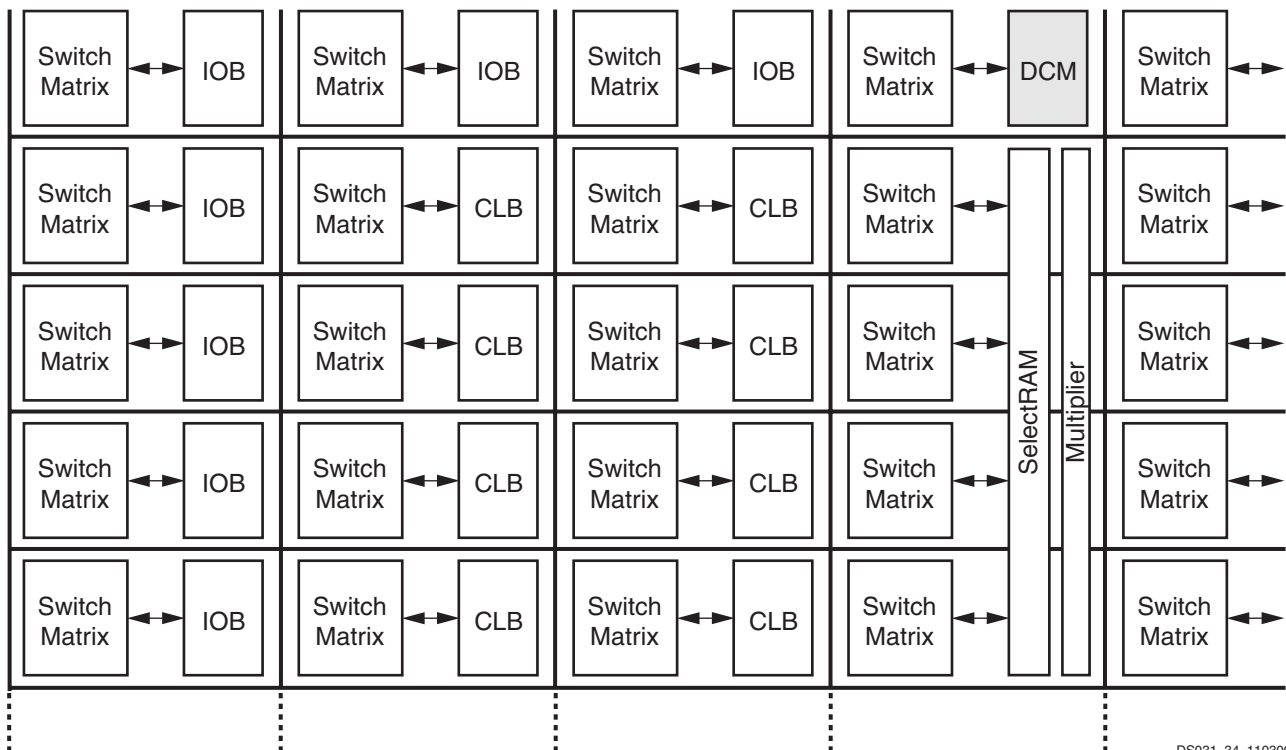
Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 46.



DS031_55_101000

Figure 46: Active Interconnect Technology

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 47.



DS031_34_110300

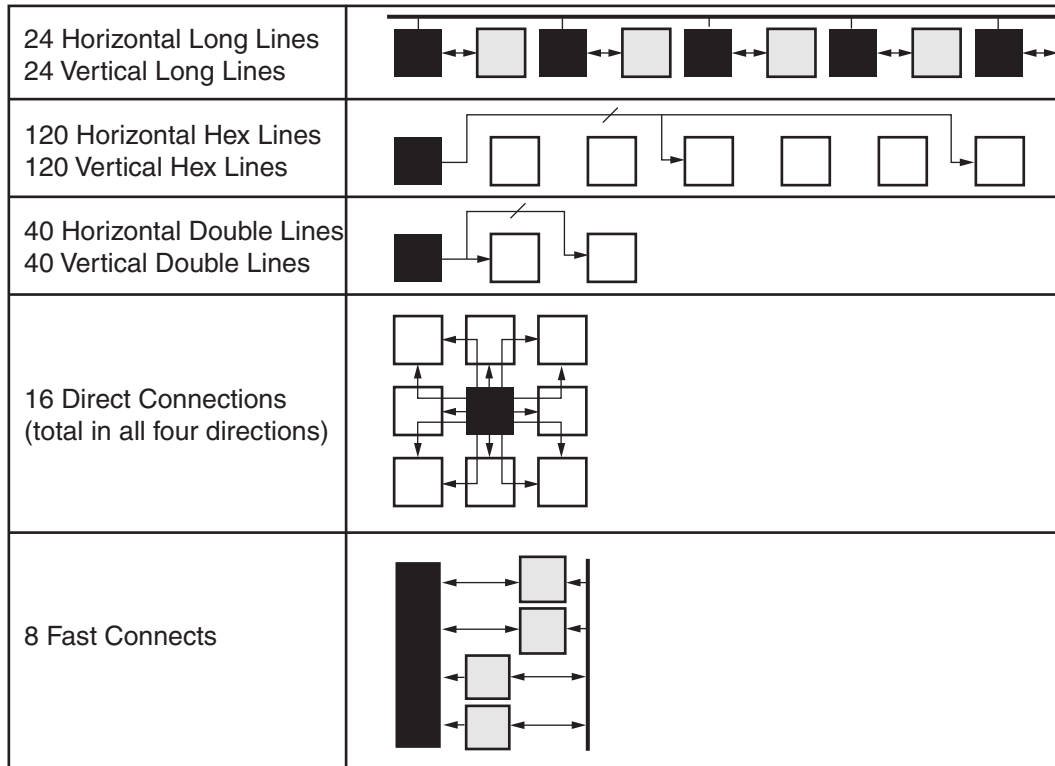
Figure 47: Routing Resources

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in [Figure 47](#), Virtex-II has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.



DS031_60_110200

Figure 48: Hierarchical Routing Resources

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).
- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant (see [Global Clock Multiplexer Buffers](#)).
- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row. (See [3-State Buffers](#).)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice. (See [CLB/Slice Configurations](#).)
- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See [Sum of Products](#).)

- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See "Shift Registers" on page 50.)

Creating a Design

Creating Virtex-II designs is easy with Xilinx development systems, supporting advanced design capabilities including incremental synthesis, modular design, integrated logic analysis, and the fastest place and route runtimes in the industry. This means designers get the performance they need, quickly.

As a result of the ongoing cooperative development efforts between Xilinx and EDA Alliance partners, designers can take advantage of the benefits provided by EDA technologies in the programmable logic design process. Xilinx development systems are available in a number of easy to use configurations within the Alliance Series and Foundation Series product families.

Alliance Series Solutions

Alliance Series solutions are designed to plug and play within a chosen design environment. Built using industry standard data formats and netlists, these stable, flexible products also enable Alliance EDA partners to deliver their best design automation capabilities to Xilinx customers, providing incremental synthesis, modular design, and error navigation -- all features developed with Xilinx EDA partners, for use with Xilinx development systems first.

Foundation Series Solutions

Foundation Series solutions feature Foundation Integrated Synthesis Environment (ISE) tools, a family of products that deliver all of the benefits of true HDL-based design in a seamlessly integrated design environment. An intuitive project navigator, as well as powerful HDL design and two HDL synthesis tools, ensure that high-quality results are achieved quickly and easily. The Foundation ISE product includes:

- State Diagram entry using StateCAD XE
- Automatic HDL Testbench generation using HDLBencher XE
- HDL Simulation using ModelSim XE-starter (MXE-starter).

MXE Starter is particularly useful in demonstrating the seamless integration available between the ISE design environment and ModelSim HDL Simulation tools.

Design Flow

Virtex-II design flow proceeds as follows:

- Design Entry
- Synthesis
- Implementation
- Verification

Most programmable logic designers iterate through these steps several times in the process of completing a design.

Design Entry

Xilinx development systems support the mainstream EDA design entry capabilities, ranging from schematic design to advanced HDL design methodologies. Given the high densities of the Virtex-II family, designs are most efficiently created using HDLs. To improve efficiency, many Xilinx customers employ incremental, modular, and Intellectual Property (IP) design techniques. When properly used, these techniques further accelerate the logic design process.

To enable designers to leverage existing investments in EDA tools, and to ensure high performance design flows, Xilinx jointly develops tools with leading EDA vendors, including:

- Aldec
- Cadence
- Exemplar
- Mentor Graphics
- Model Technology
- Synopsys
- Synplicity
- VSS

Complete information on Alliance Series partners and their associated design flows is available from the Xilinx Alliance Series web page:

www.xilinx.com/products/alliance.htm

Xilinx Foundation Series products offer schematic entry and HDL design capabilities as part of an integrated design solution - enabling one-stop shopping. These capabilities are powerful, easy to use, and they support the full portfolio of Xilinx programmable logic devices. HDL design capabilities include a color-coded HDL editor with integrated language templates, state diagram entry, and Core generation capabilities.

Synthesis

Alliance Series products are engineered to support advanced design flows with the industry's best synthesis tools for:

- Incremental synthesis
- RTL floorplanning
- Automated timing convergence
- Direct physical mapping

The Xilinx Foundation ISE product family includes synthesis capabilities from both FPGA Express and a proprietary synthesis tool referred to as Xilinx Synthesis Technology. Having two seamlessly integrated synthesis engines within the Foundation ISE products provides an alternative set of optimization

techniques for designs, helping to ensure that Foundation ISE can meet even the toughest timing requirements.

Both FPGA Express and Xilinx Synthesis Technology support the synthesis of VHDL and Verilog; however, only FPGA Express enables mixed-language synthesis. Future releases of the ISE design environment are planned to also integrate other third party synthesis tools, like Synplicity Synplify and Exemplar's Leonardo Spectrum.

Design Implementation

The Alliance Series and Foundation Series development systems both include Xilinx timing-driven implementation tools, frequently called “place and route” software. This robust suite of tools enables the creation of an intuitive, flexible, tightly integrated design flow that efficiently bridges the “logical” and “physical” design domains. This simplifies the task of defining a design, including its behavior, timing requirements, and optional layout (or floorplanning), as well as simplifying the task of analyzing reports generated during the implementation process.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or dynamic timing analysis (simulation), powerful in-circuit debugging techniques using Xilinx ChipScope ILA (Integrated Logic Analysis) is available. In these reconfigurable Xilinx FPGAs, designs can be verified in real time without the need for extensive sets of software simulation vectors. The development system supports both software simulation and in-circuit debugging techniques.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, the user can verify timing-critical portions of a design using the TRCE® static timing analyzer, or using a third party static timing analysis tool by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are

driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is “Modular Design”, part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical “logic block”, and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical “logic block” to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from “my module works in simulation” to “my module works in the FPGA”. This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Configuration

Virtex-II devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be reused as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1 and M0 are dedicated pins. An additional pin, HSWAP_EN is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configuration. By default, HSWAP_EN is tied High (internal pull-up) which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the boundary-scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and boundary scan pins are independent of the V_{CCO} . The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. (See "[Virtex-II DC Characteristics](#)" on page 76.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532/IEEE 1149)

A detailed description of configuration modes is provided in the *Virtex-II User Manual*.

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM which in turn feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active Low Chip Select (CS_B) signal and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In boundary-scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary scan is compliant with IEEE 1149.1-1993 standard and the new IEEE 1532 standard

for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes.

Table 28: Virtex-II Configuration Mode Pin Settings

Configuration Mode ¹	M2	M1	M0	CCLK Direction	Data Width	Serial D _{OUT} ²
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pullups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pullups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 29 lists the total number of bits required to configure each device.

Table 29: Virtex-II Bitstream Lengths

Device	# of Configuration Bits
XC2V40	338,208
XC2V80	597,408
XC2V250	1,591,584
XC2V500	2,557,856
XC2V1000	3,749,408
XC2V1500	5,166,240
XC2V2000	6,808,352
XC2V3000	9,589,408
XC2V4000	14,220,192
XC2V6000	19,752,096
XC2V8000	26,185,120
XC2V10000	33,519,264

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II User Manual*.

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II User Manual*.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is

loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Power-Down Sequence

The power-down sequence enables a designer to set the device into a low-power, inactive state. The sequence is initiated by pulling the PWRDWN_B pin Low.

If the PWRDWN_STAT option is selected using BitGen, the DONE pin can serve as the power-down status pin. When asserted, power-down has completed. After a successful wake-up, the status pin deasserts. While powered down, the only active pins are the PWRDWN_B and DONE. All inputs are off and all outputs are 3-stated.

While in the POWERDOWN state, the Power On Reset (POR) circuit is still active, but it does not reset the device if V_{CCINT} , V_{CCO} , or V_{CCAUX} falls below its minimum value. The POR circuit waits until the PWRDWN_B pin is released before resetting the device. Also, the PROG_B pin is not sampled while the device is in the POWERDOWN state. The PROG_B pin becomes active when the PWRDWN_B pin is released. Therefore, the device cannot be reset while in the POWERDOWN state.

The wake-up sequence is the reverse of the power-down sequence.

Virtex-II Electrical Characteristics

Virtex-II devices are provided in -4, -5, and -6 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed

grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 30: Absolute Maximum Ratings

Symbol	Description		Units
V_{CCINT}	Internal Supply voltage relative to GND	-0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	-0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	-0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	-0.5 to 4.0	V
V_{REF}	Input Reference Voltage	-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	-0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	-0.5 to 4.0	V
V_{CCINT}	Longest Supply Voltage Rise Time from 0 V - 1.425 V	50	ms
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temp.	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- Power supplies might turn on in any order.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.425	1.575	V
	Internal Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	3.0	3.6	V
	Auxiliary supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	3.0	3.6	V
V_{CCO}	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.2	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.0	3.6	V
	Battery voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.0	3.6	V

Notes:

- If V_{CCAUX} and V_{CCO} are both at 3.3V, they must use a common supply voltage.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)	All	1.2		V
V_{DRI}	Data Retention V_{CCAUX} Voltage (below which configuration data might be lost)	All	2.5		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current ¹	Device Dependent			
I_{CCOQ}	Quiescent V_{CCO} supply current ¹	Device Dependent			
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current ¹	Device Dependent			
I_{REF}	V_{REF} current per bank	All			μ A
I_L	Input or output leakage current	All			μ A
C_{IN}	Input capacitance (sample tested)	All			pF
I_{RPU}	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)	All	Note 2		mA
I_{RPD}	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)	All	Note 2		mA

Notes:

- With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
- Data are retained even if V_{CCO} drops to 0 V.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device¹ from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms).

Product	Description ²	Current Requirement ³
Virtex-II Family, Commercial Grade	Minimum required current supply	500 mA
Virtex-II Family, Industrial Grade	Minimum required current supply	500 mA

Notes:

- Ramp rate used for this specification is from 0 to 1.5 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
- Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
- Larger currents may result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	-0.5	0.8	2.0	3.6	0.4	2.4	24	-24
LVC MOS33	-0.5	0.8	2.0	3.6	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS25	-0.5	0.7	1.7	2.7	0.4	$V_{CCO} - 0.4$	24	-24
LVC MOS18	-0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	$V_{CCO} - 0.45$	16	-16
LVC MOS15	-0.5	20% V_{CCO}	70% V_{CCO}	1.65	0.4	$V_{CCO} - 0.45$	16	-16
PCI33_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI-X	-0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
HSTL I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	1.5	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	1.5	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	1.5	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	1.5	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	2.7	$V_{REF} - 0.65$	$V_{REF} + 0.65$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	2.7	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
AGP-2X	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LDT DC Specifications (LDT_25)

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	$R_T = 100$ ohm across Q and \bar{Q} signals	530	600	740	mV
Change in V_{OD} Magnitude	ΔV_{OD}	$R_T = 100$ ohm across Q and \bar{Q} signals			30	mV
Output Common Mode Voltage	V_{OS}	$R_T = 100$ ohm across Q and \bar{Q} signals	550	600	680	mV
Change in V_{OS} Magnitude	ΔV_{OS}				30	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and \bar{Q}	V_{OH}	$R_T = 100 \Omega$ across Q and \bar{Q} signals			1.475	V
Output Low Voltage for Q and \bar{Q}	V_{OL}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	0.925			V
Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	1.125	1.2	1.275	V
Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	2.2	V

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and \bar{Q}	V_{OH}	$R_T = 100 \Omega$ across Q and \bar{Q} signals			1.70	V
Output Low Voltage for Q and \bar{Q}	V_{OL}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	0.705			V
Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	1.125	1.200	1.275	V
Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{IDIFF}	Common-mode input voltage = 1.25 V				mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV				V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as "[Virtex-II Switching Characteristics](#)" on page 81 (speed files).

The following table provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Description	Pin to Pin (w/ I/O delays)	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder		
32-bit Address Decoder		
64-bit Address Decoder		
4:1 MUX		
8:1 MUX		
16:1 MUX		
32:1 MUX		
Combinatorial (pad to LUT to pad)		
Memory		
Block RAM		
Pad to setup		
Clock to Pad		
Distributed RAM		
Pad to setup		
Clock to Pad		

The following table shows internal (register-to-register) performance. Values are reported in MHz.

Description	Register to Register Performance	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder		
32-bit Address Decoder		
64-bit Address Decoder		
4:1 MUX		
8:1 MUX		
16:1 MUX		
32:1 MUX		
Register to LUT to Register		
8-bit Adder		
16-bit Adder		
64-bit Adder		
64-bit Counter		

Description	Register to Register Performance	Device Used & Speed Grade
64-bit Accumulators		
Multiplier 18x18 (with Block RAM inputs)		
Multiplier 18x18 (with Register inputs)		
Memory		
Block RAM		
Single-Port 4096 x 4 bits		
Single-Port 2048 x 9 bits		
Single-Port 1024 x 18 bits		
Single-Port 512 x 36 bits		
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits		
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits		
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits		
Distributed RAM		
Single-Port 32 x 8-bit		
Single-Port 64 x 8-bit		
Single-Port 128 x 8-bit		
Dual-Port 16 x 8		
Dual-Port 32 x 8		
Dual-Port 64 x 8		
Dual-Port 128 x 8		
Shift Registers		
128-bit SRL		
256-bit SRL		
FIFOs (Async. in Block RAM)		
1024 x 18-bit		
1024 x 18-bit		
FIFOs (Sync. in SRL)		
128 x 8-bit		
128 x 16-bit		
CAMs in Block RAM		
32 x 9-bit		
64 x 9-bit		
128 x 9-bit		
256 x 9-bit		
CAMs in SRL		
32 x 16-bit		
64 x 32-bit		
128 x 40-bit		
256 x 48-bit		
1024 x 16-bit		
1024 x 72-bit		

Virtex-II Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Final. Note that "[Virtex-II Performance Characteristics](#)" on page 80 are subject to these guidelines, as well. The status of each designation is defined as follows:

- Advance:** These speed files are based on additional simulation and testing of some family members. Although speed grades with this designation are considered relatively stable, some under-reporting might still occur. All family members do not necessarily transition to "Advance" at the same time. Typically, the slowest speed grades transition to "Advance" before faster speed grades.
- Preliminary:** Preliminary speed files are based on full device characterization. Devices and speed grades with this designation are considered safe for use in production designs. There are no under-reported delays.
- Final:** Final speed files are released once the family has enough production history and full correlation between the speeds files and devices is established over numerous production lots.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in "[IOB Input Switching Characteristics Standard Adjustments](#)" on page 82.

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All		1.03	1.19	ns, max
Pad to I output, with delay	T_{IOPID}			1.33	1.53	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All		1.28	1.48	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}			1.50	1.73	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All		1.10	1.26	ns, max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All		1.11 / 0	1.28 / 0	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$			1.41 / 0	1.62 / 0	ns, min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.20 / 0.04	0.23 / 0.04	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All		0.52	0.60	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All		0.85	0.98	ns, max
GSR to output IQ	T_{GSRQ}	All		8.25	9.49	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 32](#).

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade			Units
			-6	-5	-4	
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTTL				ns
	$T_{ILVCMOS33}$	LVC MOS33				ns
	$T_{ILVCMOS25}$	LVC MOS25				ns
	$T_{ILVCMOS18}$	LVC MOS18				ns
	$T_{ILVCMOS15}$	LVC MOS15				ns
	T_{ILVDS_25}	LVDS_25				ns
	T_{ILVDS_33}	LVDS_33				ns
	$T_{ILVPECL_33}$	LVPECL				ns
	$T_{IPCI_33_3}$	PCI, 33 MHz, 3.3 V				ns
	$T_{IPCI_66_3}$	PCI, 66 MHz, 3.3 V				ns
	T_{IPCI_X}	PCI-X, 133 MHz, 3.3 V				ns
	T_{IGTL}	GTL				ns
	$T_{IGTLPLUS}$	GTL P				ns
	T_{IHSTL_I}	HSTL I				ns
	T_{IHSTL_II}	HSTL II				ns
	T_{IHSTL_III}	HSTL III				ns
	T_{IHSTL_IV}	HSTL IV				ns
	T_{ISSTL2_I}	SSTL2 I				ns
	T_{ISSTL2_II}	SSTL2 II				ns
	T_{ISSTL3_I}	SSTL3 I				ns
	T_{ISSTL3_II}	SSTL3 II				ns
	T_{IAGP}	AGP-2X				ns
	$T_{ILVDCI33}$	LVDCI_33				ns
	$T_{ILVDCI25}$	LVDCI_25				ns
	$T_{ILVDCI18}$	LVDCI_18				ns
	$T_{ILVDCI15}$	LVDCI_15				ns
	$T_{ILVDCI_DV2_33}$	LVDCI_DV2_33				ns
	$T_{ILVDCI_DV2_25}$	LVDCI_DV2_25				ns
	$T_{ILVDCI_DV2_18}$	LVDCI_DV2_18				ns
	$T_{ILVDCI_DV2_15}$	LVDCI_DV2_15				ns
	T_{IGTL_DCI}	GTL_DCI				ns

Description	Symbol	Standard	Speed Grade			Units
			-6	-5	-4	
	T_{IGTLP_DCI}	GTLP_DCI				ns
	$T_{IHSTL_I_DCI}$	HSTL_I_DCI				ns
	$T_{IHSTL_II_DCI}$	HSTL_II_DCI				ns
	$T_{IHSTL_III_DCI}$	HSTL_III_DCI				ns
	$T_{IHSTL_IV_DCI}$	HSTL_IV_DCI				ns
	$T_{ISSTL2_I_DCI}$	SSTL2_I_DCI				ns
	$T_{ISSTL2_II_DCI}$	SSTL2_II_DCI				ns
	$T_{ISSTL3_I_DCI}$	SSTL3_I_DCI				ns
	$T_{ISSTL3_II_DCI}$	SSTL3_II_DCI				ns
	T_{ILD_T25}	LDT_25				ns
	T_{IULVDS_T25}	ULVDS_25				ns

Notes:

1. Input timing for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 32](#).

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 85.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delays					
O input to Pad	T_{IOOP}		4.40	5.06	ns, max
O input to Pad via transparent latch	T_{IOOLP}		4.65	5.34	ns, max
3-State Delays					
T input to Pad high-impedance (Note 2)	T_{IOTHZ}		1.53	1.76	ns, max
T input to valid data on Pad	T_{IOTON}		4.03	4.64	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$		1.78	2.05	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		4.28	4.93	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}		6.23	7.16	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}		5.05	5.80	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}		2.33	2.68	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		4.83	5.55	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}		0.52 / 0	0.60 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$		0.20 / 0	0.23 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$		0.52 / 0	0.60 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}		0.38 / 0	0.44 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$		0.15 / 0	0.18 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$		0.52 / 0	0.60 / 0	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}		4.80	5.52	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}		2.08	2.39	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		4.58	5.27	ns, max
GSR to Pad	T_{IOGSRQ}		5.75	6.61	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard	Speed Grade			Units
			-6	-5	-4	
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T _{OLVTTTL_S2}	LVTTTL, Slow, 2 mA				ns
	T _{OLVTTTL_S4}	4 mA				ns
	T _{OLVTTTL_S6}	6 mA				ns
	T _{OLVTTTL_S8}	8 mA				ns
	T _{OLVTTTL_S12}	12 mA				ns
	T _{OLVTTTL_S16}	16 mA				ns
	T _{OLVTTTL_S24}	24 mA				ns
	T _{OLVTTTL_F2}	LVTTTL, Fast, 2 mA				ns
	T _{OLVTTTL_F4}	4 mA				ns
	T _{OLVTTTL_F6}	6 mA				ns
	T _{OLVTTTL_F8}	8 mA				ns
	T _{OLVTTTL_F12}	12 mA				ns
	T _{OLVTTTL_F16}	16 mA				ns
	T _{OLVTTTL_F24}	24 mA				ns
	T _{OLVDS_25}	LVDS				ns
	T _{OLVDS_33}	LVDS				ns
	T _{OLVDSEXT_25}	LVDS				ns
	T _{OLVDSEXT_33}	LVDS				ns
	T _{OLDT_25}	LDT				ns
	T _{OBLVDS_25}	BLVDS				ns
	T _{OULVDS_25}	ULVDS				ns
	T _{OLVPECL_33}	LVPECL				ns
	T _{OPCI_33_3}	PCI, 33 MHz, 3.3 V				ns
	T _{OPCI_66_3}	PCI, 66 MHz, 3.3 V				ns
	T _{OPCIX}	PCI-X, 133 MHz, 3.3 V				ns
	T _{OGTL}	GTL				ns
	T _{OGTLP}	GTL P				ns
	T _{OHSTL_I}	HSTL I				ns
	T _{OHSTL_II}	HSTL II				ns
	T _{OHSTL_III}	HSTL III				ns
	T _{OHSTL_IV}	HSTL IV				ns
	T _{OSSTL2_I}	SSTL2 I				ns
	T _{OSSTL2_II}	SSTL2 II				ns

Description	Symbol	Standard	Speed Grade			Units
			-6	-5	-4	
	T _{OSSTL3_I}	SSTL3 I				ns
	T _{OSSTL3_II}	SSTL3 II				ns
	T _{OAGP}	AGP-2X				ns
	T _{OLVCMOS33_S2}	LVC MOS33, Slow, 2 mA				ns
	T _{OLVCMOS33_S4}	4 mA				ns
	T _{OLVCMOS33_S6}	6 mA				ns
	T _{OLVCMOS33_S8}	8 mA				ns
	T _{OLVCMOS33_S12}	12 mA				ns
	T _{OLVCMOS33_S16}	16 mA				ns
	T _{OLVCMOS33_S24}	24 mA				ns
	T _{OLVCMOS33_F2}	LVC MOS33, Fast, 2 mA				ns
	T _{OLVCMOS33_F4}	4 mA				ns
	T _{OLVCMOS33_F6}	6 mA				ns
	T _{OLVCMOS33_F8}	8 mA				ns
	T _{OLVCMOS33_F12}	12 mA				ns
	T _{OLVCMOS33_F16}	16 mA				ns
	T _{OLVCMOS33_F24}	24 mA				ns
	T _{OLVCMOS25_S2}	LVC MOS25, Slow, 2 mA				ns
	T _{OLVCMOS25_S4}	4 mA				ns
	T _{OLVCMOS25_S6}	6 mA				ns
	T _{OLVCMOS25_S8}	8 mA				ns
	T _{OLVCMOS25_S12}	12 mA				ns
	T _{OLVCMOS25_S16}	16 mA				ns
	T _{OLVCMOS25_S24}	24 mA				ns
	T _{OLVCMOS25_F2}	LVC MOS25, Fast, 2 mA				ns
	T _{OLVCMOS25_F4}	4 mA				ns
	T _{OLVCMOS25_F6}	6 mA				ns
	T _{OLVCMOS25_F8}	8 mA				ns
	T _{OLVCMOS25_F12}	12 mA				ns
	T _{OLVCMOS25_F16}	16 mA				ns
	T _{OLVCMOS25_F24}	24 mA				ns
	T _{OLVCMOS18_S2}	LVC MOS18, Slow, 2 mA				ns
	T _{OLVCMOS18_S4}	4 mA				ns
	T _{OLVCMOS18_S6}	6 mA				ns
	T _{OLVCMOS18_S8}	8 mA				ns
	T _{OLVCMOS18_S12}	12 mA				ns
	T _{OLVCMOS18_S16}	16 mA				ns

Description	Symbol	Standard	Speed Grade			Units
			-6	-5	-4	
	T _{OLVCMOS18_F2}	LVC MOS18, Fast, 2 mA				ns
	T _{OLVCMOS18_F4}	4 mA				ns
	T _{OLVCMOS18_F6}	6 mA				ns
	T _{OLVCMOS18_F8}	8 mA				ns
	T _{OLVCMOS18_F12}	12 mA				ns
	T _{OLVCMOS18_F16}	16 mA				ns
	T _{OLVCMOS15_S2}	LVC MOS15, Slow, 2 mA				ns
	T _{OLVCMOS15_S4}	4 mA				ns
	T _{OLVCMOS15_S6}	6 mA				ns
	T _{OLVCMOS15_S8}	8 mA				ns
	T _{OLVCMOS15_S12}	12 mA				ns
	T _{OLVCMOS15_S16}	16 mA				ns
	T _{OLVCMOS15_F2}	LVC MOS15, Fast, 2 mA				ns
	T _{OLVCMOS15_F4}	4 mA				ns
	T _{OLVCMOS15_F6}	6 mA				ns
	T _{OLVCMOS15_F8}	8 mA				ns
	T _{OLVCMOS15_F12}	12 mA				ns
	T _{OLVCMOS15_F16}	16 mA				ns
	T _{OLVDCI33}	LVDCI_33				ns
	T _{OLVDCI25}	LVDCI_25				ns
	T _{OLVDCI18}	LVDCI_18				ns
	T _{OLVDCI15}	LVDCI_15				ns
	T _{OLVDCI_DV2_33}	LVDCI_DV2_33				ns
	T _{OLVDCI_DV2_25}	LVDCI_DV2_25				ns
	T _{OLVDCI_DV2_18}	LVDCI_DV2_18				ns
	T _{OLVDCI_DV2_15}	LVDCI_DV2_15				ns
	T _{OGTL_DCI}	GTL_DCI				ns
	T _{OGTLP_DCI}	GTL_P_DCI				ns
	T _{OHSTL_I_DCI}	HSTL_I_DCI				ns
	T _{OHSTL_II_DCI}	HSTL_II_DCI				ns
	T _{OHSTL_III_DCI}	HSTL_III_DCI				ns
	T _{OHSTL_IV_DCI}	HSTL_IV_DCI				ns
	T _{OSSTL2_I_DCI}	SSTL2_I_DCI				ns
	T _{OSSTL2_II_DCI}	SSTL2_II_DCI				ns
	T _{OSSTL3_I_DCI}	SSTL3_I_DCI				ns
	T _{OSSTL3_II_DCI}	SSTL3_II_DCI				ns

Calculation of $T_{I\text{OOP}}$ as a Function of Capacitance

$T_{I\text{OOP}}$ is the propagation delay from the O input of the IOB to the pad. The values for $T_{I\text{OOP}}$ are based on the standard capacitive load (C_{SL}) for each I/O standard, as listed in [Table 31](#).

Table 31: Constants for Use in Calculation of $T_{I\text{OOP}}$

Standard	Csl (pF)	fl (ns/pF)
LVTTTL Fast Slew Rate, 2mA drive	35	
LVTTTL Fast Slew Rate, 4mA drive	35	
LVTTTL Fast Slew Rate, 6mA drive	35	
LVTTTL Fast Slew Rate, 8mA drive	35	
LVTTTL Fast Slew Rate, 12mA drive	35	
LVTTTL Fast Slew Rate, 16mA drive	35	
LVTTTL Fast Slew Rate, 24mA drive	35	
LVTTTL Slow Slew Rate, 2mA drive	35	
LVTTTL Slow Slew Rate, 4mA drive	35	
LVTTTL Slow Slew Rate, 6mA drive	35	
LVTTTL Slow Slew Rate, 8mA drive	35	
LVTTTL Slow Slew Rate, 12mA drive	35	
LVTTTL Slow Slew Rate, 16mA drive	35	
LVTTTL Slow Slew Rate, 24mA drive	35	
LVC MOS33	35	
LVC MOS25	35	
LVC MOS18	35	
LVC MOS15	35	
PCI 33MHZ 3.3 V	10	
PCI 66 MHz 3.3 V	10	
PCI-X 133 MHz 3.3 V	10	
GTL	0	
GTL P	0	
HSTL Class I	20	
HSTL Class II	20	
HSTL Class III	20	
HSTL Class IV	20	
SSTL2 Class I	30	
SSTL2 Class II	30	
SSTL3 Class I	30	
SSTL3 Class II	30	
AGP-2X	10	

Notes:

- I/O parameter measurements are made with the capacitance values shown above.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{I\text{OOP}}$.

$$T_{I\text{OOP}} = T_{I\text{OOP}} + T_{\text{OPADJUST}} + (C_{\text{LOAD}} - C_{\text{SL}}) * fl$$

Where:

T_{OPADJUST} is reported above in the Output Delay Adjustment section.

C_{LOAD} is the capacitive load for the design.

Table 32: Delay Measurement Methodology

Standard	V_L^1	V_H^1	Meas. Point	V_{REF} (Typ) ²
LVTTTL	0	3	1.4	-
LVC MOS33	0	3.3	1.65	-
LVC MOS25	0	2.5	1.125	-
LVC MOS18	0	1.8	0.9	-
LVC MOS15	0	1.5	0.75	-
PCI33_3	Per PCI Specification			-
PCI66_3	Per PCI Specification			-
PCIX33_3	Per PCI-X Specification			-
GTL	$V_{\text{REF}} - 0.2$	$V_{\text{REF}} + 0.2$	V_{REF}	0.80
GTL P	$V_{\text{REF}} - 0.2$	$V_{\text{REF}} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.75
HSTL Class II	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.90
SSTL3 I & II	$V_{\text{REF}} - 1.0$	$V_{\text{REF}} + 1.0$	V_{REF}	1.5
SSTL2 I & II	$V_{\text{REF}} - 0.75$	$V_{\text{REF}} + 0.75$	V_{REF}	1.25
AGP-2X	$V_{\text{REF}} - (0.2xV_{\text{CCO}})$	$V_{\text{REF}} + (0.2xV_{\text{CCO}})$	V_{REF}	Per AGP Spec
LVDS_25			1.2	
LVDS_33			1.2	
LVDS EXT_25			1.2	
LVDS EXT_33			1.2	

Table 32: Delay Measurement Methodology

Standard	V_L^1	V_H^1	Meas. Point	V_{REF} (Typ) ²
ULVDS_25			0.6	
LDT_25			0.6	
LVPECL	1.6 - 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in [Table 31](#).
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
5. Use of IBIS models results in a more accurate prediction of the propagation delay:
 - a. Model the output in an IBIS simulation into the standard capacitive load.
 - b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
 - c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
 - d. Record the results from the new simulation.
 - e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
GCLK IOB and Buffer					
Global Clock PAD to output.	T_{GPIO}		0.34	0.39	ns, max
Global Clock Buffer I input to O output	T_{GIO}		0.50	0.58	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 15). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}		0.44	0.50	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}		0.64	0.73	ns, max
5-input function: F/G inputs to X output	T_{IF5X}		0.81	0.93	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}		0.37	0.43	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}		0.29	0.33	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}		0.29	0.33	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}		0.78	0.90	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}		0.41	0.47	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}		0.41	0.48	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}		1.10	1.26	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}		0.31 / 0	0.36 / 0	ns, min
DY inputs	T_{DYCK}/T_{CKDY}		0.24 / 0	0.27 / 0	ns, min
DX inputs	T_{DXCK}/T_{CKDX}		0.24 / 0	0.27 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}		0.20 / 0	0.23 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}		0.17 / 0.08	0.20 / 0.09	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}		0.54	0.62	ns, min
Minimum Pulse Width, Low	T_{CL}		0.54	0.62	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}		0.54	0.62	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}		0.44	0.51	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}		934.58	813.67	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$		1.82	2.09	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$		2.09	2.41	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$		1.92	2.21	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		0.64 / 0	0.73 / 0	ns, min
F/G address inputs	T_{AS}/T_{AH}		0.42 / 0	0.48 / 0	ns, min
CE input (WE)	T_{WES}/T_{WEH}		0.44 / 0	0.51 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}		2.10	2.42	ns, min
Minimum Pulse Width, Low	T_{WPL}		2.10	2.42	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		4.20	4.83	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}		0.31	0.35	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}		0.13	0.15	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}		0.75	0.86	ns, max
Clock CLK to Shiftout	T_{CKSH}		0.12	0.14	ns, max
Clock CLK to F5 output	T_{REGF5}		0.41	0.47	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}		0.31 / 0	0.36 / 0	ns, min
CE input (WS)	T_{WSS}/T_{WSH}		0.20 / 0.04	0.23 / 0.04	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}		2.10	2.42	ns, min
Minimum Pulse Width, Low	T_{SRPL}		2.10	2.42	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT}		4.18	4.83	ns, max
Input to Pin34	T_{MULT}		4.07	4.70	ns, max
Input to Pin33	T_{MULT}		3.96	4.58	ns, max
Input to Pin32	T_{MULT}		3.85	4.45	ns, max
Input to Pin31	T_{MULT}		3.74	4.32	ns, max
Input to Pin30	T_{MULT}		3.63	4.20	ns, max
Input to Pin29	T_{MULT}		3.52	4.07	ns, max
Input to Pin28	T_{MULT}		3.41	3.94	ns, max
Input to Pin27	T_{MULT}		3.30	3.81	ns, max
Input to Pin26	T_{MULT}		3.19	3.69	ns, max
Input to Pin25	T_{MULT}		3.08	3.56	ns, max
Input to Pin24	T_{MULT}		2.97	3.43	ns, max
Input to Pin23	T_{MULT}		2.86	3.31	ns, max
Input to Pin22	T_{MULT}		2.75	3.18	ns, max
Input to Pin21	T_{MULT}		2.64	3.05	ns, max
Input to Pin20	T_{MULT}		2.53	2.93	ns, max
Input to Pin19	T_{MULT}		2.42	2.80	ns, max
Input to Pin18	T_{MULT}		2.31	2.67	ns, max
Input to Pin17	T_{MULT}		2.20	2.54	ns, max
Input to Pin16	T_{MULT}		2.09	2.42	ns, max
Input to Pin15	T_{MULT}		1.98	2.29	ns, max
Input to Pin14	T_{MULT}		1.87	2.16	ns, max
Input to Pin13	T_{MULT}		1.76	2.04	ns, max
Input to Pin12	T_{MULT}		1.65	1.91	ns, max
Input to Pin11	T_{MULT}		1.54	1.78	ns, max
Input to Pin10	T_{MULT}		1.43	1.66	ns, max
Input to Pin9	T_{MULT}		1.32	1.53	ns, max
Input to Pin8	T_{MULT}		1.21	1.40	ns, max
Input to Pin7	T_{MULT}		1.10	1.27	ns, max
Input to Pin6	T_{MULT}		0.99	1.15	ns, max
Input to Pin5	T_{MULT}		0.88	1.02	ns, max
Input to Pin4	T_{MULT}		0.77	0.89	ns, max
Input to Pin3	T_{MULT}		0.66	0.77	ns, max
Input to Pin2	T_{MULT}		0.55	0.64	ns, max
Input to Pin1	T_{MULT}		0.44	0.51	ns, max
Input to Pin0	T_{MULT}		0.33	0.39	ns, max

Block SelectRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}		2.89	3.33	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}		0.30 / 0.00	0.35 / 0.00	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}		0.30 / 0.00	0.35 / 0.00	ns, min
EN input	T_{BECK}/T_{BCKE}		1.60 / 1.30	1.84 / 1.50	ns, min
RST input	T_{BRCK}/T_{BCKR}		1.38 / 1.08	1.59 / 1.25	ns, min
WEN input	T_{BWCK}/T_{BCKW}		0.60 / 0.30	0.69 / 0.35	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}		1.45	1.67	ns, min
Minimum Pulse Width, Low	T_{BPWL}		1.45	1.67	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
IN input to OUT output	T_{IO}		0.24	0.28	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.46	0.53	ns, max
TRI input to valid data on OUT output	T_{ON}		0.46	0.53	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
TMS and TDI Setup times before TCK	T_{TAPTK}				ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}				ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}				ns, max
Maximum TCK clock frequency	F_{TCK}				MHz, max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *With* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 85.	$T_{ICKOFDCM}$					ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 31](#) and [Table 32](#).
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *Without* DCM

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 85.	T_{ICKOF}					ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 31](#) and [Table 32](#).
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTTL Standard, *With DCM*

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 82.						
No Delay Global Clock and IFF	T_{PSDCM}/T_{PHDCM}					ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTTL Standard *Without DCM*

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 82.						
Full Delay Global Clock and IFF	T_{PSFD}/T_{PHFD}					ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DCM Timing Parameters

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605; all devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Table 33: Operating Frequency Ranges

Description	Symbol	Constraints	Speed Grade						Units	
			-6		-5		-4			
			Min	Max	Min	Max	Min	Max		
Output Clocks (Low Frequency Mode)										
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF									MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF									MHz
CLKDV	CLKOUT_FREQ_DV_LF									MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF									MHz
Input Clocks (Low Frequency Mode)										
CLKIN (using DLL outputs ¹)	CLKIN_FREQ_DLL_LF									MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_LF									MHz
PSCLK	PSCLK_FREQ_LF									MHz
Output Clocks (High Frequency Mode)										
CLK0, CLK180	CLKOUT_FREQ_1X_HF									MHz
CLKDV	CLKOUT_FREQ_DV_HF									MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF									MHz
Input Clocks (High Frequency Mode)										
CLKIN (using DLL outputs ¹)	CLKIN_FREQ_DLL_HF									MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_HF									MHz
PSCLK	PSCLK_FREQ_HF									MHz

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Table 34: Input Clock Tolerances

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz							ns
CLKIN ²	CLKIN_PULSE	1 - 10 MHz							ns
		10 - 25 MHz							ns
		25 - 50 MHz							ns
		50 - 100 MHz							ns
		100 - 150 MHz							ns
		150 - 200 MHz							ns
		200 - 250 MHz							ns
		250 - 300 MHz							ns
		300 - 350 MHz							ns
		350 - 400 MHz							ns
		> 400 MHz							ns
Input Clock Period Drift (Low Frequency Mode)									
CLKIN (using DLL outputs ¹)	CLKIN_PER_DRIFT_DLL_LF								ns
CLKIN (using CLKFX outputs)	CLKIN_PER_DRIFT_FX_LF								ns
Input Clock Period Drift (High Frequency Mode)									
CLKIN (using DLL outputs ¹)	CLKIN_PER_DRIFT_DLL_HF								ns
CLKIN (using CLKFX outputs)	CLKIN_PER_DRIFT_FX_HF								ns
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs ¹)	CLKIN_PER_JITT_DLL_LF								ps
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_LF								ps
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs ¹)	CLKIN_PER_JITT_DLL_HF								ps
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_HF								ps
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT								ns

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Table 35: Output Clock Jitter

Description	Symbol	Constraints	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Clock Synthesis Period Jitter									
CLK0	CLKOUT_PER_JITT_0								ps
CLK90	CLKOUT_PER_JITT_90								ps
CLK180	CLKOUT_PER_JITT_180								ps
CLK270	CLKOUT_PER_JITT_270								ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X								ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1								ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2								ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX								ps

Table 36: Output Clock Phase Alignment

Description	Symbol	Constraints	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Phase Offset Between CLKIN and CLKFB									
CLKIN/CLKFB	CLKIN_CLKFB_PHASE								ps
Phase Offset Between Any DCM Outputs									
All CLK* outputs	CLKOUT_PHASE								ps
Duty Cycle Precision									
DLL outputs ¹	CLKOUT_DUTY_CYCLE_DLL								ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX								ps

Table 37: Miscellaneous Timing Parameters

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Time Required to Achieve LOCK									
Using DLL outputs ¹	LOCK_DLL								
		> 60MHz							us
		50 - 60 MHz							us
		40 - 50 MHz							us
		30 - 40 MHz							us
		24 - 30 MHz							us
Using CLKFX outputs	LOCK_FX								us
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT								us
Fine Phase Shifting									
Absolute shifting range	FINE_SHIFT_RANGE								ns
Delay Lines									
Tap delay resolution	DCM_TAP								ps

Notes:

- “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- Specification also applies to PSCLK.

Table 38: Parameter Cross-Reference

Libraries Guide	Data Sheet
DLL_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_{1X 2X DV}_LF
DFS_CLKOUT_{MINIMAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MINIMAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_{1X DV}_HF
DFS_CLKOUT_{MINIMAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MINIMAX}_HF	CLKIN_FREQ_FX_HF

Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. Table 39 and Table 40 show the maximum possible number of user I/Os in wire-bond and flip-chip packages, respectively. Table 41 shows the number of available user I/Os for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2,

PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD) and VBATT.

Table 39: Wire-Bond Packages Information

Package	CS144	FG256	FG456	FG676	BG575	BG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Table 40: Flip-Chip Packages Information

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 41: Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)

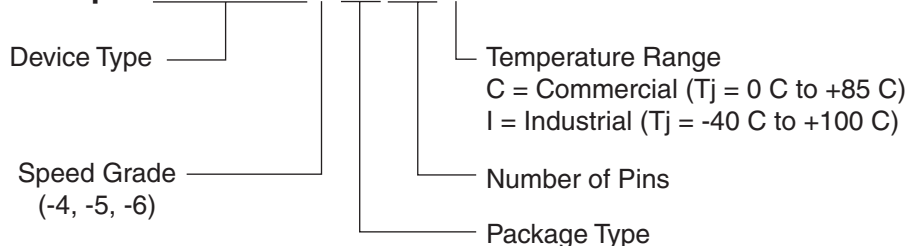
Package	Available I/Os											
	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000	XC2V10000
CS144	88	92	92									
FG256	88	120	172	172	172							
FG456			200	264	324							
FG676						392	456	484				
FF896					432	528	624					
FF1152								720	824	824	824	824
FF1517									912	1,104	1,108	1,108
BG575					328	392	408					
BG728							456	516				
BF957							624	684	684	684	684	684

Note: All devices in a particular package are pin-out (footprint) compatible. In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages.

Virtex-II Ordering Information

Virtex-II ordering information is shown in Figure 49

Example: XC2V1000-5FG456C



DS031_35_050200

Figure 49: Virtex-II Ordering Information

Revision History

This section records the change history for the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.

