4Kx36 Asynchronous FIFO MODULE *ADVANCED**

FEATURES

- Fast Access Times of 20, 30, 40ns
- Packaging:
  - 132-pin Hermetic Ceramic Quad Flatpack, CQFP, 24mm (0.950") sq.
- Asynchronous First-In First-Out (FIFO) Buffer Memory
- Asynchronous and Simultaneous Read and Write
- Status Flags: Empty, Half-Full, Full
- Retransmit Capability in stand-alone.
- 5V ± 10% Power Supply
- Industrial and Military Temperature Ranges
- Low Power CMOS
- TTL Compatible
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

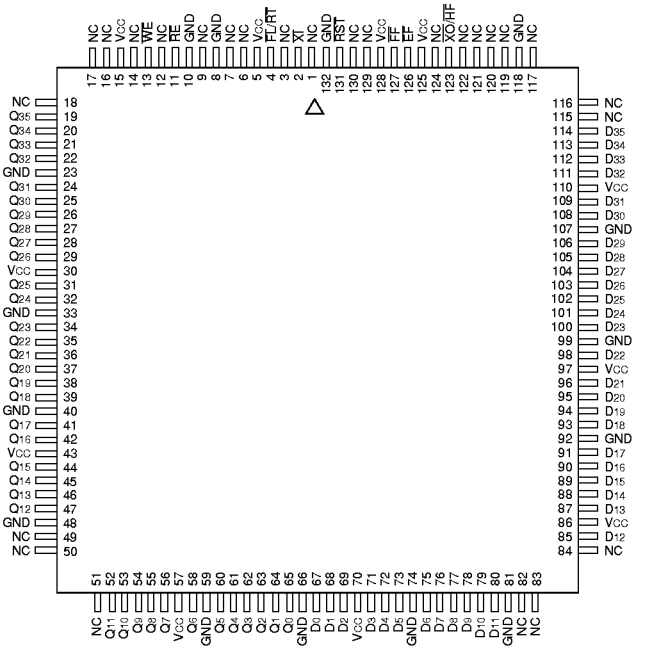
** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FUNCTIONAL DESCRIPTION

- WT4K36-XGX is First-In First-out (FIFO) memory, organized as 4K x 36 in a 132-pin Ceramic QFP. The memory is organized such that the data is read in the same sequential order that it is written. Full and Empty Flags are provided to prevent overrun or underrun. Three pins are provided to facilitate depth expansion.
- The read and write operations may be asynchronous. The write operation occurs when the Write Enable ($\overline{WE}$) signal is low. Read occurs when Read Enable ($\overline{RE}$) goes low. The data outputs go to the high impedance state when $\overline{RE}$ is High.
- A Half-Full ($\overline{HF}$) output flag is provided and is only valid in the stand-alone configuration. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.
- In the stand-alone configuration, a low on the Retransmit ($\overline{RT}$) input causes the FIFO to retransmit the data. Read Enable ($\overline{RE}$) and Write Enable ($\overline{WE}$) must both be high during retransmit, and then $\overline{RE}$ is used to access the data.

FIG. 1 PIN CONFIGURATION FOR WT4K36-XGX

TOP VIEW



PIN DESCRIPTION

$D_{0\text{-}35}$	Data Inputs
$Q_{0\text{-}35}$	Data Outputs
$\overline{RST}$	Reset Input
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
$\overline{FL}/\overline{RT}$	First Load/Retransmit
$\overline{XI}$	Expansion Input
$\overline{FF}$	Full Flag Output
$\overline{EF}$	Empty Flag Output
$\overline{XO}/\overline{HF}$	Expansion Output/ Half-Full Flag Output
Vcc	Power Supply
GND	Ground
NC	Not Connected

SIGNAL DESCRIPTIONS

DATA IN (D_{0-35})

Data Inputs for 36-bit wide data.

DATA OUT (Q_{0-35})

Data Outputs for 36-bit wide data. These outputs are in high-impedance condition whenever Read Enable ($\overline{RE}$) is in a High State.

RESET ($\overline{RST}$)

Reset is accomplished whenever the Reset ($\overline{RST}$) input is taken to a Low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place.

WRITE ENABLE ($\overline{WE}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold times must be adhered - to, with respect to the rising edge of the Write Enable ($\overline{WE}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next operation, the Half-Full Flag ($\overline{HF}$) will be set to Low, and will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go Low on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go High after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{WE}$, so external changes in $\overline{WE}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{RE}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{RE}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{RE}$) goes High, the Data Outputs will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go Low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{RE}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual purpose input. In Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded. The Single device Mode is initiated by grounding the Expansion Input ($\overline{XI}$).

The device can be made to retransmit data when Retransmit Enable Control ($\overline{RT}$) input is pulsed Low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{RE}$) and Write Enable ($\overline{WE}$) must be in the High state during retransmit. This feature is useful when less than 4,096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION INPUT ($\overline{XI}$)

This input is a dual-purpose pin. Expansion Input ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion Input ($\overline{XI}$) is connected to Expansion Output ($\overline{XO}$) of the previous device in the Depth Expansion Mode.

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go Low, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RST}$), the Full Flag ($\overline{FF}$) will go Low after 4,096 writes.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go Low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

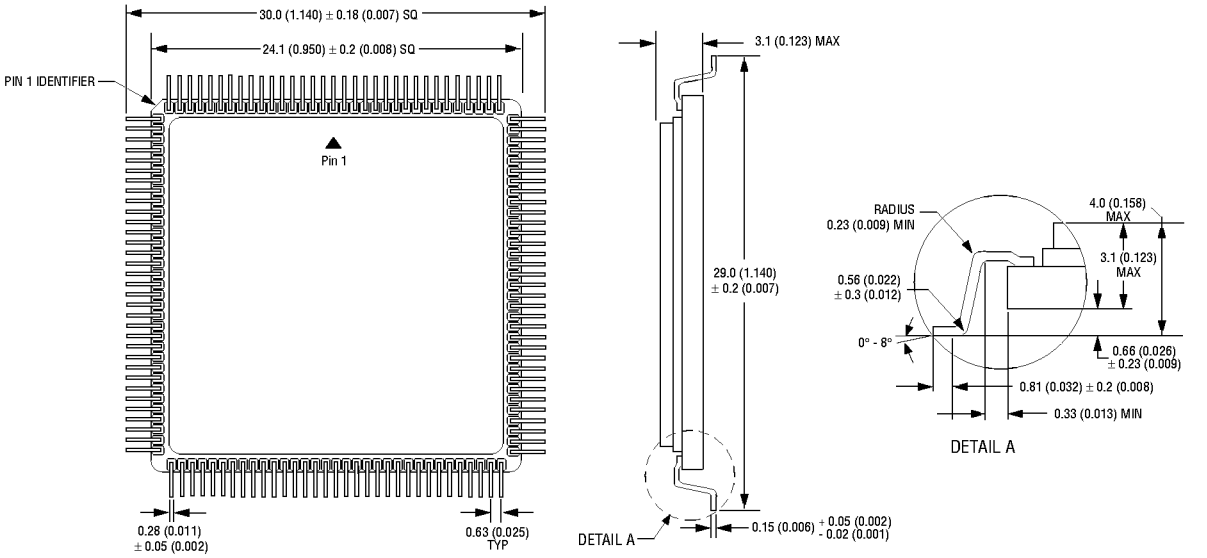
EXPANSION OUTPUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion Input ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to Low and will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In Depth Expansion Mode, Expansion Input ($\overline{XI}$) is connected to Expansion Output ($\overline{XO}$) of the previous device. This output acts as a signal to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the read pointer reaches the last location of memory.

PACKAGE 505: 132 PIN, CERAMIC QUAD FLAT PACK, CQFP (G)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W T 4K 36 - XX G X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
M = Military -55°C to +125°C
I = Industrial -40°C to +85°C

PACKAGE TYPE:
G = 24mm sq,132-pin Ceramic Quad Flatpack, CQFP (Package 505)

ACCESS TIME (ns)

ORGANIZATION, 4Kx36

Asynchronous FIFO

WHITE MICROELECTRONICS