To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8172TK

SMALL PACKAGE FREQUENCY UP-CONVERTER IC

DESCRIPTION

The μPC8172TK is a silicon monolithic integrated circuit designed as frequency up-converter for cellular telephone transmitter stage.

This TK suffix IC which is smaller package than conventional TB suffix IC contribute to reduce your system size.

This IC is manufactured using our 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process.

FEATURES

- High output frequency : f_{RFout} = 0.8 to 2.5 GHz
- Circuit current : I_{CC} = 9.0 mA TYP.
- High-density surface mounting : 6-pin lead-less minimold package
- Supply voltage : V_{CC} = 2.7 to 3.3 V

APPLICAIONS

- PCS1900M
- 2.4 GHz band transmitter/receiver system (wireless LAN etc.)
- RF module etc.

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μ PC8172TK-E2	μ PC8172TK-E2-A	6-pin lead-less minimold (1511) (Pb-Free) Note	6A	• Embossed tape 8 mm wide • Pin 1, 6 face the perforation side of the tape • Qty 5 kpcs/reel

Note With regards to terminal solder (the solder contains lead) plated products (conventionally plated), contact your nearby sales office.

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: μPC8172TK

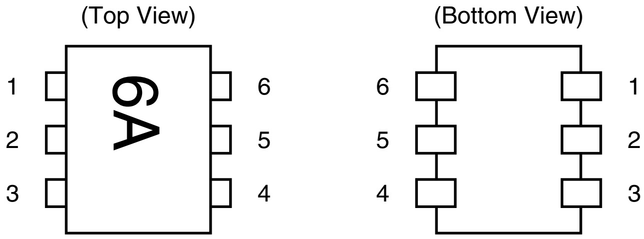
Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

Document No. PU10407EJ02V0DS (2nd edition)
Date Published December 2004 CP(K)
Printed in Japan

The mark ★ shows major revised points.

CONTENTS

1. PIN CONNECTIONS



Pin No.	Pin Name
1	IFinput
2	GND
3	LOinput
4	PS
5	V_{CC}
6	RFoutput

Caution Pin arrangement differs from the conventional 6-pin super mini-mold type (μPC8172TB).

2. PRODUCT LINE-UP

Part No.	Package	I_{CC} (mA)	f_{RFout} (GHz)	CG (dB)		
				@RF0.9 (GHz) Note	@RF1.9 (GHz)	@RF2.4 (GHz)
μPC8172TK	6-pin lead-less minimold	9.0	0.8 to 2.5	9.5	8.5	8.0
μPC8106TB	6-pin super minimold	9.0	0.4 to 2.0	9.0	7.0	–
μPC8109TB	(1511)	5.0	0.4 to 2.0	6.0	4.0	–
μPC8163TB		16.5	0.8 to 2.0	9.0	5.5	–
μPC8172TB		9.0	0.8 to 2.5	9.5	8.5	8.0
μPC8187TB		15.0	0.8 to 2.5	11.0	11.0	10.0

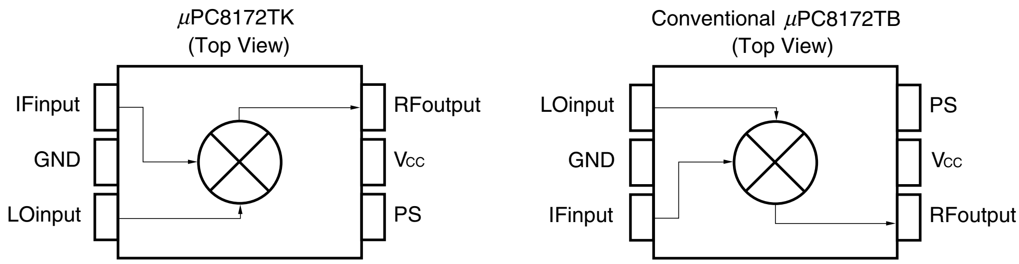
Part No.	$P_{O (sat)}$ (dBm)			OIP_3 (dBm)		
	@RF0.9 (GHz) Note	@RF1.9 (GHz)	@RF2.4 (GHz)	@RF0.9 (GHz) Note	@RF1.9 (GHz)	@RF2.4 (GHz)
μPC8172TK	+0.5	0	−0.5	+7.5	+6.0	+4.0
μPC8106TB	−2.0	−4.0	–	+5.5	+2.0	–
μPC8109TB	−5.5	−7.5	–	+1.5	−1.0	–
μPC8163TB	+0.5	−2.0	–	+9.5	+6.0	–
μPC8172TB	+0.5	0	−0.5	+7.5	+6.0	+4.0
μPC8187TB	+4.0	+2.5	+1.0	+10.0	+10.0	+8.5

Note f_{RFout} = 0.83 GHz@ μPC8163TB, μPC8187TB

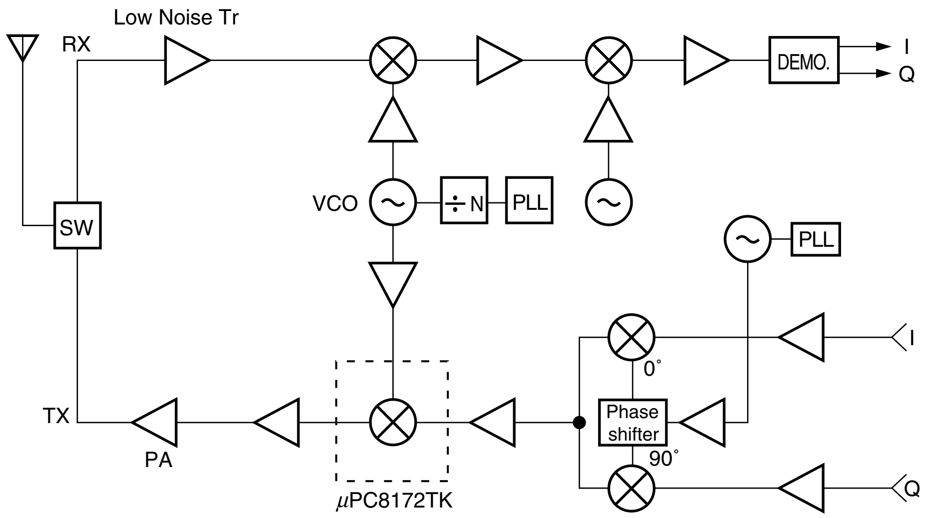
Remarks 1. Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

2. To know the associated product, please refer to each latest data sheet.

3. BLOCK DIAGRAM

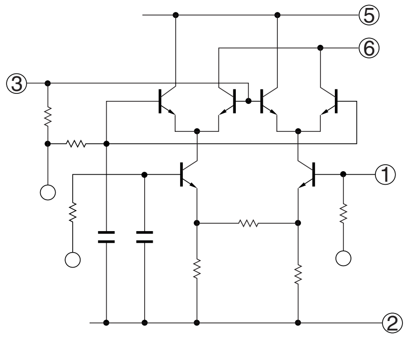
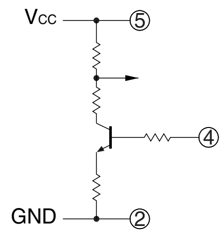


4. SYSTEM APPLICATION EXAMPLE



Caution To know the associated products, please refer to each latest data sheet.

5. PIN EXPLANATION

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Applied Voltage (V)</th><th>Pin Voltage (V) Note</th><th>Function and Applications</th><th>Internal Equivalent Circuit</th></tr>
<tr><td>1</td><td>IFinput</td><td>–</td><td>1.3</td><td>This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.</td><td rowspan="5"></td></tr>
<tr><td>2</td><td>GND</td><td>GND</td><td>–</td><td>GND pin.
Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.</td></tr>
<tr><td>3</td><td>LOinput</td><td>–</td><td>2.4</td><td>Local input pin.
Recommendable input level is –10 to 0 dBm.</td></tr>
<tr><td>5</td><td>V_{CC}</td><td>2.7 to 3.3</td><td>–</td><td>Supply voltage pin.</td></tr>
<tr><td>6</td><td>RFoutput</td><td>Same bias as V_{CC} through external inductor</td><td>–</td><td>This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.</td></tr>
<tr><td>4</td><td>PS</td><td>V_{CC}/GND</td><td>–</td><td>Power save control pin.
Bias controls operation as follows.<table><tr><th>Pin bias</th><th>Control</th></tr><tr><td>V_{CC}</td><td>Operation</td></tr><tr><td>GND</td><td>Power Save</td></tr></table></td><td></td></tr>
</table>

Note Each pin voltage is measured with $V_{CC} = V_{PS} = V_{RFout} = 3.0$ V

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C	3.6	V
PS pin input Voltage	V_{PS}	T_A = +25°C	3.6	V
Power Dissipation of Package	P_D	T_A = +85°C **Note**	203	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}		+10	dBm

Note Mounted on double-side copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

7. RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V_{CC}	2.7	3.0	3.3	V	Same voltage should be applied to pin 5 and pin 6.
Operating Ambient Temperature	T_A	–40	+25	+85	°C	
Local Input Level	P_{LOin}	–10	–5	0	dBm	Z_S = 50 Ω (without matching)
RF Output Frequency	f_{RFout}	0.8	–	2.5	GHz	With external matching circuit
IF Input Frequency	f_{IFin}	50	–	600	MHz	

8. ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, f_{IFin} = 240 MHz, P_{LOin} = –5 dBm, and V_{PS} ≥ 2.7 V, unless otherwise specified)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal		5.5	9.0	13	mA
Circuit Current In Power Save Mode	$I_{CC (PS)}$	V_{PS} = 0 V		–	–	2.0	μA
Conversion Gain	CG1	f_{RFout} = 0.9 GHz Note1	P_{IFin} = –30 dBm, f_{IFin} = 240 MHz	6.5	9.5	12.5	dB
	CG2	f_{RFout} = 1.9 GHz Note2		5.5	8.5	11.5	dB
	CG3	f_{RFout} = 2.4 GHz Note2		5.0	8.0	11.0	dB
Saturated RF output Power	$P_{O (sat)}$ 1	f_{RFout} = 0.9 GHz Note1	P_{IFin} = 0 dBm, f_{IFin} = 240 MHz	–2.5	+0.5	–	dBm
	$P_{O (sat)}$ 2	f_{RFout} = 1.9 GHz Note2		–3.5	0	–	dBm
	$P_{O (sat)}$ 3	f_{RFout} = 2.4 GHz Note2		–4.0	–0.5	–	dBm

Notes 1. f_{RFout} < f_{LOin} @ f_{RFout} = 0.9 GHz

2. f_{LOin} < f_{RFout} @ f_{RFout} = 1.9 GHz/2.4 GHz

9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

(T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, P_{LOin} = –5 dBm, and V_{PS} ≥ 2.7 V, unless otherwise specified)

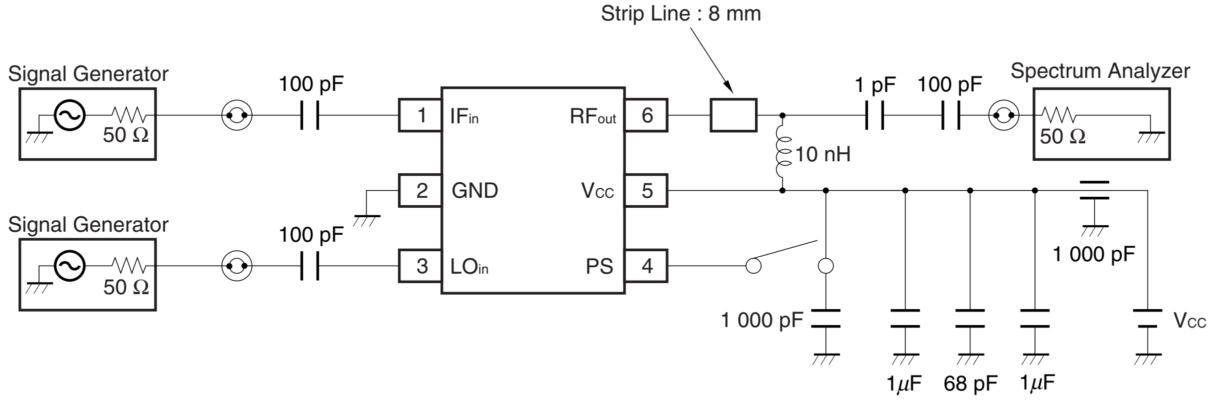
Parameter		Symbol	Test Conditions		Data	Unit
Output 3rd Order Distortion Intercept Point		OIP_31	f_{RFout} = 0.9 GHz Note1	$f_{IFin}1$ = 240 MHz, $f_{IFin}2$ = 241 MHz	+7.5	dBm
		OIP_32	f_{RFout} = 1.9 GHz Note2		+6.0	dBm
		OIP_33	f_{RFout} = 2.4 GHz Note2		+4.0	dBm
Input 3rd Order Distortion Intercept Point		IIP_31	f_{RFout} = 0.9 GHz Note1	$f_{IFin}1$ = 240 MHz, $f_{IFin}2$ = 241 MHz	–2.0	dBm
		IIP_32	f_{RFout} = 1.9 GHz Note2		–2.5	dBm
		IIP_33	f_{RFout} = 2.4 GHz Note2		–4.0	dBm
SSB Noize Figure		SSB·NF1	f_{RFout} = 0.9 GHz, f_{IFin} = 240 MHz		9.5	dB
		SSB·NF2	f_{RFout} = 1.9 GHz, f_{IFin} = 240 MHz		10.4	dB
		SSB·NF3	f_{RFout} = 2.4 GHz, f_{IFin} = 240 MHz		10.6	dB
Power Save Response Time	Rise time	$T_{PS\ (rise)}$	V_{PS} : GND → V_{CC}		1.0	μs
	Fall time	$T_{PS\ (fall)}$	V_{PS} : V_{CC} → GND		1.5	μs

Notes1. $f_{RFout} < f_{LOin}$ @ f_{RFout} = 0.9 GHz

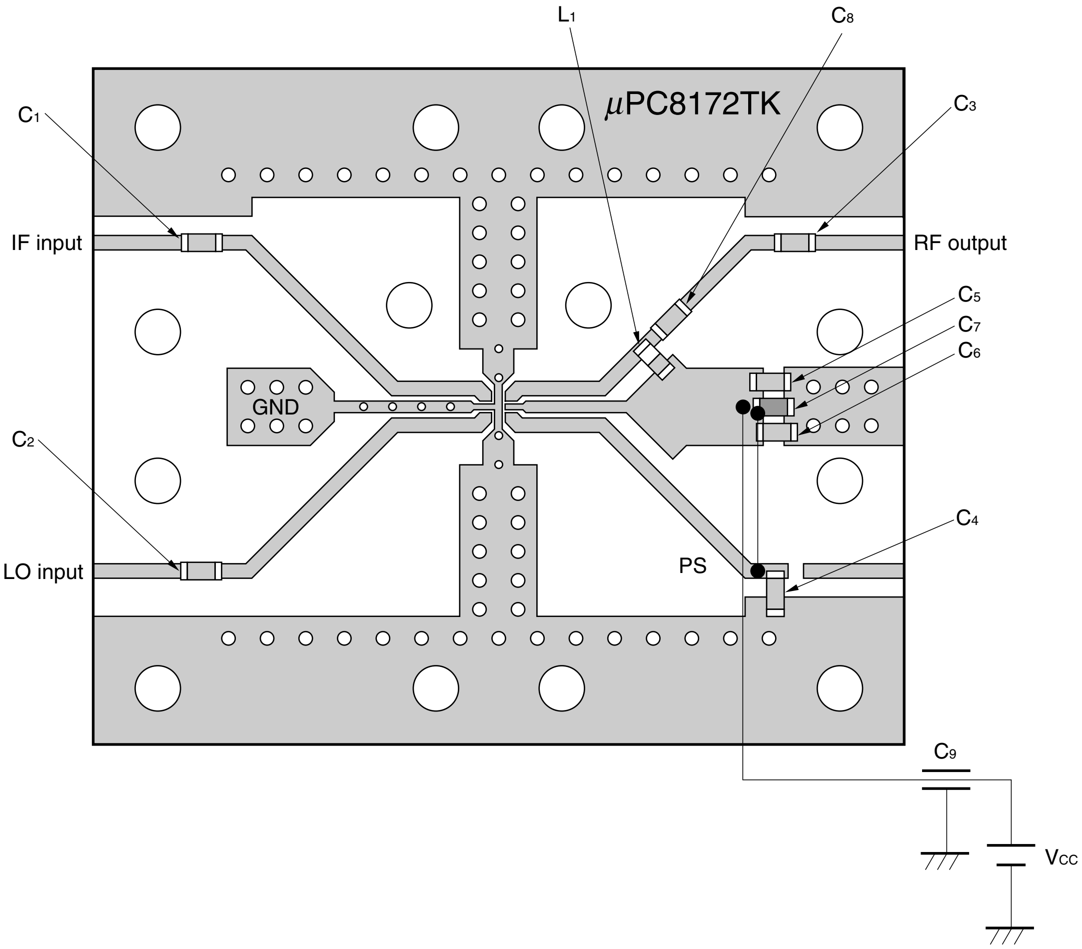
2. $f_{LOin} < f_{RFout}$ @ f_{RFout} = 1.9 GHz/2.4 GHz

★ 10. TEST CIRCUIT

10.1 TEST CIRCUIT 1 (f_{RFout} = 0.9 GHz)



EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD

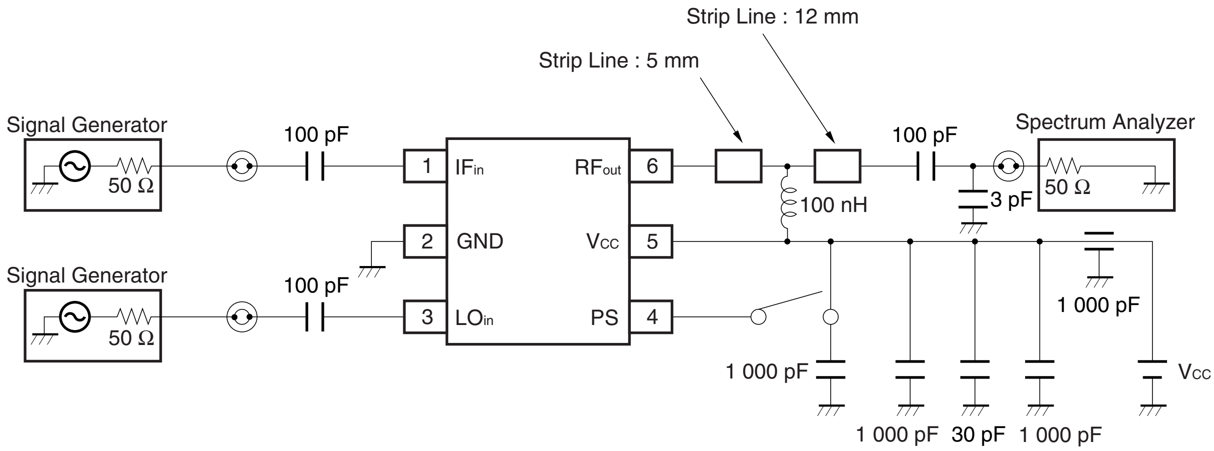


COMPONENT LIST

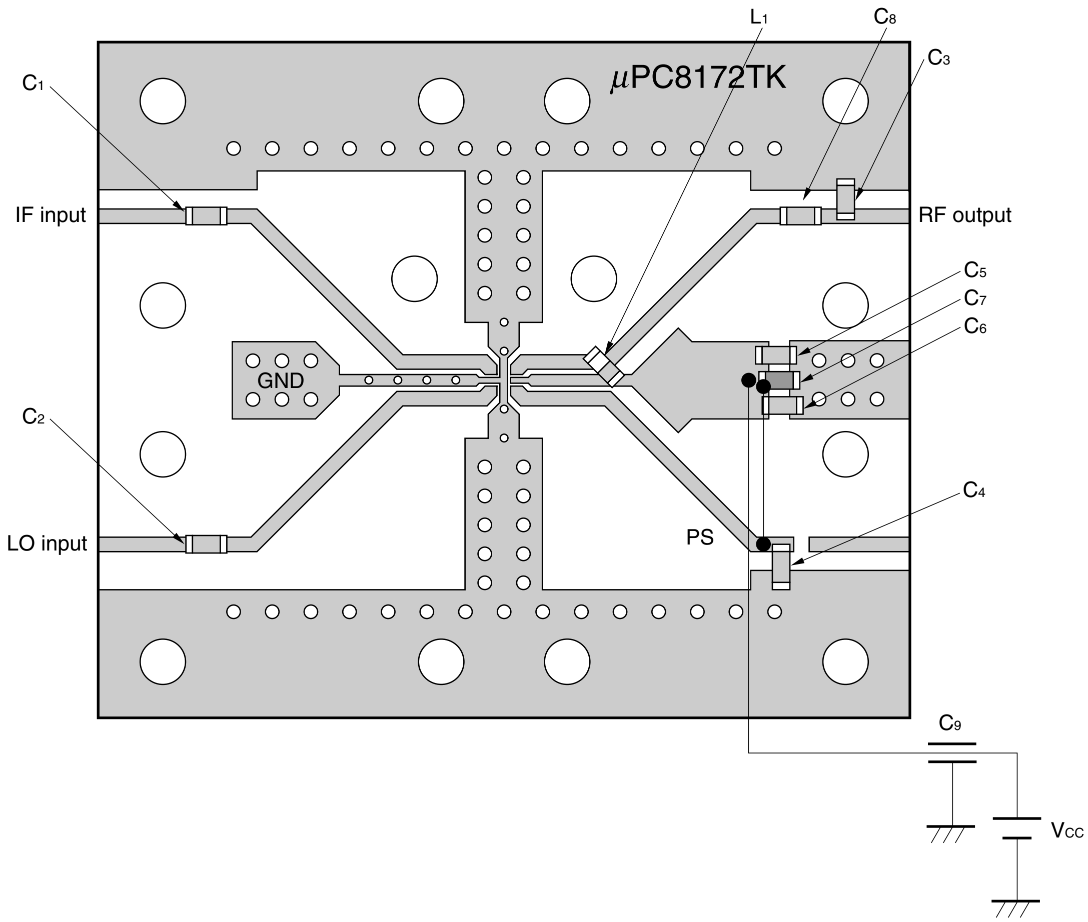
Form	Symbol	Value	Type code	Maker
Chip capacitor	C_1, C_2, C_3	100 pF	GRM39CH101J50PT	murata
	C_4	1 000 pF	GRM39B102K50PT	murata
	C_5, C_6	1 μF	GRM39F105Z10PT	murata
	C_7	68 pF	GRM39CH680J50PT	murata
	C_8	1 pF	GRM39CH010C50PT	murata
Feed-through Capacitor	C_9	1 000 pF	DFT301-801 × 7R102S50	murata
Chip inductor	L_1	10 nH	LL1608-F10N	TOKO

(∗1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
(∗2) Ground pattern on rear of the board
(∗3) Solder plated patterns
(∗4) ◦○◯: Through holes

10.2 TEST CIRCUIT 2 (f_{RFout} = 1.9 GHz)



EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD

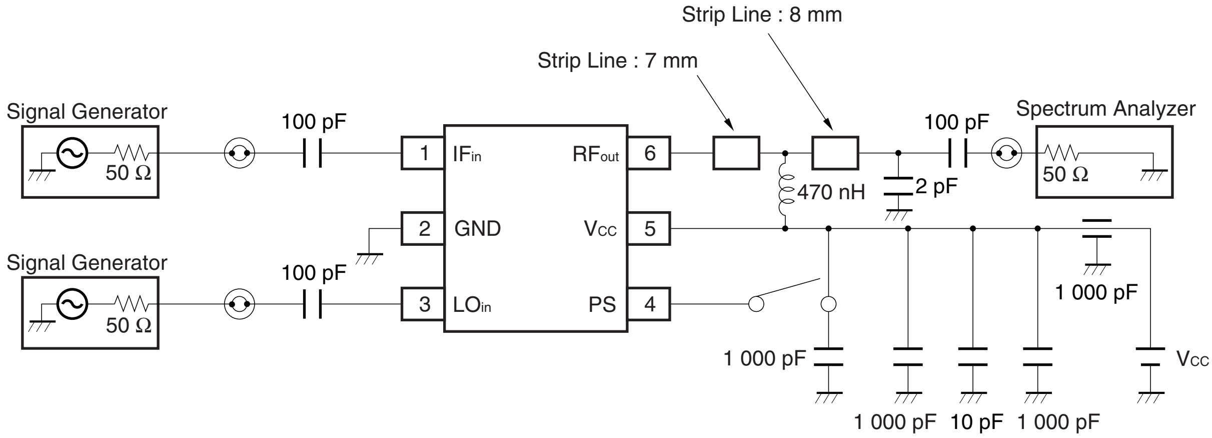


COMPONENT LIST

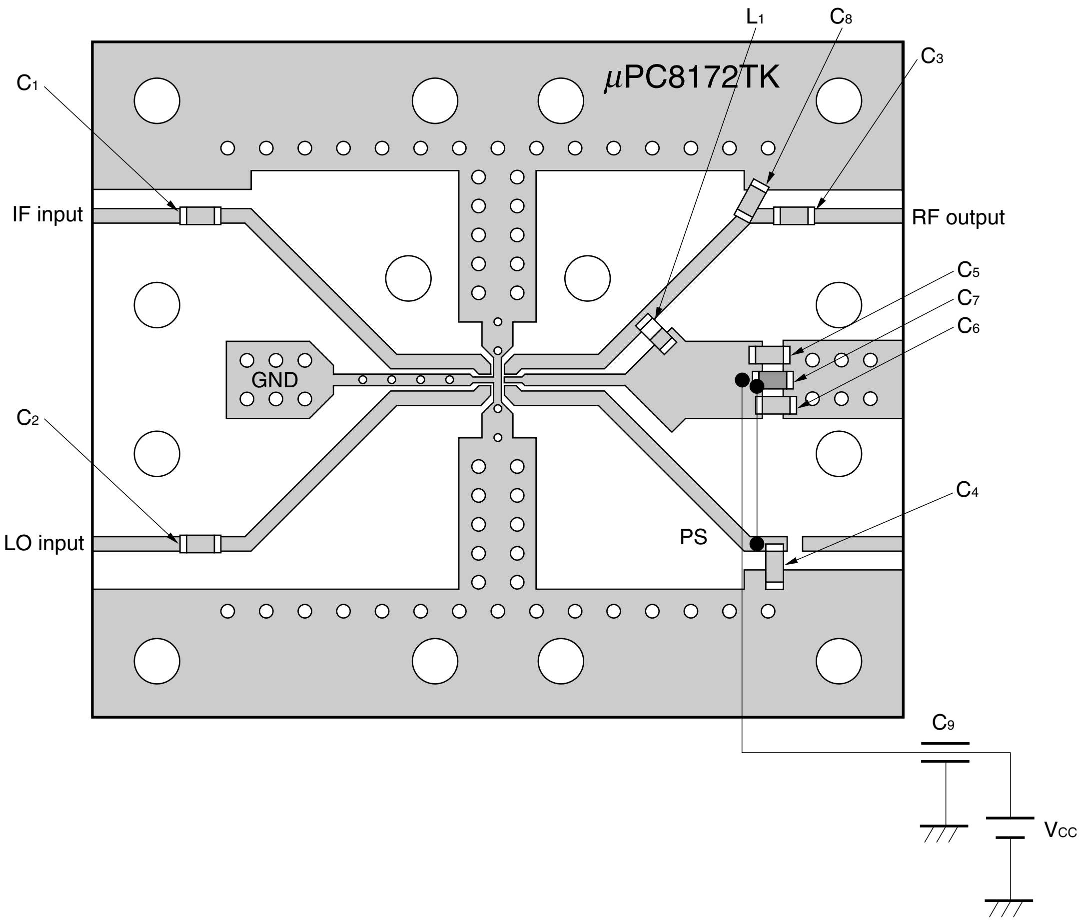
Form	Symbol	Value	Type code	Maker
Chip capacitor	C_1, C_2 ,C_3	100 pF	GRM39CH101J50PT	murata
	C_4, C_5, C_6	1 000 pF	GRM39B102K50PT	murata
	C_7	30 pF	GRM39CH300J50PT	murata
	C_8	3 pF	GRM39CH030C50PT	murata
Feed-through Capacitor	C_9	1 000 pF	DFT301-801 × 7R102S50	murata
Chip inductor	L_1	100 nH	LL1608-FR10	TOKO

(∗1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
(∗2) Ground pattern on rear of the board
(∗3) Solder plated patterns
(∗4) ∘○◯: Through holes

10.3 TEST CIRCUIT 3 (f_{RFout} = 2.4 GHz)



EXAMPLE OF TEST CIRCUIT 3 ASSEMBLED ON EVALUATION BOARD



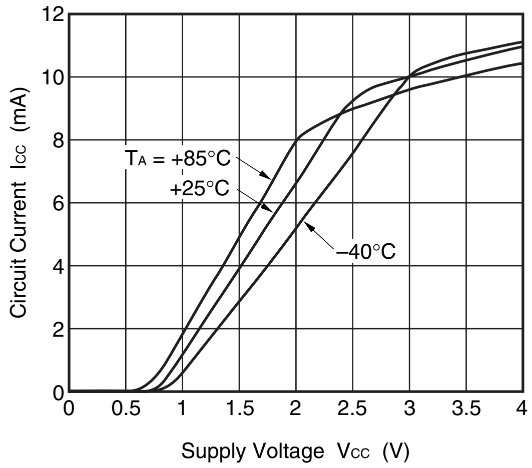
COMPONENT LIST

Form	Symbol	Value	Type code	Maker
Chip capacitor	C_1, C_2, C_3	100 pF	GRM39CH101J50PT	murata
	C_4, C_5, C_6	1 000 pF	GRM39B102K50PT	murata
	C_7	10 pF	GRM39CH100D50PT	murata
	C_8	2 pF	GRM39CH020C50PT	murata
Feed-through Capacitor	C_9	1 000 pF	DFT301-801 × 7R102S50	murata
Chip inductor	L_1	470 nH	LL2012-FR47	TOKO

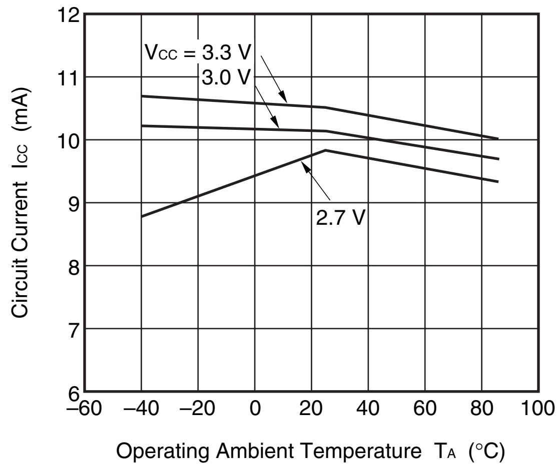
(∗1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
(∗2) Ground pattern on rear of the board
(∗3) Solder plated patterns
(∗4) ∘○◯: Through holes

★ 11. TYPICAL CHARACTERISTICS (T_A = +25°C, unless otherwise specified)

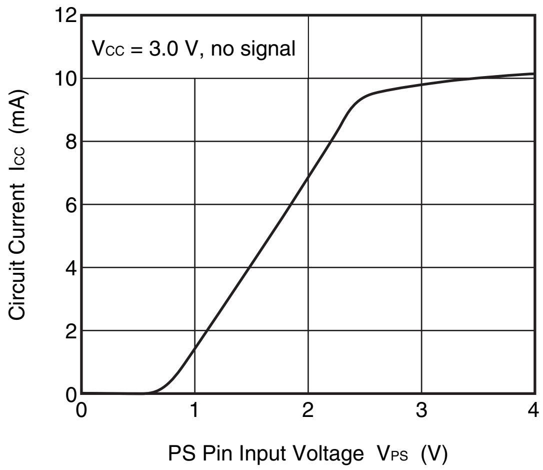
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



CIRCUIT CURRENT vs.
OPERATING AMBIENT TEMPERATURE



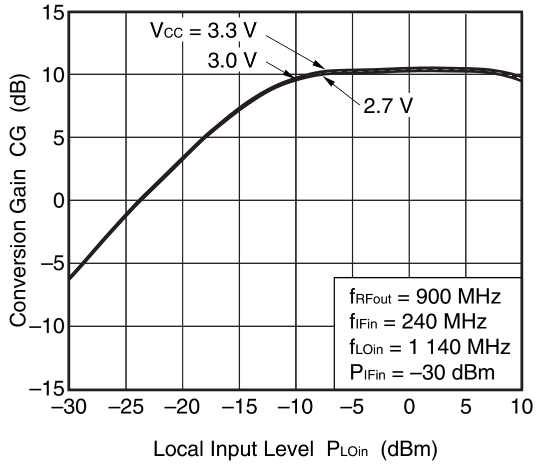
CIRCUIT CURRENT vs.
PS PIN INPUT VOLTAGE



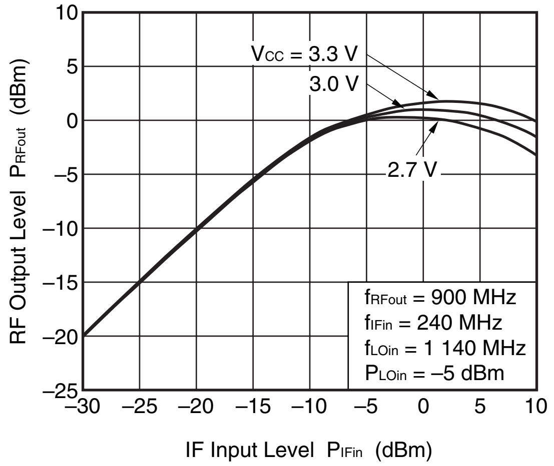
Remark The graphs indicate nominal characteristics.

11.1 f_{RFout} = 900 MHz MATCHING

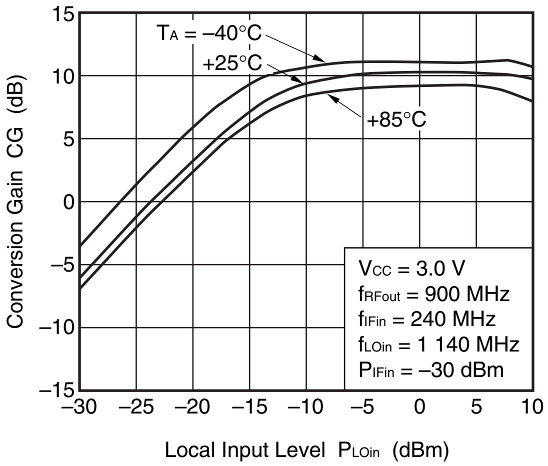
CONVERSION GAIN vs. LOCAL INPUT LEVEL



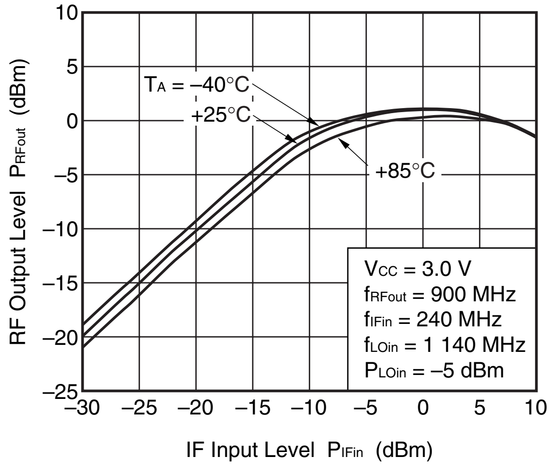
RF OUTPUT LEVEL vs. IF INPUT LEVEL



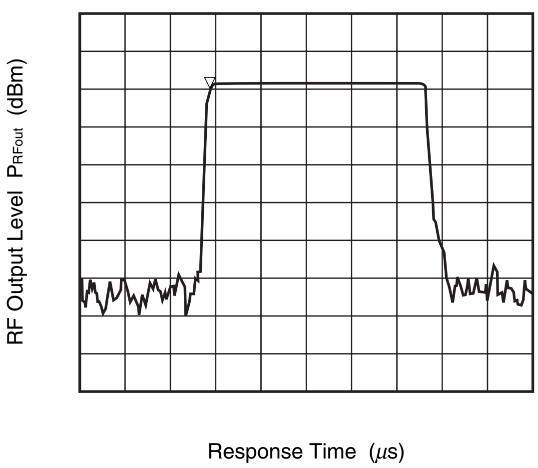
CONVERSION GAIN vs. LOCAL INPUT LEVEL



RF OUTPUT LEVEL vs. IF INPUT LEVEL



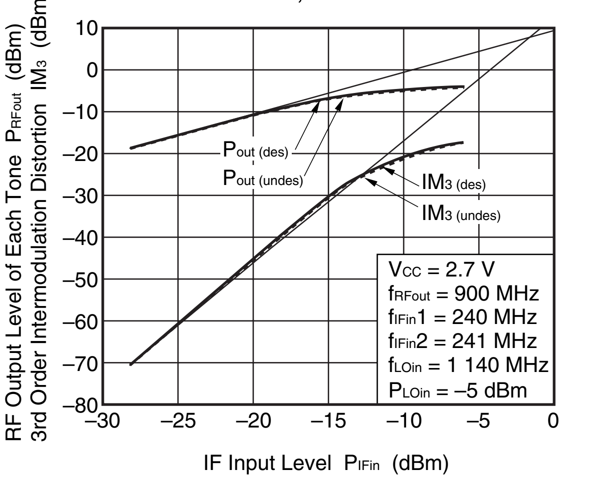
PS PIN CONTROL RESPONSE TIME



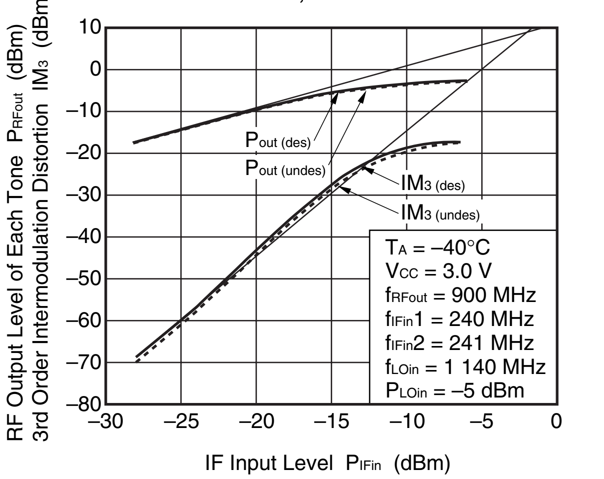
REF LVL = 0 dBm	V_{CC} = 3.0 V
10 dB/DIV (vertical axis)	f_{RFout} = 0.9 GHz
ATT = 10 dB	f_{IFin} = 240 MHz
CENTER = 0.9 GHz	P_{IFin} = –30 dBm
SPAN = 0 Hz	f_{LOin} = 1 140 MHz
RBW = 2 MHz	P_{LOin} = –5 dBm
VBW = 3 MHz	ΔMKR –20.0 dBm,14.7 μs
SWP = 50 μsec	
5 μsec/DIN (horizontal axis)	

Remark The graphs indicate nominal characteristics.

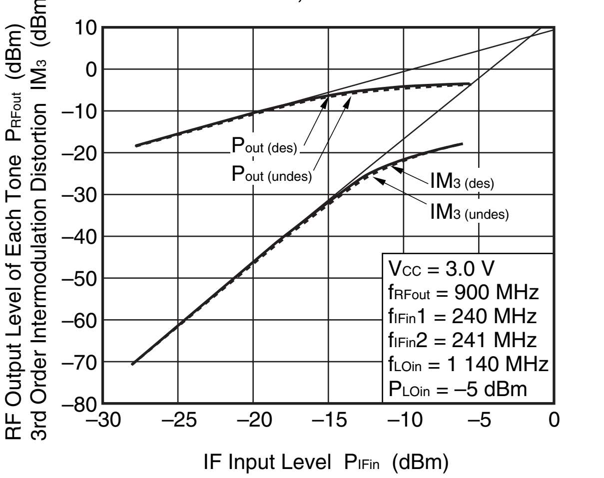
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL



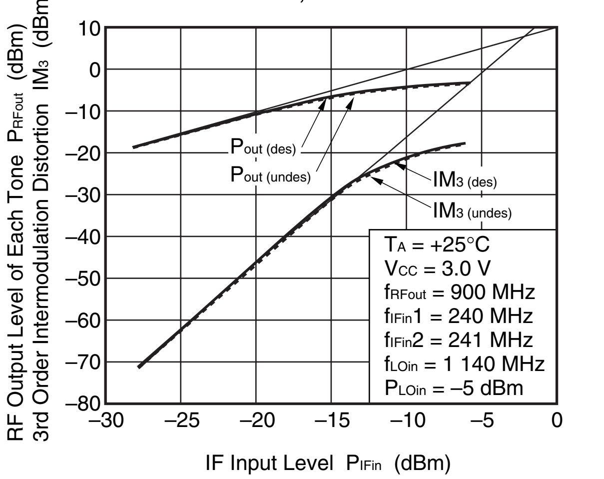
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL



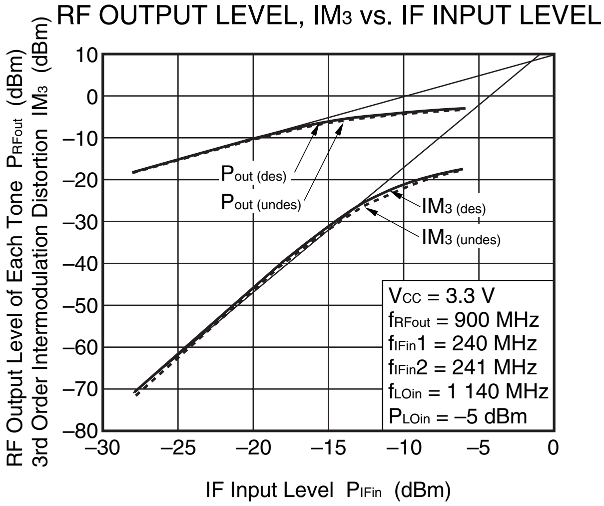
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL



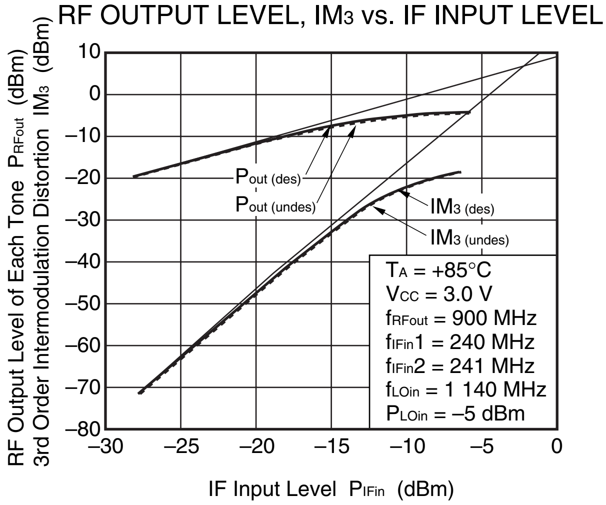
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL



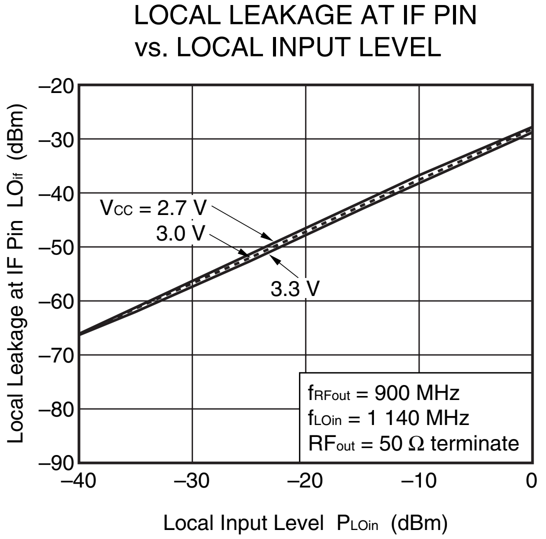
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL

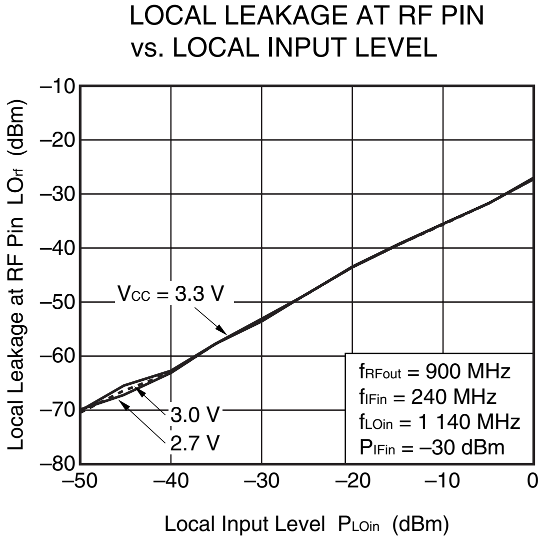


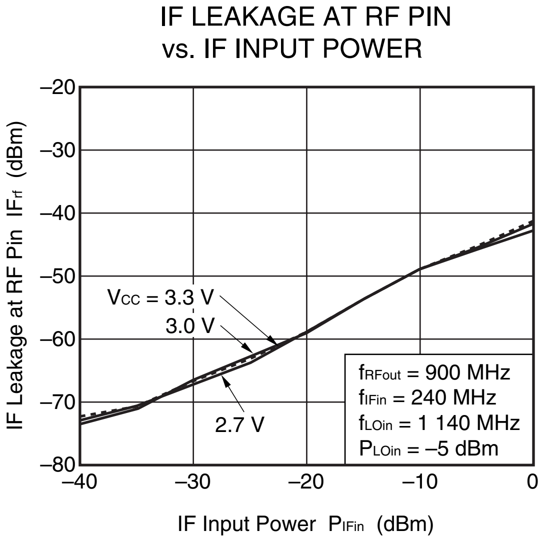
RF OUTPUT LEVEL, IM_3 vs. IF INPUT LEVEL

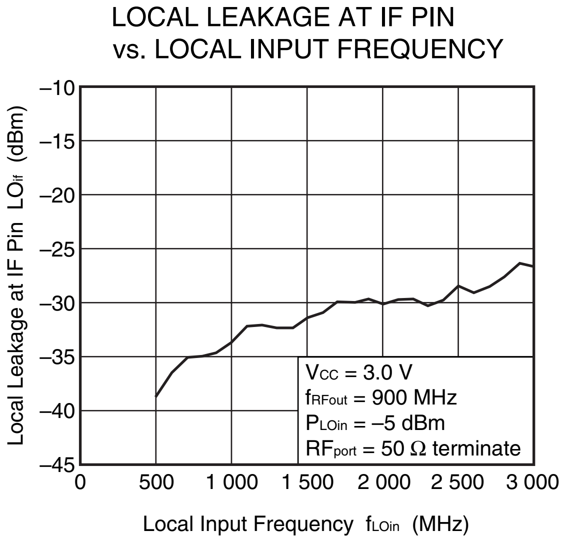


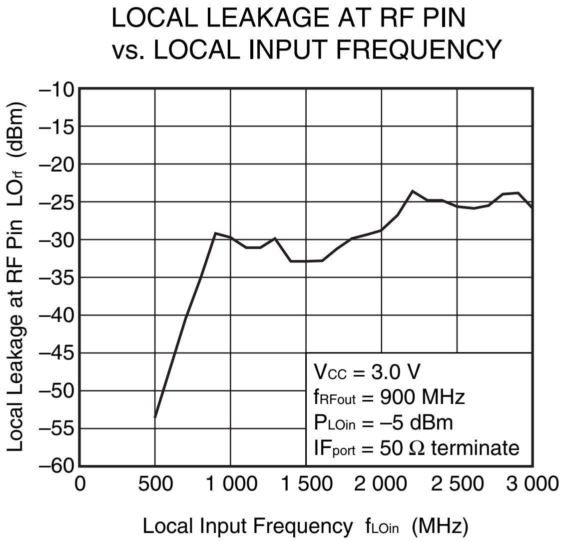
Remark The graphs indicate nominal characteristics.

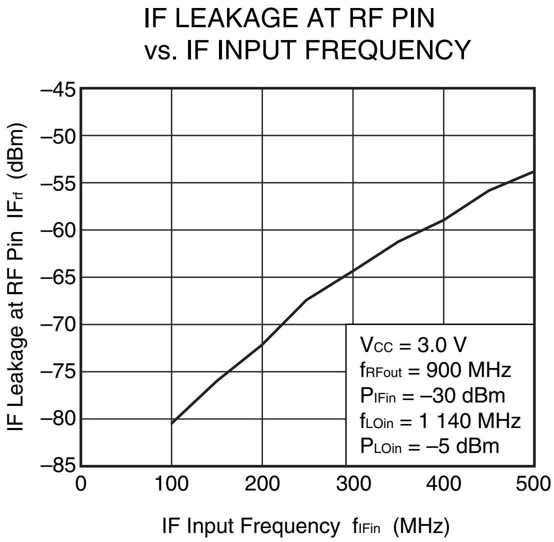






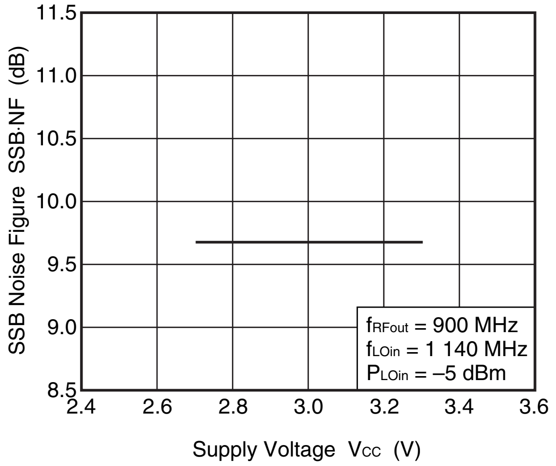




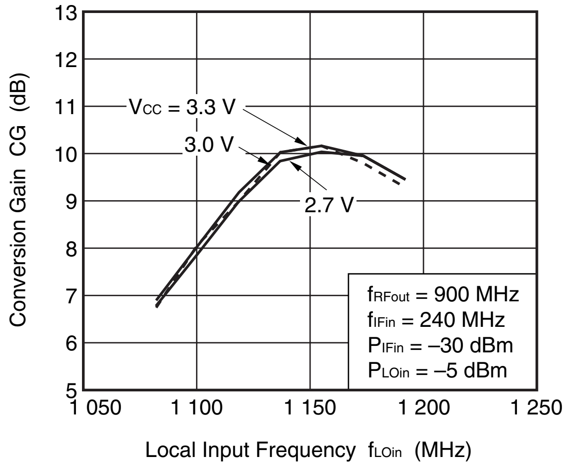


Remark The graphs indicate nominal characteristics.

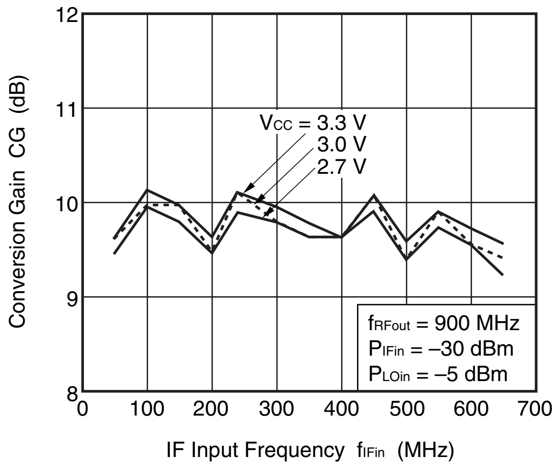
SSB NOISE FIGURE vs. SUPPLY VOLTAGE



CONVERSION GAIN vs.
LOCAL INPUT FREQUENCY



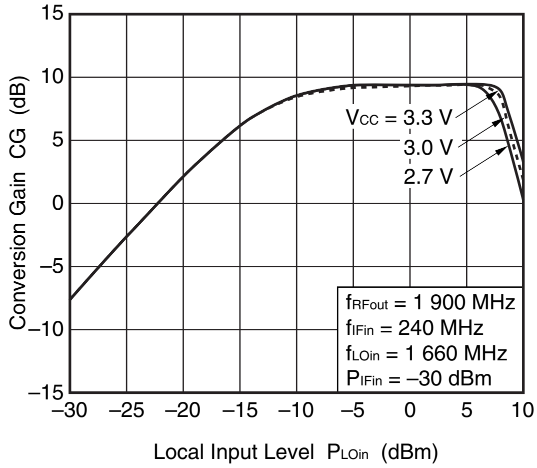
CONVERSION GAIN vs.
IF INPUT FREQUENCY



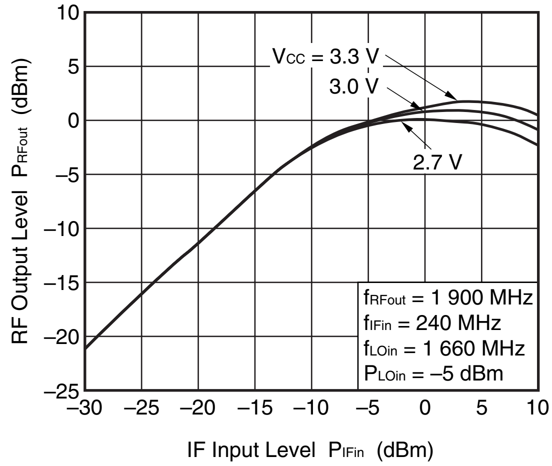
Remark The graphs indicate nominal characteristics.

11.2 f_{RFout} = 1 900 MHz MATCHING

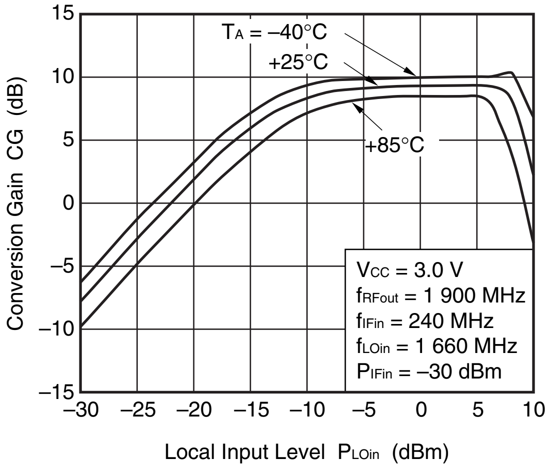
CONVERSION GAIN vs. LOCAL INPUT LEVEL



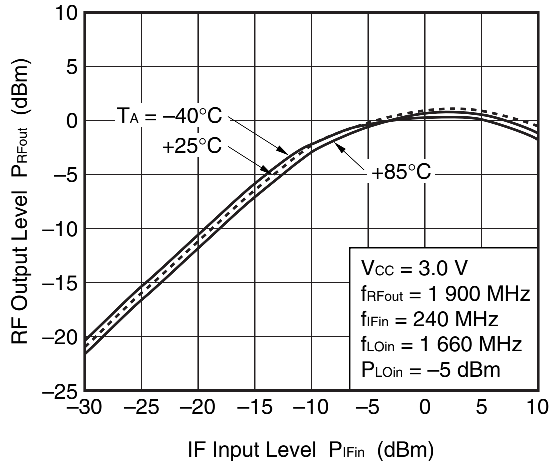
RF OUTPUT LEVEL vs. IF INPUT LEVEL



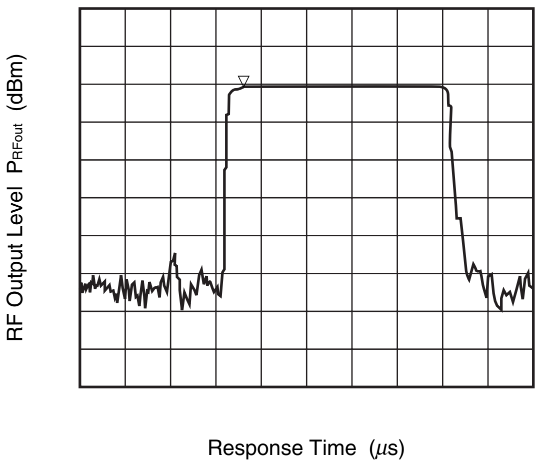
CONVERSION GAIN vs. LOCAL INPUT LEVEL



RF OUTPUT LEVEL vs. IF INPUT LEVEL

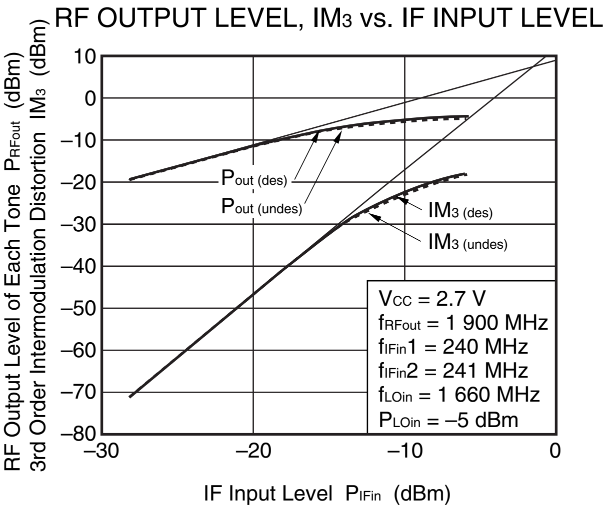


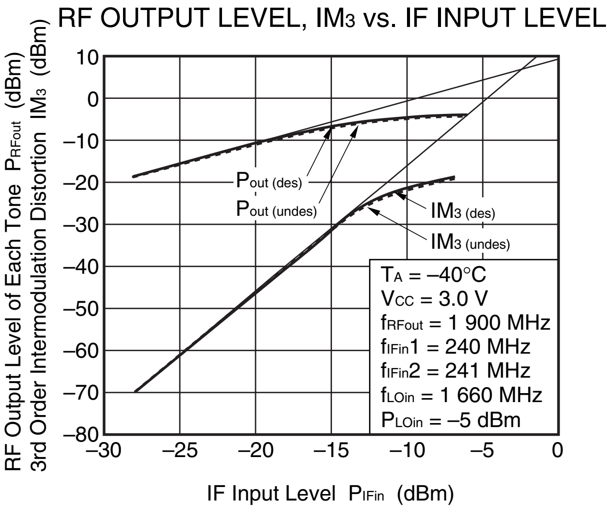
PS PIN CONTROL RESPONSE TIME

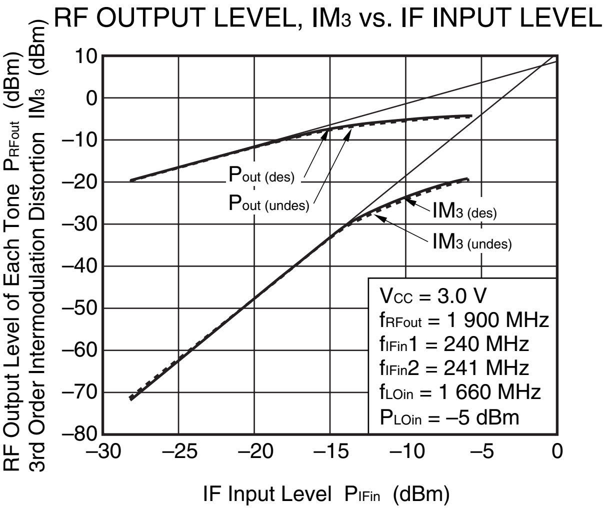


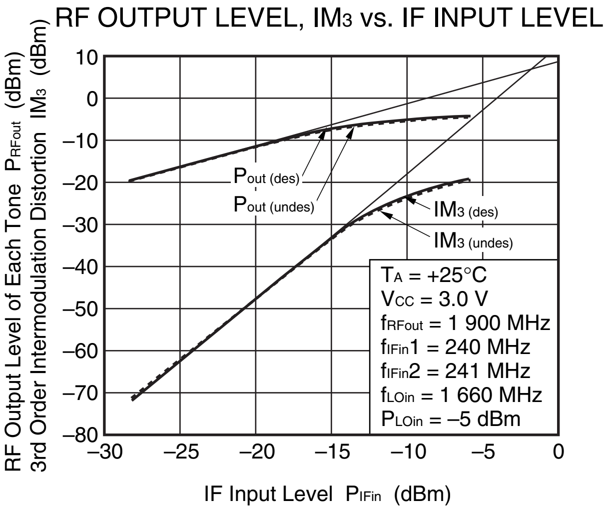
REF LVL = 0 dBm	V_{CC} = 3.0 V
10 dB/DIV (vertical axis)	f_{RFout} = 1.9 GHz
ATT = 10 dB	f_{IFin} = 240 MHz
CENTER = 1.9 GHz	P_{IFin} = –30 dBm
SPAN = 0 Hz	f_{LOin} = 1 660 MHz
RBW = 2 MHz	P_{LOin} = –5 dBm
VBW = 3 MHz	ΔMKR –21.0 dBm,17.9 μs
SWP = 50 μsec	
5 μsec/DIN (horizontal axis)	

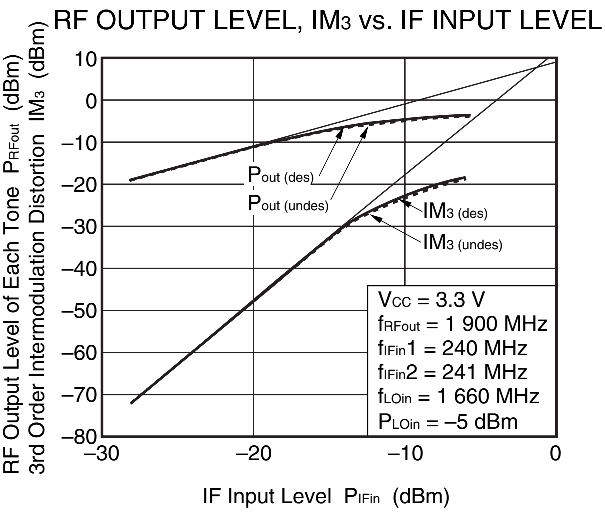
Remark The graphs indicate nominal characteristics.

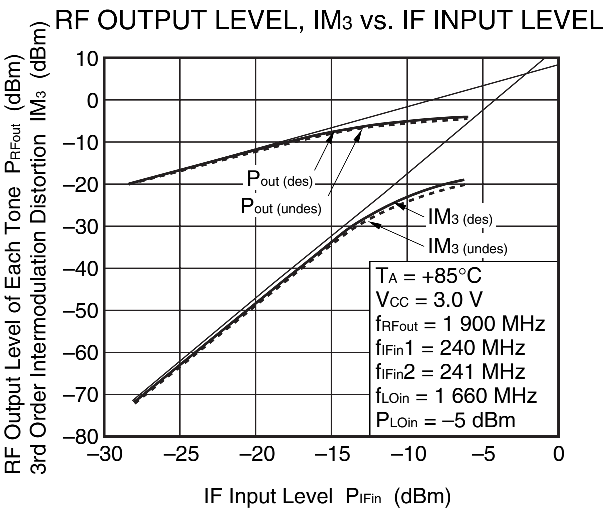






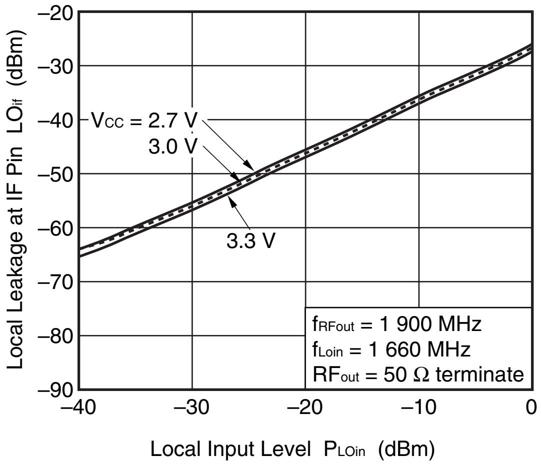




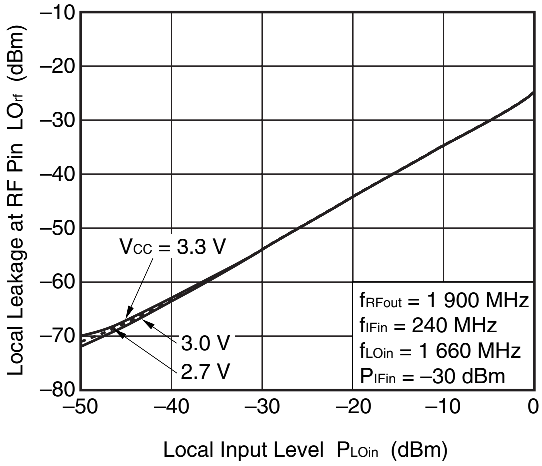


Remark The graphs indicate nominal characteristics.

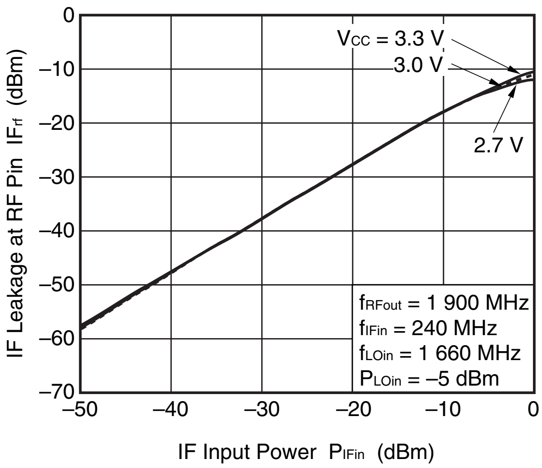
LOCAL LEAKAGE AT IF PIN
vs. LOCAL INPUT LEVEL



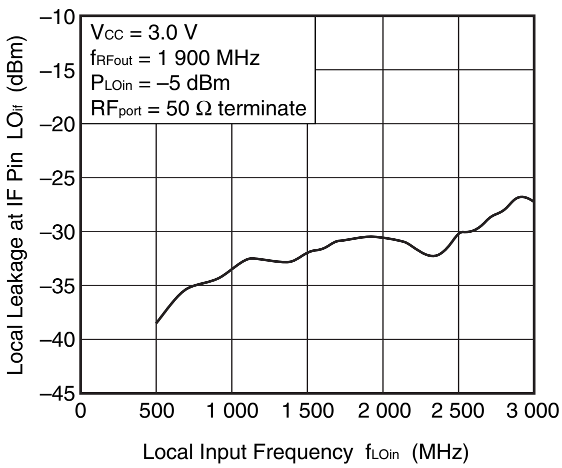
LOCAL LEAKAGE AT RF PIN
vs. LOCAL INPUT LEVEL



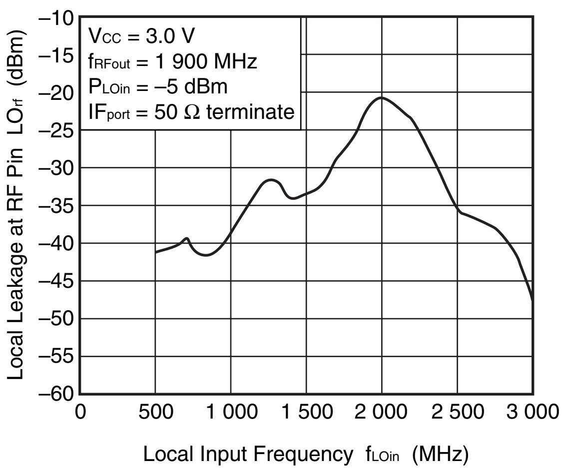
IF LEAKAGE AT RF PIN
vs. IF INPUT POWER



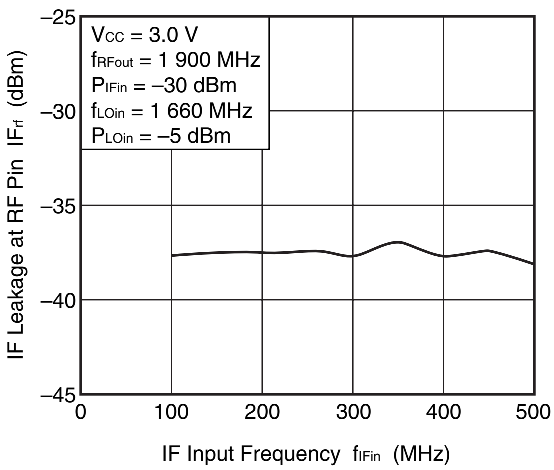
LOCAL LEAKAGE AT IF PIN
vs. LOCAL INPUT FREQUENCY



LOCAL LEAKAGE AT RF PIN
vs. LOCAL INPUT FREQUENCY

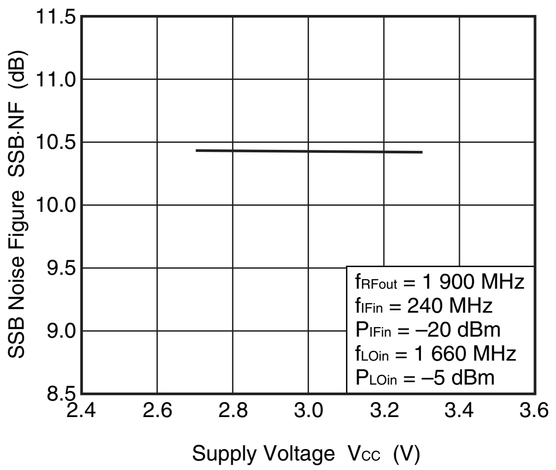


IF LEAKAGE AT RF PIN
vs. IF INPUT FREQUENCY

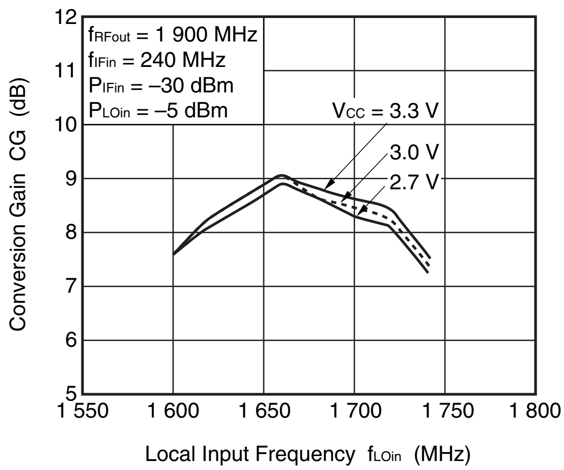


Remark The graphs indicate nominal characteristics.

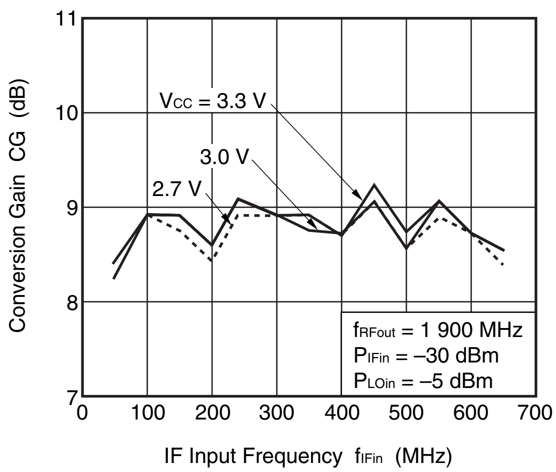
SSB NOISE FIGURE vs. SUPPLY VOLTAGE



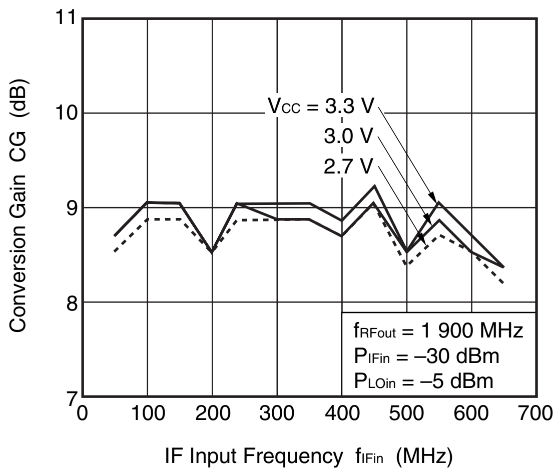
CONVERSION GAIN vs. LOCAL INPUT FREQUENCY



CONVERSION GAIN vs. IF INPUT FREQUENCY ($f_{LOin} < f_{RFout}$)



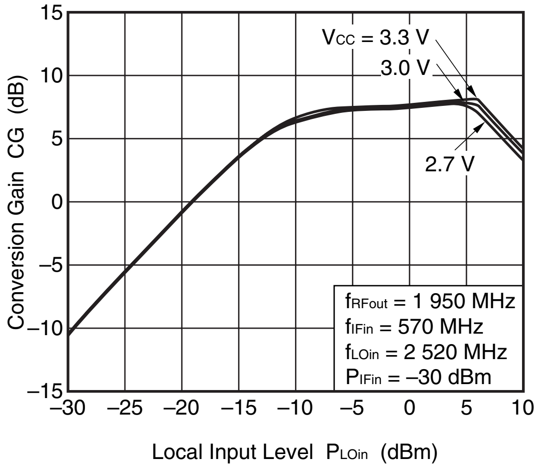
CONVERSION GAIN vs. IF INPUT FREQUENCY ($f_{LOin} > f_{RFout}$)



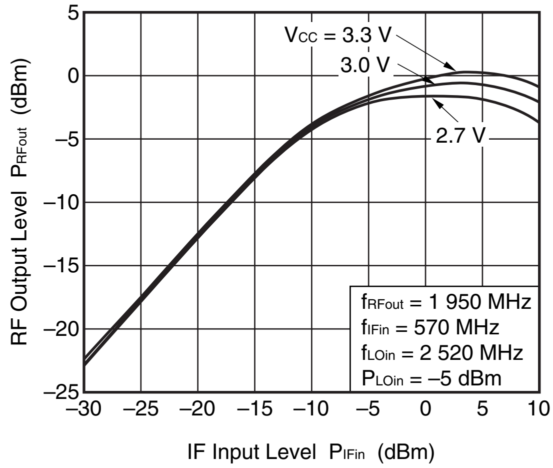
Remark The graphs indicate nominal characteristics.

11.3 f_{RFout} = 1 950 MHz MATCHING

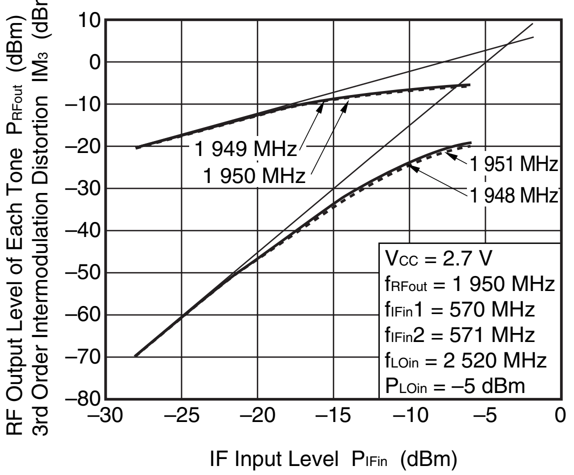
CONVERSION GAIN vs. LOCAL INPUT LEVEL



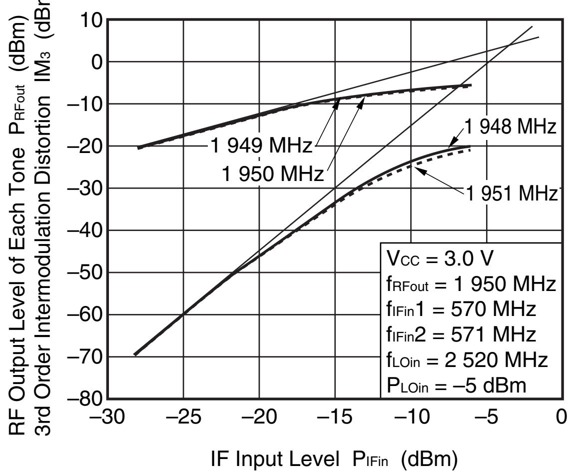
RF OUTPUT LEVEL vs. IF INPUT LEVEL



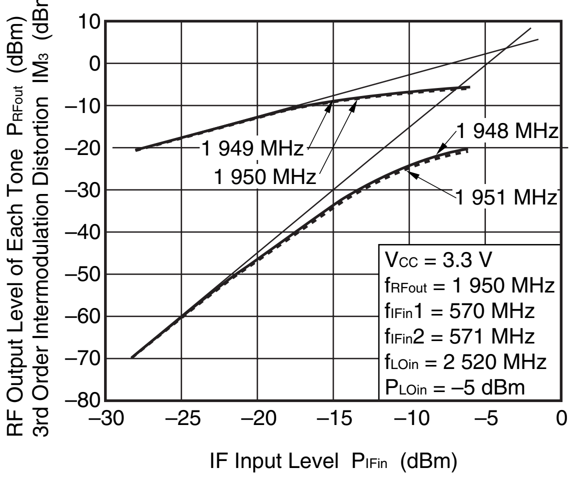
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



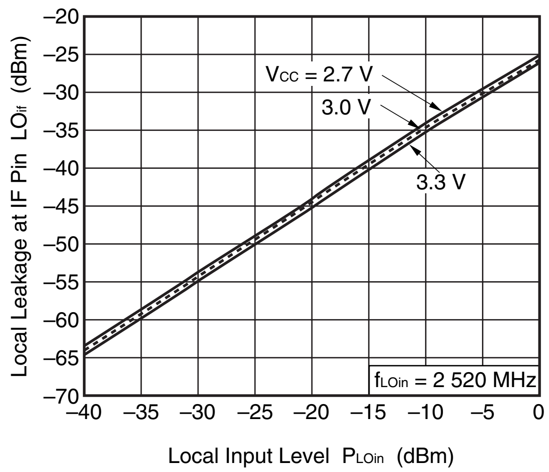
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL

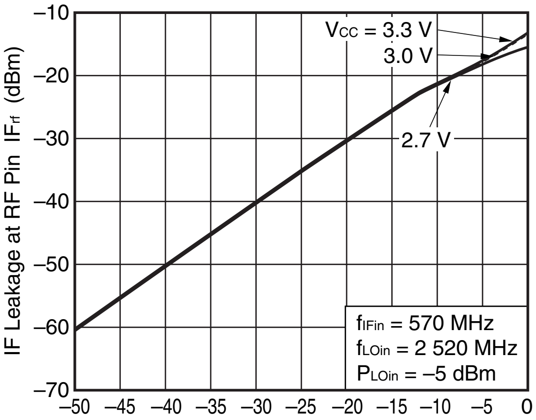


LOCAL LEAKAGE AT IF PIN
vs. LOCAL INPUT LEVEL

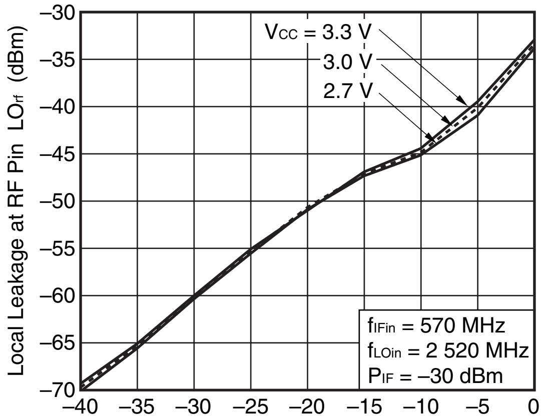


Remark The graphs indicate nominal characteristics.

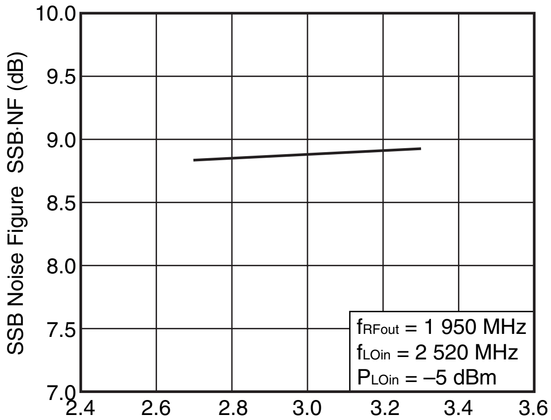
IF LEAKAGE AT RF PIN vs. IF INPUT POWER



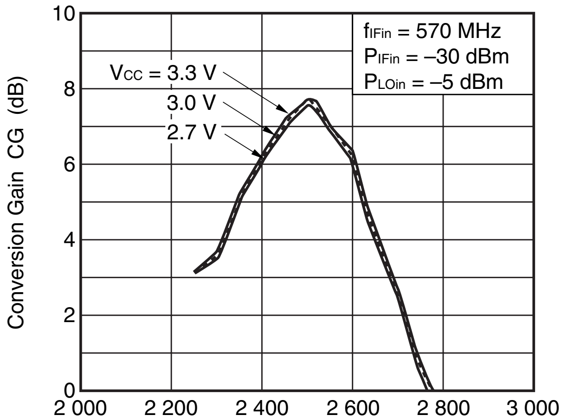
LOCAL LEAKAGE AT RF PIN vs. LOCAL INPUT LEVEL



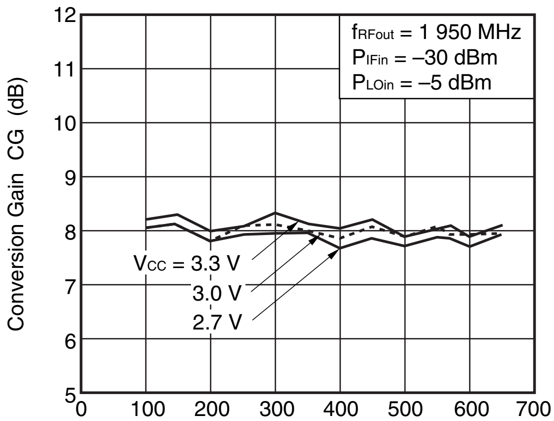
SSB NOISE FIGURE vs. SUPPLY VOLTAGE



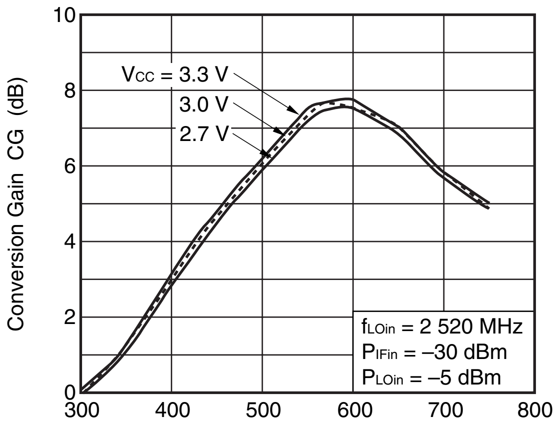
CONVERSION GAIN vs. LOCAL INPUT FREQUENCY



CONVERSION GAIN vs. IF INPUT FREQUENCY



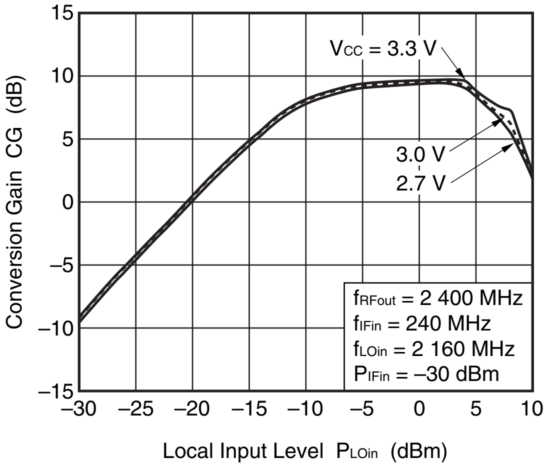
CONVERSION GAIN vs. IF INPUT FREQUENCY



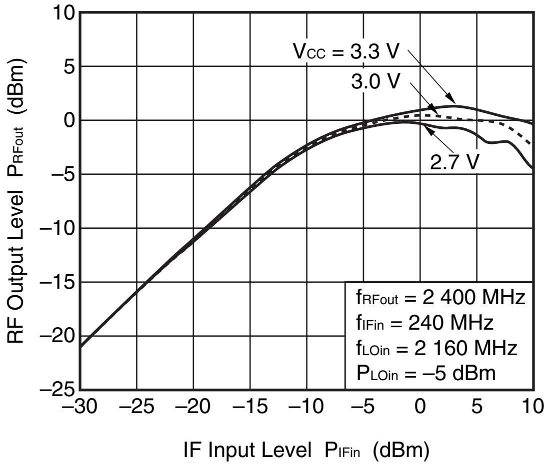
Remark The graphs indicate nominal characteristics.

11.4 f_{RFout} = 2 400 MHz MATCHING

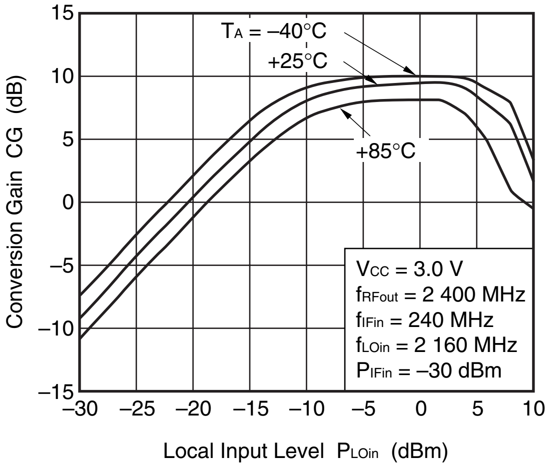
CONVERSION GAIN vs. LOCAL INPUT LEVEL



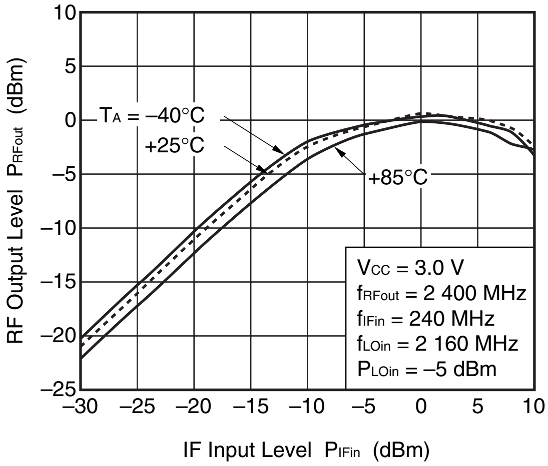
RF OUTPUT LEVEL vs. IF INPUT LEVEL



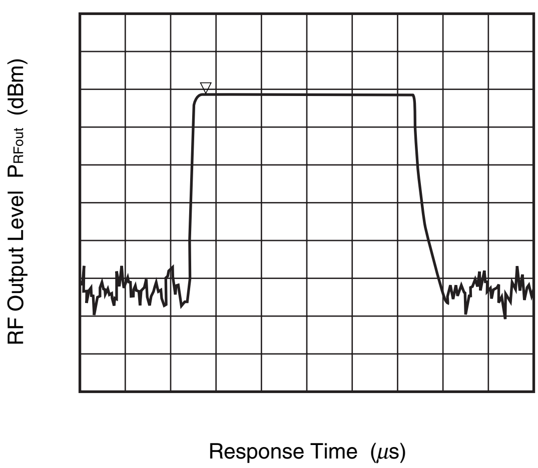
CONVERSION GAIN vs. LOCAL INPUT LEVEL



RF OUTPUT LEVEL vs. IF INPUT LEVEL



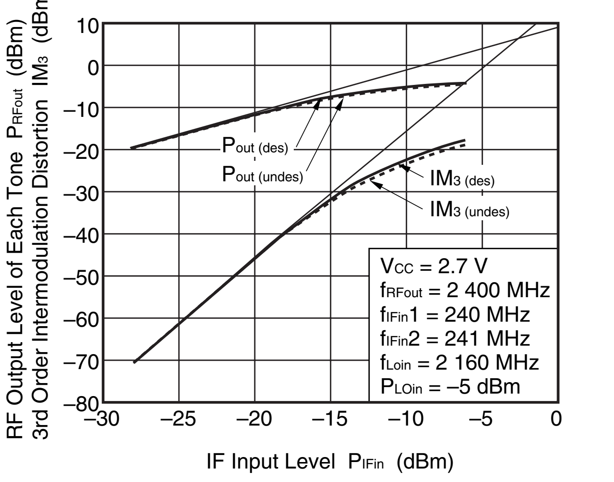
PS PIN CONTROL RESPONSE TIME



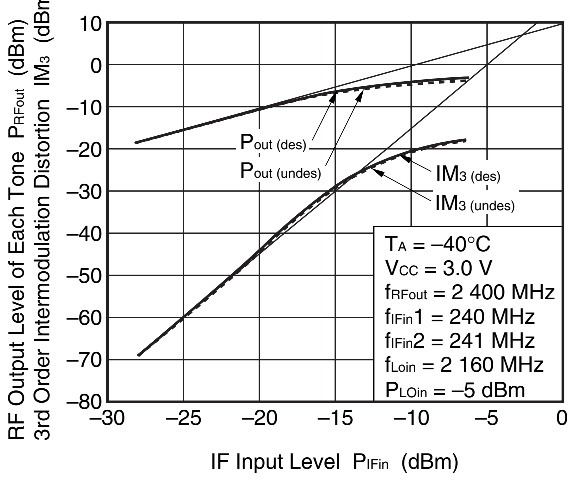
REF LVL = 0 dBm	V_{CC} = 3.0 V
10 dB/DIV (vertical axis)	f_{RFout} = 2.4 GHz
ATT = 10 dB	f_{IFin} = 240 MHz
CENTER = 2.4 GHz	P_{IFin} = –30 dBm
SPAN = 0 Hz	f_{LOin} = 2 160 MHz
RBW = 2 MHz	P_{LOin} = –5 dBm
VBW = 3 MHz	ΔMKR –21.5 dBm,13.8 μs
SWP = 50 μsec	
5 μsec/DIN (horizontal axis)	

Remark The graphs indicate nominal characteristics.

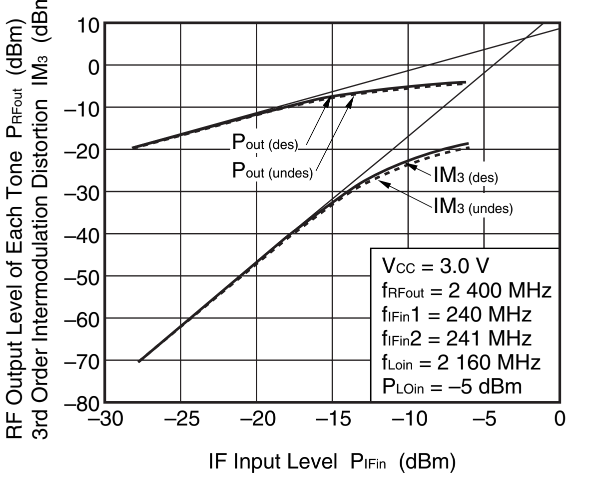
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



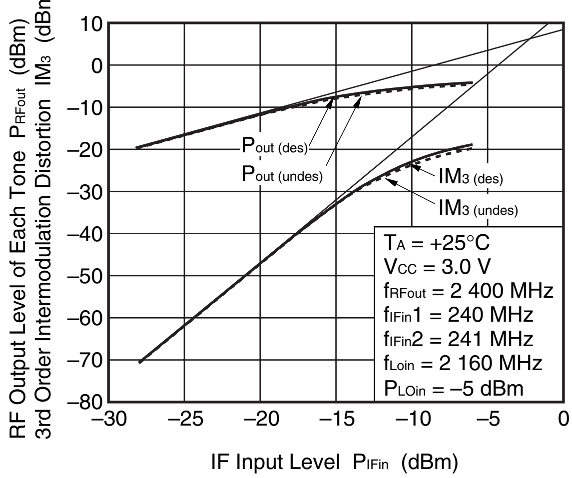
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



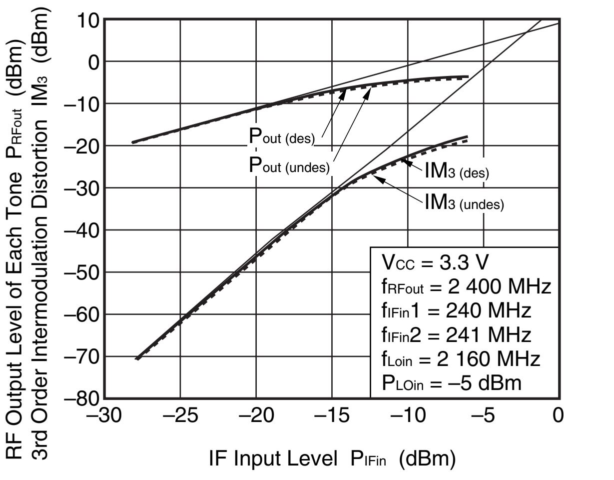
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



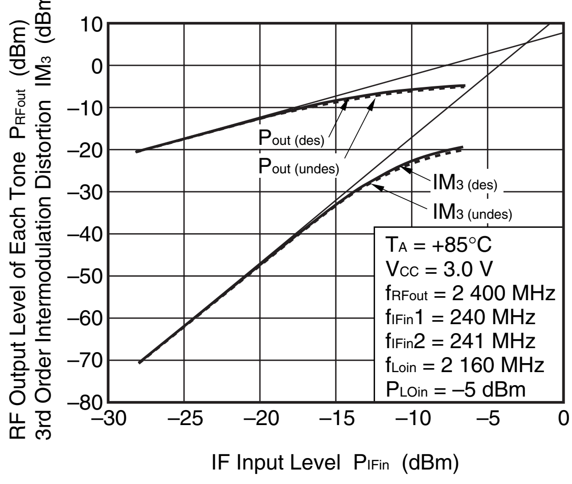
RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL



RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL

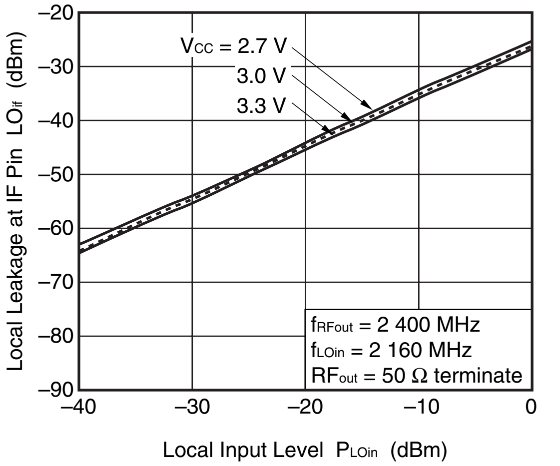


RF OUTPUT LEVEL, IM3 vs. IF INPUT LEVEL

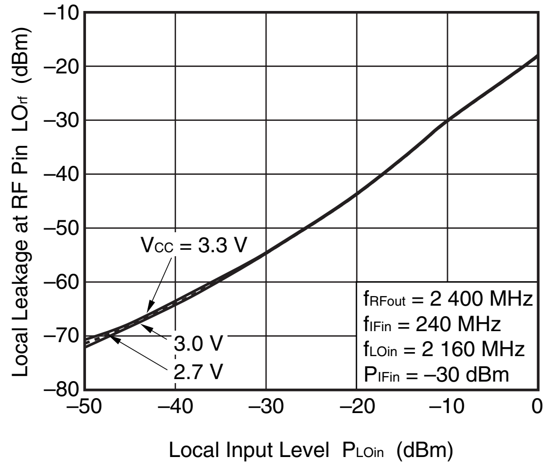


Remark The graphs indicate nominal characteristics.

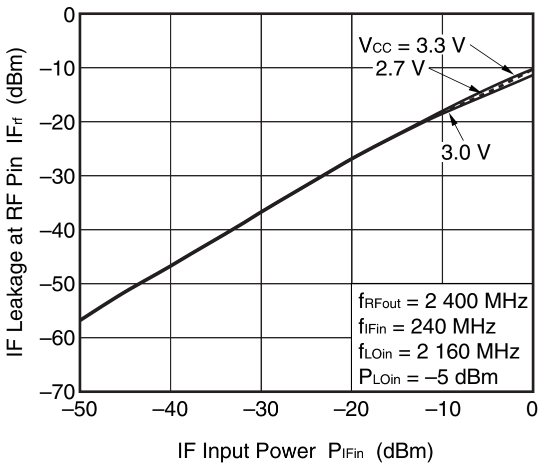
LOCAL LEAKAGE AT IF PIN
vs. LOCAL INPUT LEVEL



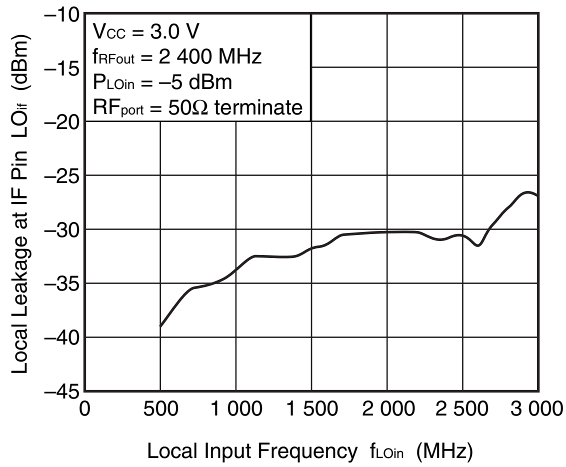
LOCAL LEAKAGE AT RF PIN
vs. LOCAL INPUT LEVEL



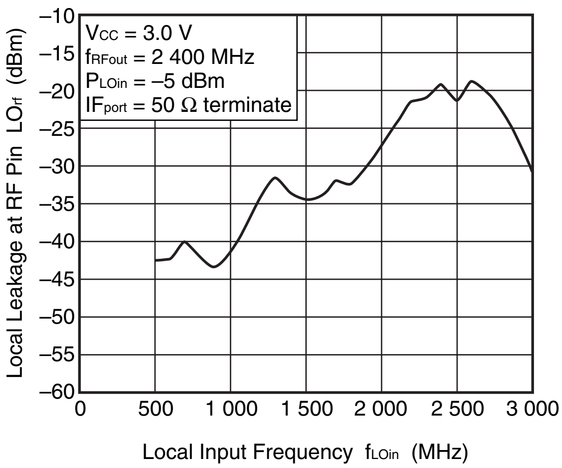
IF LEAKAGE AT RF PIN
vs. IF INPUT POWER



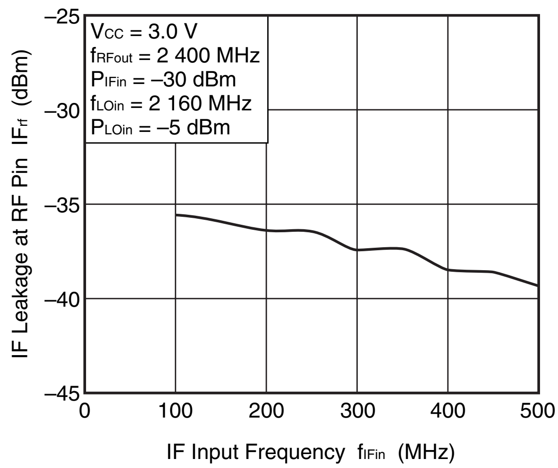
LOCAL LEAKAGE AT IF PIN
vs. LOCAL INPUT FREQUENCY



LOCAL LEAKAGE AT RF PIN
vs. LOCAL INPUT FREQUENCY

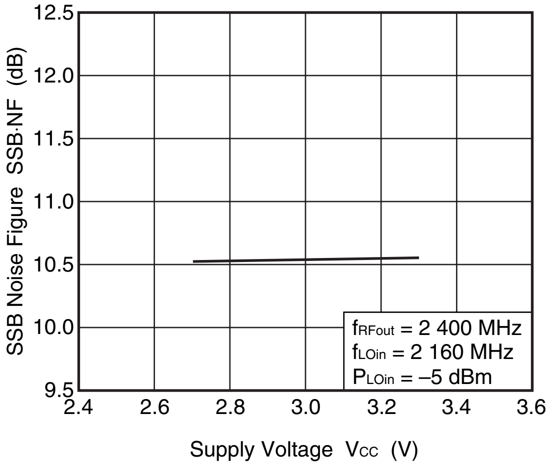


IF LEAKAGE AT RF PIN
vs. IF INPUT FREQUENCY

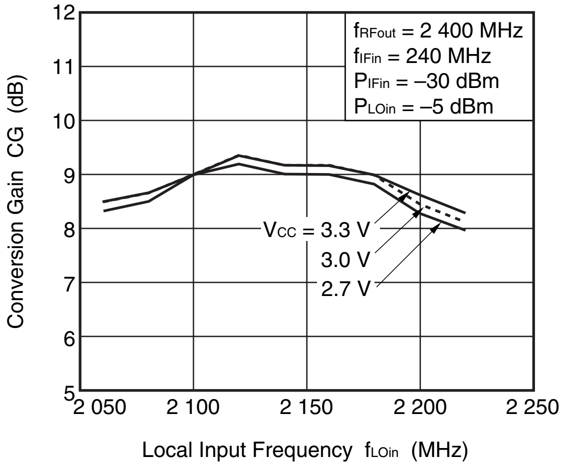


Remark The graphs indicate nominal characteristics.

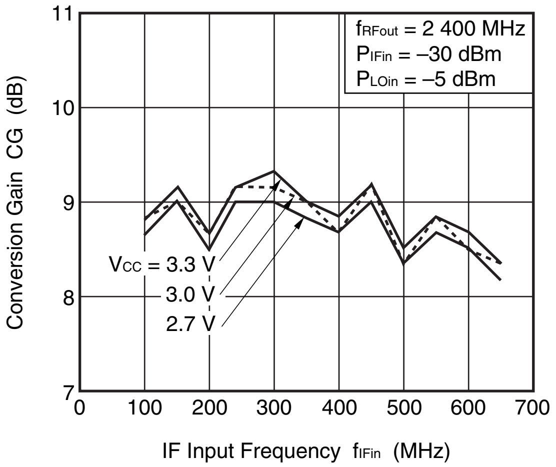
SSB NOISE FIGURE vs. SUPPLY VOLTAGE



CONVERSION GAIN vs.
LOCAL INPUT FREQUENCY



CONVERSION GAIN vs.
IF INPUT FREQUENCY



Remark The graphs indicate nominal characteristics.

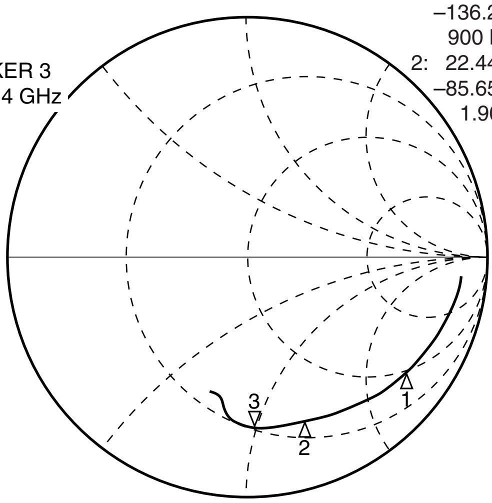
★ 12. S-PARAMETERS

LO port Inpedance (at L loaded)

CH1 B_{11} 1 U FB B : 17.816 Ω –49.146 Ω 1.3493 pF
2 400.000 000 MHz

1: 45.734 Ω
–136.26 Ω
900 MHz
2: 22.445 Ω
–85.655 Ω
1.90 Hz

MARKER 3
2.4 GHz



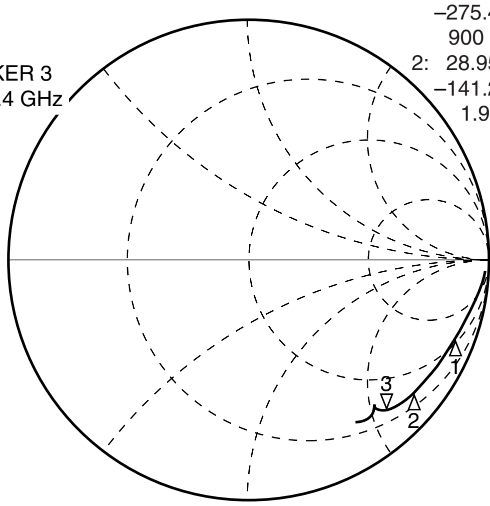
START 100.000 000 MHz
STOP 3 100.000 000 MHz

RF port Inpedance (at L loaded)

CH1 B_{22} 1 U FB B : 22.96 Ω –107.45 Ω 617.19 fF
2 400.000 000 MHz

1: 63.672 Ω
–275.47 Ω
900 MHz
2: 28.953 Ω
–141.21 Ω
1.90 Hz

MARKER 3
2.4 GHz



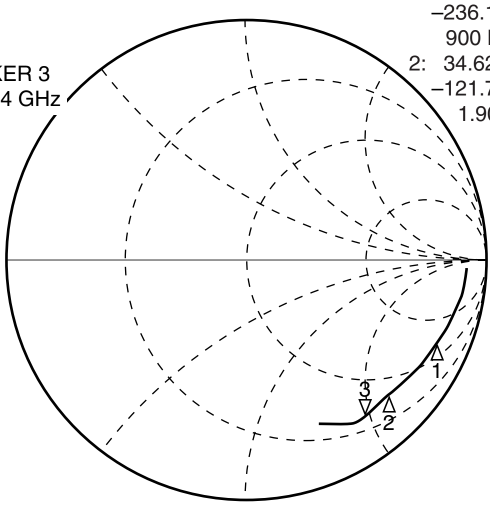
START 100.000 000 MHz
STOP 3 100.000 000 MHz

IF port Inpedance (at L loaded)

CH1 B_{11} 1 U FB B : 25.383 Ω –96.613 Ω 672.47 fF
2 400.000 000 MHz

1: 66.539 Ω
–236.11 Ω
900 MHz
2: 34.626 Ω
–121.79 Ω
1.90 Hz

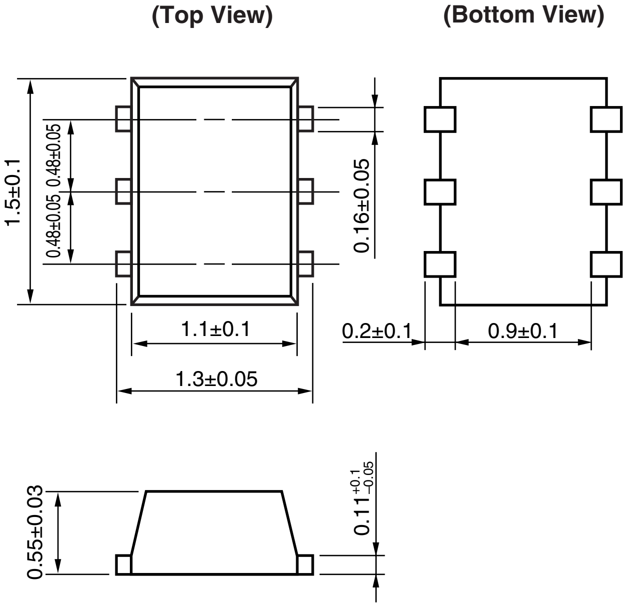
MARKER 3
2.4 GHz



START 100.000 000 MHz
STOP 3 100.000 000 MHz

★ 13. PACKAGE DIMENSIONS

6-PIN LEAD-LESS MINIMOLD (1511) (UNIT: mm)



Remark ( ) : Reference value

14. NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Connect a bypass capacitor (example : 1 000 pF) to the V_{CC} pin.
(4) Connect a matching circuit to the RF output pin.
(5) The DC cut capacitor must be attached to input and output pin.

15. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (terminal temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350

Caution Do not use different soldering methods together (except for partial heating).

When the product(s) listed in this document is subject to any applicable import or export control laws and regulation of the authority having competent jurisdiction, such product(s) shall not be imported or exported without obtaining the import or export license.

▶For further information, please contact

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