4 X 4 REGISTER FILE WITH 3-STATE OUTPUTS

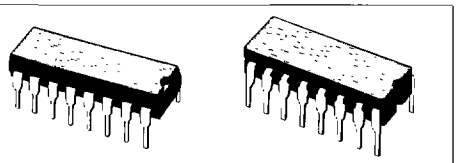
- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BIT
- TYPICAL ACCESS TIME OF 20 ns
- 3-STATE OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW

DESCRIPTION

The TTL/MSI T74LS670 is a high speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-State outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these device can be operated in parallel to generate an n-bit lenght.

The T74LS170 provides a simular function to this device but is features open-collector outputs.



B1
(Plastic Package)

D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

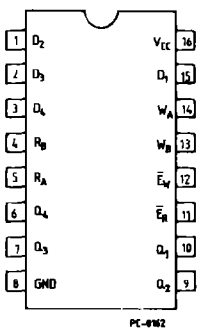
T74LS670 D1
T74LS670 B1
T74LS670 C1
T74LS670 M1

PIN NAMES

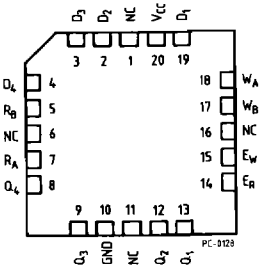
D_1-D_4	DATA INPUTS
$\overline{W}_A$, W_B	WRITE ADDRESS INPUTS
$\overline{E}_W$	WRITE ENABLE (active LOW) INPUT
$\overline{R}_A$, R_B	READ ADDRESS INPUTS
$\overline{E}_R$	READ ENABLE (active LOW) INPUT
Q_1-Q_4	OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

WRITE FUNCTION TABLE AND READ FUNCTION TABLE

(see notes A, B and C)

Write Inputs			Word			
WB	WA	EW	0	1	2	3
L	L	L	Q = D	00	00	00
L	H	L	00	Q = D	00	00
H	L	L	00	00	Q = D	00
H	H	L	00	00	00	Q = D
X	X	H	00	00	00	00

(see notes A, and D)

Read Inputs			Outputs			
RB	RA	ER	01	02	03	04
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes : A. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance
B. Q = D = The four selected internal flip-flops will assume the state applied to the 4 external data inputs.
C. 00 = The level of 0 before the indicated input conditions were established.
D. W0B1 = The first bit word 0, etc

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 50 to 5	mA
I_O	Output Current, into Outputs	50	mA

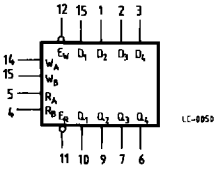
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

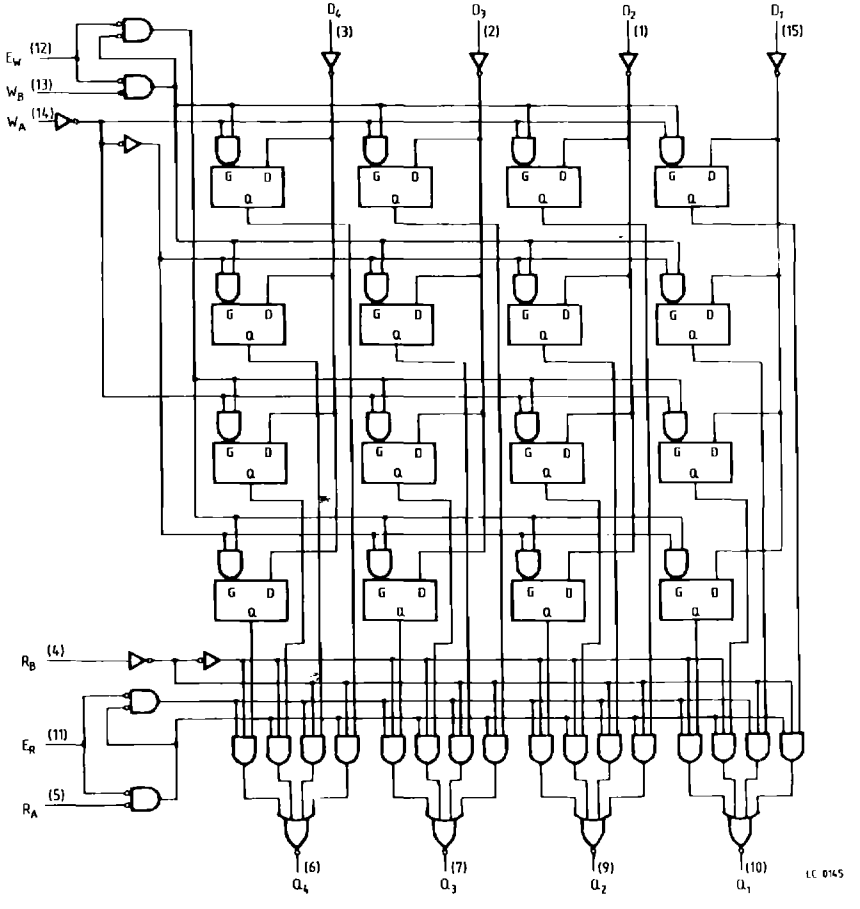
GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS670XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = Package type

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_{IH} = 2.0 V	µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V V_{IH} = 2.0 V	µA
I_{IH}	Input HIGH Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$			 20 40 60	V_{CC} = MAX, V_{IN} = 2.7 V	µA
	Any D, R or W $\overline{E}_W$ $\overline{E}_R$			0.1 0.2 0.3	VCC = MAX, V_{IN} = 7.0 V	mA
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$			 - 0.4 - 0.8 - 1.2	VCC = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V	mA
I_{CC}	Power Supply Current (note 3)		30	50	V_{CC} = MAX	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time
3. Maximum I_{CC} is guaranteed for the following worst-case conditions : 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : $T_A = 25$ °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs		23 25	40 45	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs		26 28	45 50	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		25 23	45 40	Fig. 1		ns
t_{PZH}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going HIGH		15	35	Figs. 4, 5		ns
t_{PZL}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going LOW		22	40	Figs. 3, 5	$V_{CC} = 5.0$ V $C_L = 5.0$ pF	ns
t_{PHZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from HIGH		30	50	Figs. 4, 5		ns
t_{PLZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from LOW		16	35	Figs. 3, 5		ns

AC CHARACTERISTICS : $T_A = 25$ °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_W	Clock Pulse Width (LOW) for $\overline{E}_W$	25			$V_{CC} = 5.0$ V Fig. 3	ns
t_sD (note 5)	Set-up Time, Data Inputs with Respect to Positive-going $\overline{E}_W$	10				ns
t_hD	Hold Time, Data Inputs with Respect to Positive-going $\overline{E}_W$	15				ns
t_sW (note 7)	Set-up Time, Write Select Inputs W_A and W_B with Respect to Negative-going $\overline{E}_W$	15				ns
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Negative-going $\overline{E}_W$	5				ns
t_{rec}	Recovery Time	25				ns

Notes : 5 The data to Enable Set-up time is defined as the time required for the logic level to be present at the data input prior to the enable transition from LOW to HIGH in order for latch to recognize and store the new data.

6. The hold time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
7. The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.
8. The Shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS

Figure 1.

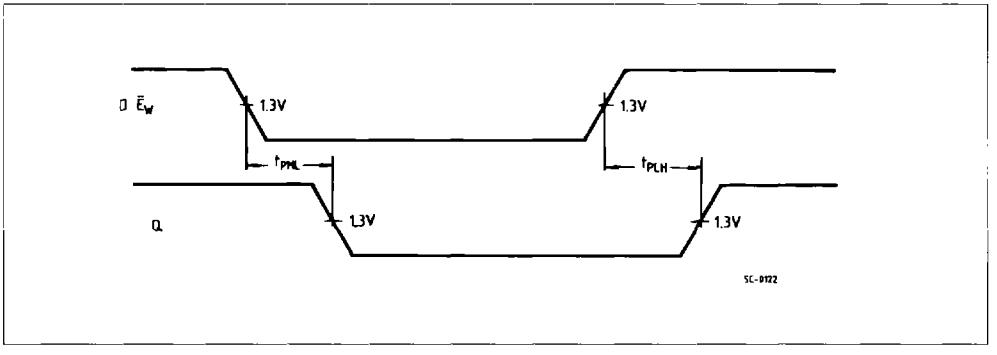


Figure 2.

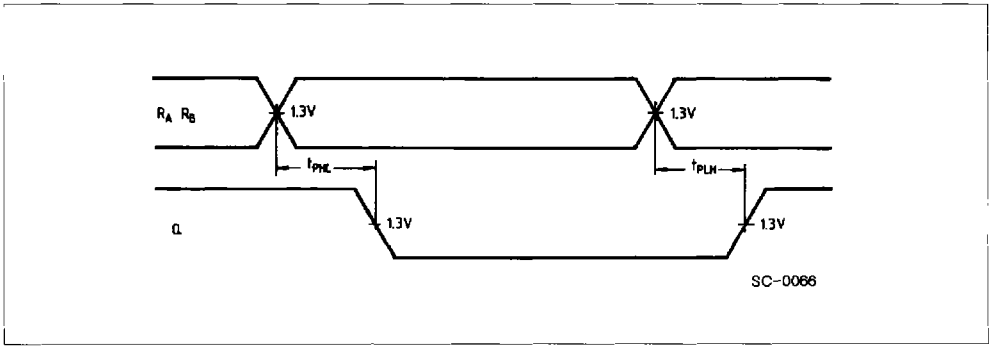


Figure 3.