Clock Generator Circuit for digital TV systems (CGC)

SAA7157

1. FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

2. GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157P	20	DIP	plastic	SOT146-1
SAA7157T	20	SO	plastic	SOT163-1