PACE1753
SINGLE CHIP, 40MHz
CMOS MMU/COMBO

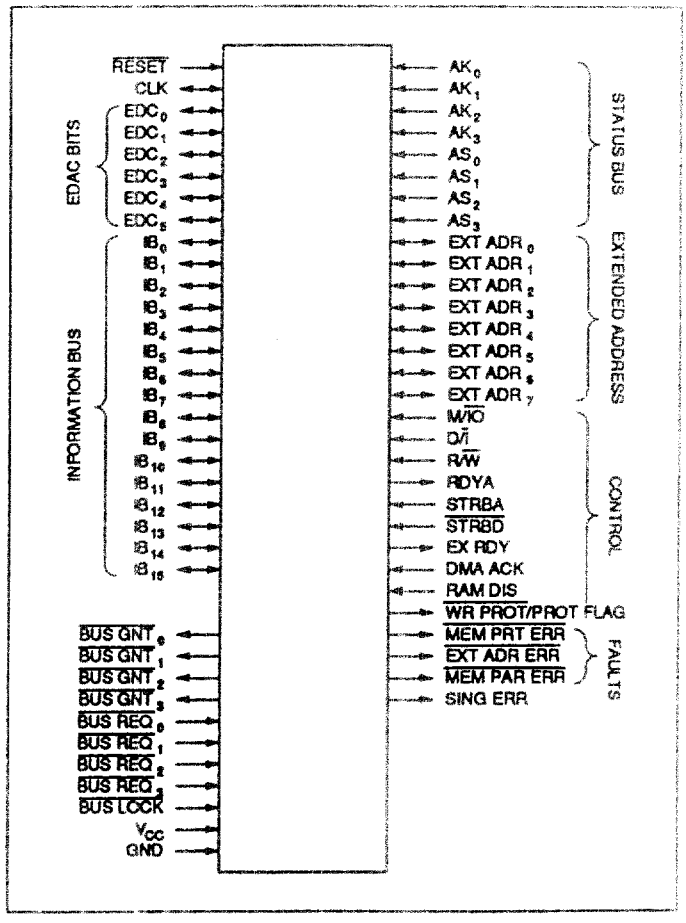
FEATURES

- Implements the MIL-STD-1750A Instruction Set Architecture for Memory Management and Protection of up to 1 Megaword. All mapping memory (10,240 bits) for both the MMU and BPU functions are included on the chip.
- Designed to interface memory to the PACE1750A/AE 16-bit, 40 MHz processor. Systems can be designed where no WAIT states are required up to 40 MHz clock rates when using these PACE products.
- System performance and device count are optimized when used with the PACE1754 Processor Interface Circuit (PIC) and PACE RAM™.
- Provides the following additional functions:
  - EDAC, Error Detection and Correction—or parity generation and detection
  - Correct data register—for diagnostics
  - First memory failing address register
  - Illegal address error detection—programmable
  - Multi-Master arbitration
- 8-bit extended address latches and drivers on chip
- Information bus and EDAC transceivers on chip
- 20, 30 and 40 MHz operation over the Military Temperature Range
- Single 5V ± 10% Power Supply
- Power Dissipation over Military Temperature Range (P_D Outputs Open)
  - < 0.20 watts at 20 MHz
  - < 0.30 watts at 30 MHz
  - < 0.40 watts at 40 MHz
- Available in:
  - 64-Pin DIP or Gull Wing (50 Mil Pin centers)
  - 68-Pin Pin Grid Array (PGA) (100 Mil centers)
  - 68-Lead Quad Pack (Leaded Chip Carrier)

MEMORY MANAGEMENT UNIT AND BLOCK PROTECT UNIT "COMBO" (PACE1753)—FUNCTIONAL DESCRIPTION

The PACE1753 (COMBO) is a support chip for the PACE1750A/AE microprocessor family. It provides the following supporting functions to the system:

1. Memory management and access protection for up to 1M words.
2. Physical memory write protection for up to 1M words memory in pages of 1K words each. Separate protection is provided for the CPU and for DMA in systems which include DMA.
3. Detection of illegal I/O accesses (as defined by MIL-STD-1750A) or access to an unimplemented block of memory. In each case an error flag is generated to the processor.
4. Detection of double errors on the data bus and correction of single errors. An error signal is generated to the processor when a multiple error is detected.
5. RDYA generation. Up to three wait states can be inserted in the address phase of the bus by generating a not-ready, RDYA low signal. The number of wait states required can be programmed in an internal register in the COMBO.
6. Bus arbitration for up to 4 masters. Arbitration is done on a fixed priority basis (i.e. by interconnection of hardware). (In 68 pin package only).



PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	0.5V to +7.0V
Input Voltage Range	0.5V to V_{CC} + 0.5V
Storage Temperature Range	–65°C to +150°C
Input Current Range	–30mA to +5mA
Current applied to any output[3]	150mA
Maximum Power Dissipation[2]	1.5W
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance (θ_{JC}):	
Cases X and T	8°C/W
Cases Y and U	5°C/W
Case Z	6°C/W

Notes

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS}.
3. Duration 1 second or less.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	4.5V to +5.5V
Case Operating Temperature Range	–55°C to +125°C
Operating Maximum Power Dissipation (Outputs Open)	
Device Type 20MHz	0.20W
Device Type 30MHz	0.30W
Device Type 40MHz	0.40W

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage[2]	–0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage		–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA	
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = 4.5V,	I_{OH} = –8.0mA
		V_{CC} – 0.2		V	V_{IN} = 0.8V, 2.0V	I_{OH} = –300µA
V_{OL}	Output LOW Voltage, except EXT ADR_0 – EXT ADR_7		0.5	V	V_{CC} = 4.5V,	I_{OL} = 8.0mA
			0.2	V	V_{IN} = 0.8V, 2.0V	I_{OL} = 300µA
V_{OL}	Output LOW Voltage, EXT ADR_0 – EXT ADR_7		0.5	V	V_{CC} = 4.5V,	I_{OL} = 20.0mA
			0.2	V	V_{IN} = 0.8V, 2.0V	I_{OL} = 300µA
I_{IH}	Input HIGH Current, except IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		10	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IH}	Input HIGH Current, IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		50	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IL}	Input LOW Current, except IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		–10	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{IL}	Input LOW Current, IB_0 – IB_{15}, EDC_0 – EDC_5, EXT ADR_0 – EXT ADR_7		–50	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{OZH}	Output Three-State Current		50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V	
I_{OZL}	Output Three-State Current		–50	µA	V_{OUT} = 0.5V, V_{CC} = 5.5V	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels, Active)		60	mA	V_{IN} < 0.2V or < V_{CC} – 0.2V f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels, Active)		110	mA	V_{IN} = 3.4V, f = 0MHz, All Inputs, Outputs Open, V_{CC} = 5.5V	
I_{CCD}	Dynamic Power Supply Current		40	mA	V_{CC} = 0V to V_{CC}, tr = tf = 2.5 ns, Outputs Open, V_{CC} = 5.5V	F = 20MHz
			50	mA		F = 30MHz
			60	mA		F = 40MHz
I_{OS}	Output Short Circuit Current[3]	–25		mA	V_{OUT} = GND, V_{CC} = 5.5V	
C_{IN}	Input Capacitance		10	pF	Inputs Only	
C_{OUT}	Output/Bi-directional Capacitance		15	pF	Outputs Only (Including I/O Buffers)	

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V)

Symbol	Parameter	20 MHz		30MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	
TD/$\overline{I}$ (EXT ADR)$_V$	MMU Cache Hit		25		23		23	ns
$\overline{TSTRBD}$ ($\overline{EXT\ ADR\ ERR}$)$_L$	External Address Error		25		20		16	ns
TC (IBD CORR)	Error Correction Read Cycle		25		20		19	ns
IBD$_V$ (SING ERR)$_H$	Error Correction Read Cycle		35		30		25	ns
TC (SING ERR)$_L$	Error Correction Read Cycle		25		20		12	ns
TIBD$_V$ (EDC GEN)$_V$	EDAC or Parity Write Cycle		30		25		23	ns
TSTRBD (EX RDY)$_L$	MMU Cache Miss		25		20		12	ns
TC (EX RDY)$_H$	MMU Cache Miss		25		20		12	ns
TC ($\overline{WR\ PROT}$)$_L$	MMU Cache Miss		25		22		18	ns
$\overline{TSTRBD}_H$ ($\overline{WR\ PROT}$)$_H$	MMU Cache Miss		25		20		16	ns
TC ($\overline{GNT1}$)$_H$	Arbiter LOW to HIGH Priority		35		25		18	ns
TC ($\overline{GNT0}$)$_L$	Arbiter LOW to HIGH Priority		35		25		18	ns
TC ($\overline{GNT0}$)$_H$	Arbiter HIGH to LOW Priority		35		25		18	ns
TC ($\overline{GNT1}$)$_L$	Arbiter HIGH to LOW Priority		35		25		18	ns
TC (RDYA)	Address Ready		30		25		17	ns
TFC (IB OUT)$_V$	Clock to IB Out Valid (I/O Read)		30		28		25	ns
TIBD$_{IN}$ ($\overline{MEM\ PAR\ ERR}$)	Parity Mode		34		30		25	ns
TC ($\overline{MEM\ PRT\ ERR}$)	Memory Protect Error		50		45		40	ns
$\overline{TSTRBD}$ ($\overline{WR\ PROT}$)	Write Protect Cache Hit		25		20		16	ns
TC ($\overline{WR\ PROT}$)$_L$	Write Protect Cache Miss		25		22		18	ns
$\overline{TSTRBD}_H$ ($\overline{WR\ PROT}$)$_H$	Write Protect Cache Miss		25		22		18	ns
TD/$\overline{I}$ (PROT FLAG)	Cache Hit (BPU Protection Error)		50		45		40	ns
TD/$\overline{I}$ (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		40		35		30	ns
TC (PROT FLAG)	Cache Miss (BPU Protection Error)		45		35		30	ns
TC (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		25		20		20	ns
TC (EXT ADR)	Clock to EXT ADR Valid (Miss)		32		30		23	ns

Notes:

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.
4. Pulse width of $\overline{WR\ PROT}$/PROT FLAG shall be ≥ 80% of STRBD pulse width.

TERMINAL CONNECTIONS

Case Outlines		T and X			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	23	IB_{13}	44	AS_1
2	EDC_0	24	IB_{14}	45	AS_0
3	EDC_1	25	IB_{15}	46	GND
4	EDC_2	26	$\overline{\text{MEM PRT ERR}}$	47	AK_3
5	$\overline{\text{RESET}}$	27	$\overline{\text{MEM PAR ERR}}$	48	AK_2
6	EDC_3	28	$\overline{\text{EXT ADR ERR}}$	49	AK_1
7	EDC_4	29	RAM DIS	50	AK_0
8	EDC_5	30	SING ERR	51	CLK
9	IB_0	31	DMA ACK	52	STRBA
10	IB_1	32	GND	53	$\overline{\text{STRBD}}$
11	IB_2	33	$EXT\ ADR_0$	54	GND
12	IB_3	34	$EXT\ ADR_1$	55	EX RDY
13	IB_4	35	$EXT\ ADR_2$	56	$\overline{\text{WR PROT}}$/PROT FLAG
14	IB_5	36	$EXT\ ADR_3$	57	$R/\overline{W}$
15	IB_6	37	$EXT\ ADR_4$	58	$D/\overline{I}$
16	IB_7	38	$EXT\ ADR_5$	59	$M/\overline{IO}$
17	IB_8	39	$EXT\ ADR_6$	60	RDYA
18	IB_9	40	$EXT\ ADR_7$	61	NC
19	VCC	41	VCC	62	NC
20	IB_{10}	42	AS_3	63	NC
21	IB_{11}	43	AS_2	64	VCC
22	IB_{12}				

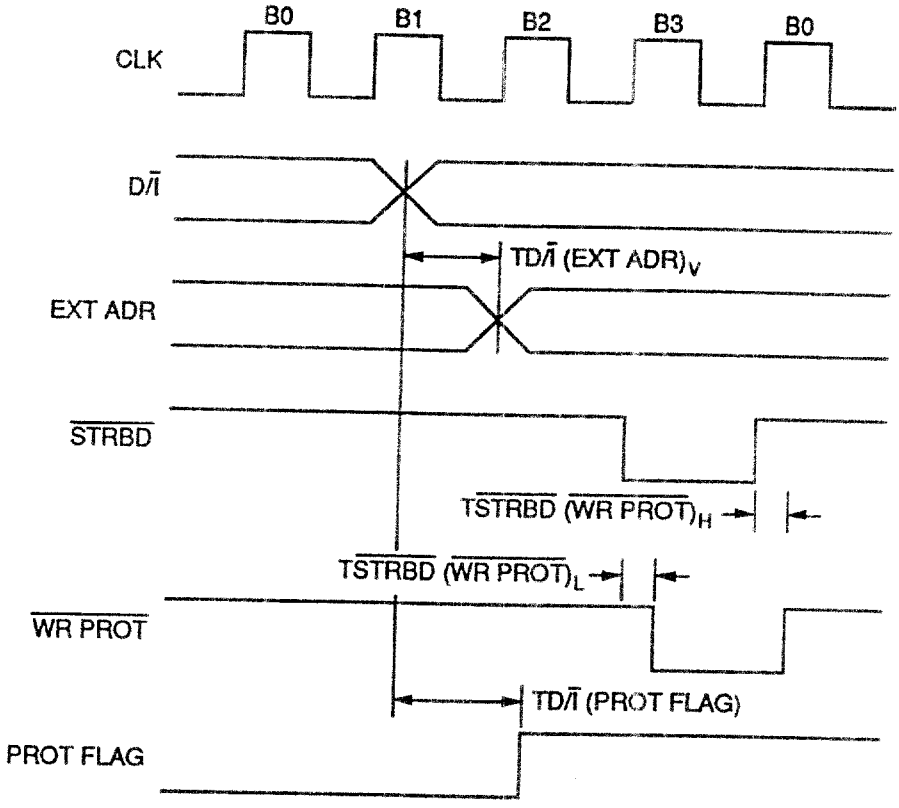
TERMINAL CONNECTIONS

Case Outlines		U and Y			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	24	IB_{12}	47	AS_1
2	EDC_0	25	IB_{13}	48	AS_0
3	EDC_1	26	IB_{14}	49	$\overline{BUS\ REQ_2}$
4	EDC_2	27	IB_{15}	50	AK_3
5	$\overline{RESET}$	28	$\overline{MEM\ PRT\ ERR}$	51	AK_2
6	EDC_3	29	$\overline{MEM\ PAR\ ERR}$	52	$\overline{BUS\ GNT_1}$
7	EDC_4	30	$\overline{EXT\ ADR\ ERR}$	53	AK_1
8	EDC_5	31	RAM DIS	54	AK_0
9	$\overline{BUS\ GNT_2}$	32	SING ERR	55	CLK
10	IB_0	33	DMA ACK	56	STRBA
11	IB_1	34	GND	57	$\overline{STRBD}$
12	IB_2	35	V_{CC}	58	$\overline{BUS\ REQ_0}$
13	IB_3	36	$EXT\ ADR_0$	59	EX RDY
14	IB_4	37	$EXT\ ADR_1$	60	$\overline{WR\ PROT}$/PROT FLAG
15	IB_5	38	$EXT\ ADR_2$	61	$R/\overline{W}$
16	IB_6	39	$EXT\ ADR_3$	62	$D/\overline{I}$
17	IB_7	40	$EXT\ ADR_4$	63	$M/\overline{IO}$
18	$\overline{BUS\ REQ_3}$	41	$EXT\ ADR_5$	64	RDYA
19	IB_8	42	$EXT\ ADR_6$	65	$\overline{BUS\ GNT_0}$
20	IB_9	43	$EXT\ ADR_7$	66	$\overline{BUS\ LOCK}$
21	$\overline{BUS\ GNT_3}$	44	GND	67	$\overline{BUS\ REQ_1}$
22	IB_{10}	45	AS_3	68	V_{CC}
23	IB_{11}	46	AS_2		

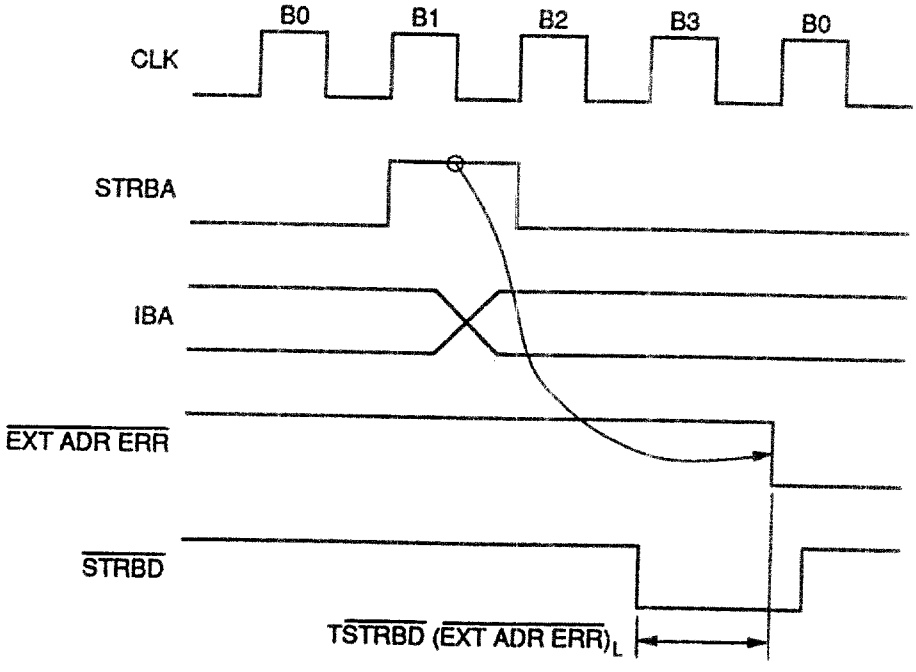
TERMINAL CONNECTIONS

Case Outline		Z			
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
B1	IB_{14}	L5	EDC_1	D11	AS_0
B2	IB_{13}	K5	EDC_0	D10	AS_1
C1	IB_{12}	L6	GND	C11	AS_2
C2	IB_{11}	K6	VCC	C10	AS_3
D1	IB_{10}	L7	$\overline{\text{BUS REQ}}_1$	B11	VCC
D2	$\overline{\text{BUS GNT}}_3$	K7	BUS LOCK	A10	GND
E1	IB_9	L8	$\overline{\text{BUS GNT}}_0$	B10	EXT ADR_7
E2	IB_8	K8	RDYA	A9	EXT ADR_6
F1	$\overline{\text{BUS REQ}}_3$	L9	M/$\overline{\text{IO}}$	B9	EXT ADR_5
F2	IB_7	K9	D/$\overline{\text{I}}$	A8	EXT ADR_4
G1	IB_6	L10	R/$\overline{\text{W}}$	B8	EXT ADR_3
G2	IB_5	K11	$\overline{\text{WR PROT}}$/PROT FLAG	A7	EXT ADR_2
H1	IB_4	K10	EX RDY	B7	EXT ADR_1
H2	IB_3	J11	$\overline{\text{BUS REQ}}_0$	A6	EXT ADR_0
J1	IB_2	J10	$\overline{\text{STRBD}}$	B6	GND
J2	IB_1	H11	STRBA	A5	DMA ACK
K1	IB_0	H10	CLK	B5	SING ERR
L2	$\overline{\text{BUS GNT}}_2$	G11	AK_0	A4	RAM DIS
K2	EDC_5	G10	AK_1	B4	$\overline{\text{EXT ADR ERR}}$
L3	EDC_4	F11	$\overline{\text{BUS GNT}}_1$	A3	$\overline{\text{MEM PAR ERR}}$
K3	EDC_3	F10	AK_2	B3	$\overline{\text{MEM PRT ERR}}$
L4	$\overline{\text{RESET}}$	E11	AK_3	A2	IB_{15}
K4	EDC_2	E10	$\overline{\text{BUS REQ}}_2$		

MMU Cache Hit

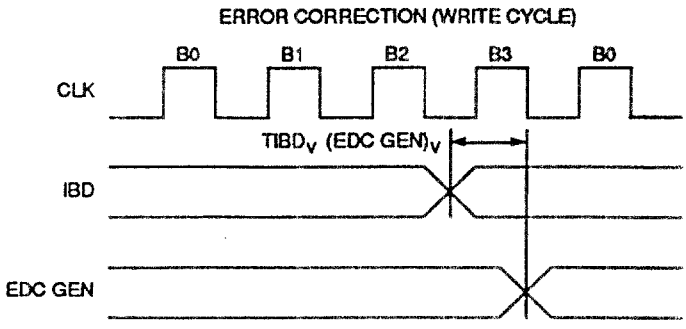


External Address Error

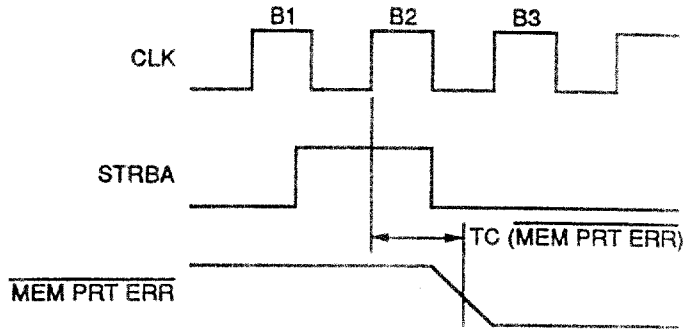


Note:
All time measurements on active signals relate to 1.5V levels.

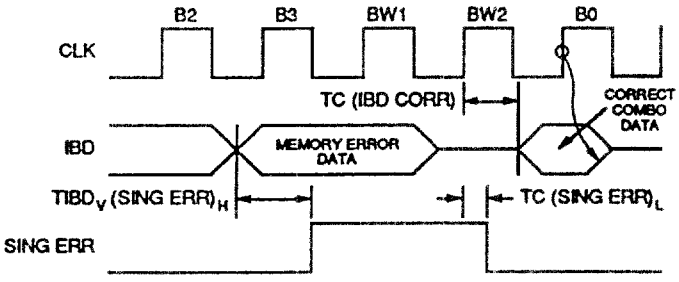
Error Correction (Write Cycle)



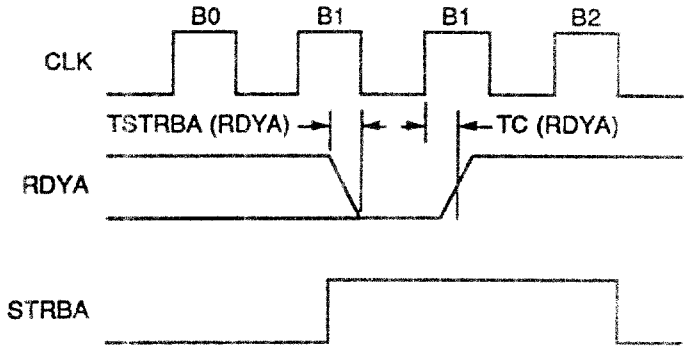
Memory Protect Error



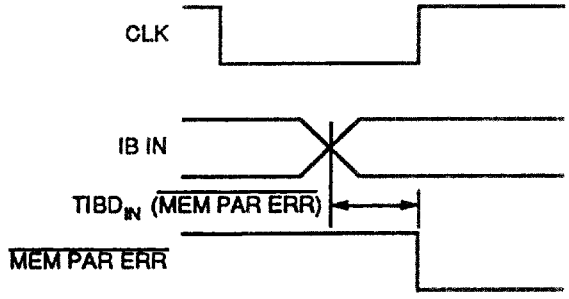
Error Correction (Read Cycle)



Ready Address

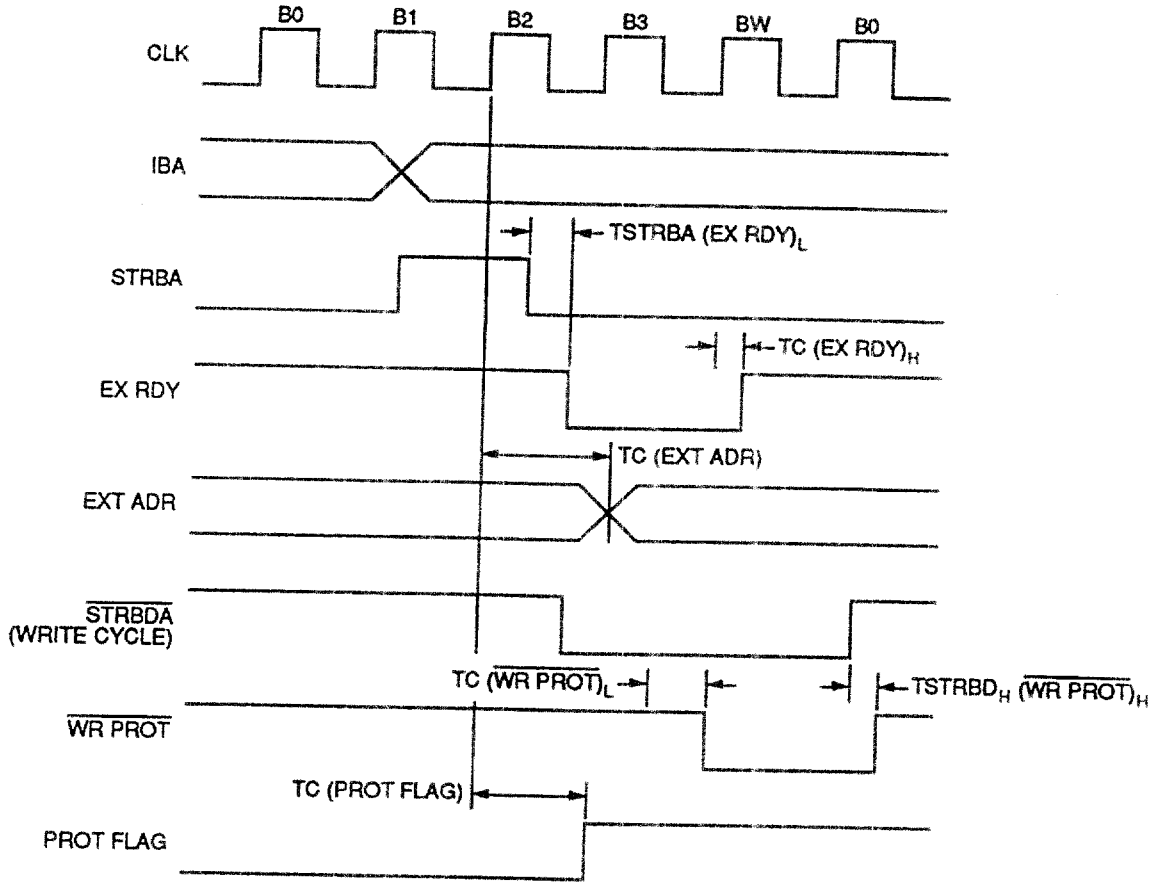


Memory Parity Error

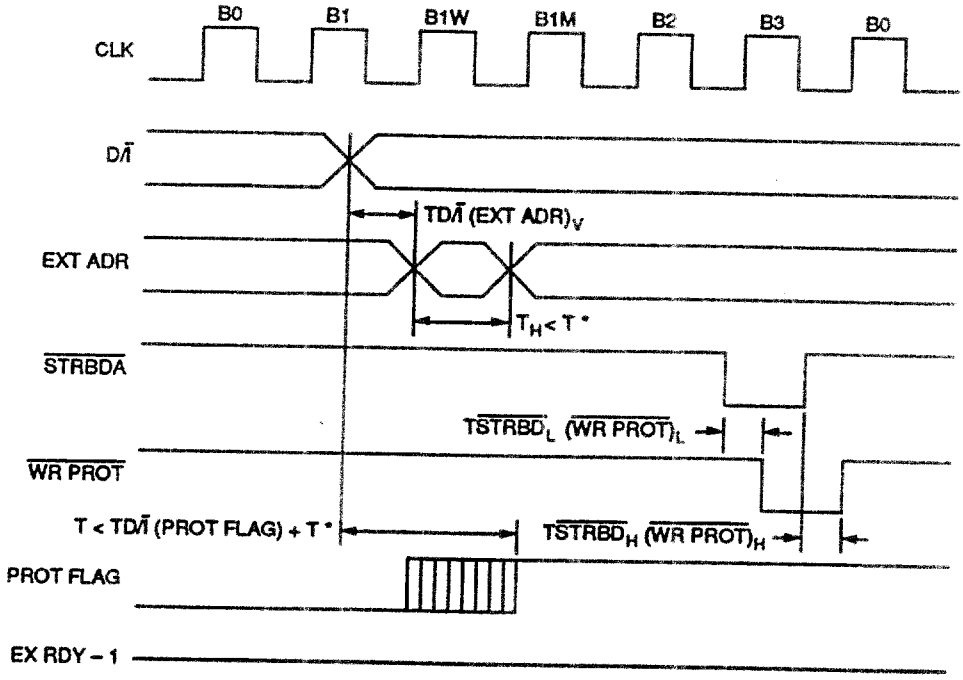


Note:
All time measurements on active signals relate to 1.5V levels.

MMU Cache Miss Cycle (WA = 0)



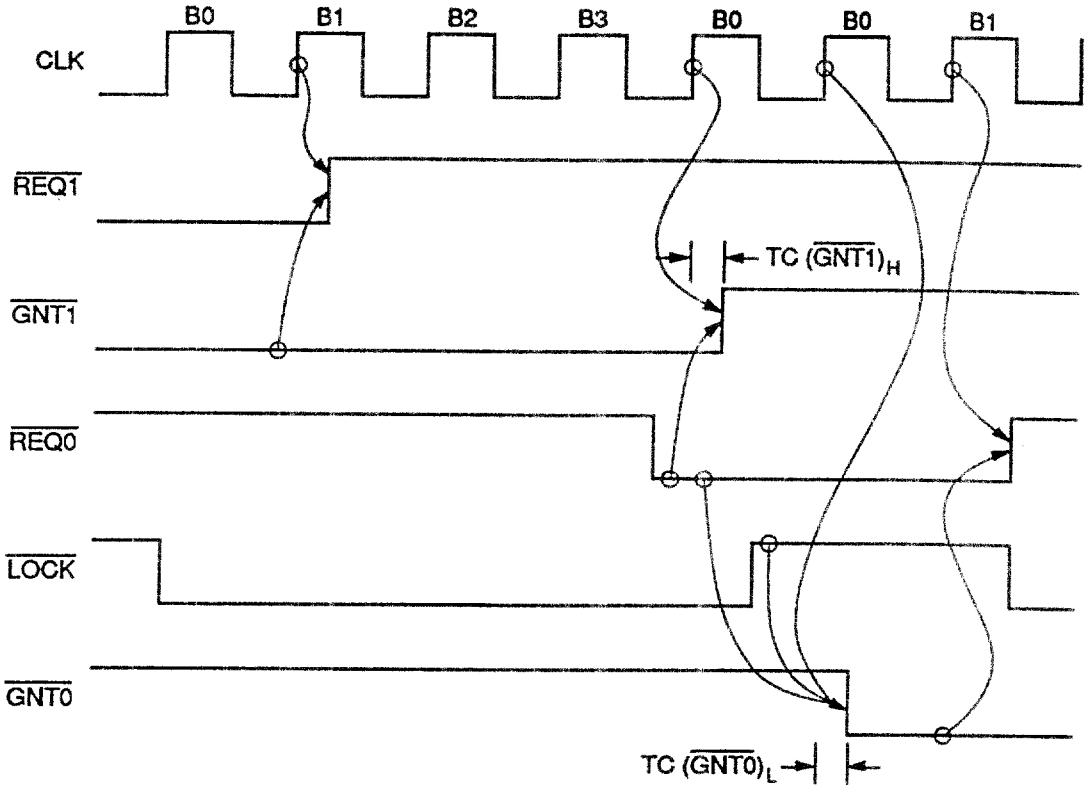
MMU Cache Miss Cycle (WA > 0)



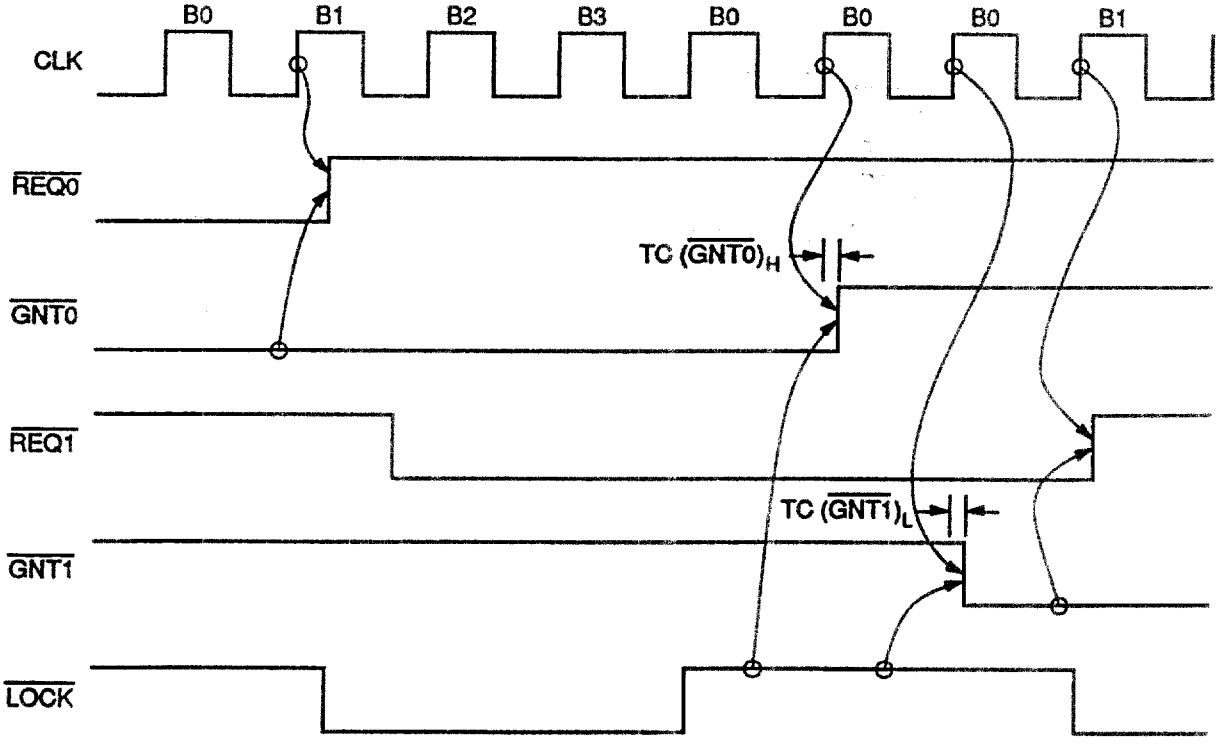
* The WR PROT/PROT FLAG signal is programmed as WR PROT or PROT FLAG. (See BPU Description), T = 1 Clock Period.

Note:
All time measurements on active signals relate to 1.5V levels.

Low Priority to High Priority Transition



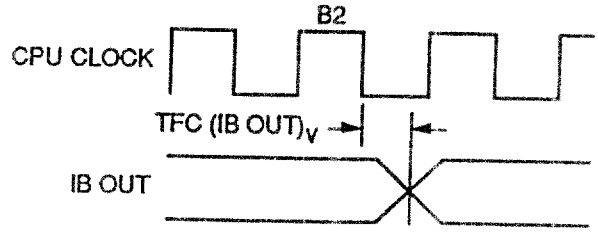
Bus Arbitrator High Priority to Low Priority Transition



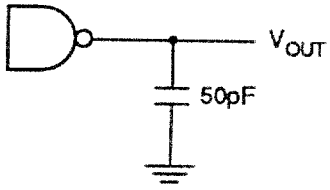
Note:
All time measurements on active signals relate to 1.5V levels.

SWITCHING WAVEFORMS AND TEST CIRCUIT (Continued)

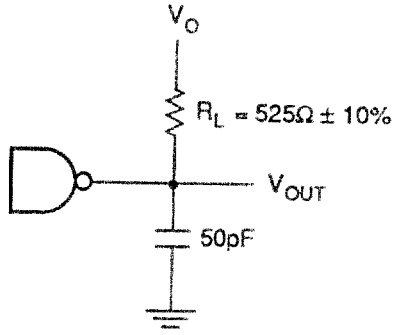
IB Bus Output (0:15)



Standard Output (Non Three-State)



Three-State



Note:
All time measurements on active signals relate to 1.5V levels.

Parameter	V_O	V_{MEA}
TPLZ	≥ 3V	0.5V
TPHZ	0V	V_{CC} – 0.5V
TPXL	$V_{CC}/2$	1.5V
TPXH	$V_{CC}/2$	1.5V

PIN FUNCTIONS

Symbol	Name	Description
$\overline{\text{BUS REQ}_0}$ - $\overline{\text{BUS REQ}_3}$	Bus Request[1]	Active low inputs that indicate a requirement for the bus from 4 masters on the bus. The master assigned to pin $\overline{\text{BUS-REQ}_0}$ has highest priority; the master assigned to pin $\overline{\text{BUS-REQ}_3}$ has lowest priority.
$\overline{\text{BUS LOCK}}$	Bus Lock[1]	An active low input that indicates that the one master assigned the bus is using the bus. A new master will receive a bus grant only after this signal becomes inactive.
$\overline{\text{BUS GNT}_0}$ - $\overline{\text{BUS GNT}_3}$	Bus Grant[1]	Active low outputs indicating which master was granted the bus. It remains active during $\overline{\text{BUS LOCK}}$ unless a higher master request occurs, which resets it. However, the higher master will be granted the bus only after the present master's $\overline{\text{BUS LOCK}}$ releases the bus.
M/$\overline{\text{IO}}$	Memory or I/O	An input signal that indicates whether the current bus cycle is a memory (high) or I/O (low) cycle.
D/$\overline{\text{I}}$	Data or Instruction	An input signal that indicates whether the current bus cycle access is for data (high) or instruction (low).
R/$\overline{\text{W}}$	Read or Write	An input signal that indicates the direction of data flow on the bus. A high indicates a memory read or input operation into the master and a low indicates a memory write or output operation from the master.
STRBA	Address Strobe	An active high input used to latch the address at the high-to-low transition of the strobe.
$\overline{\text{STRBD}}$	Data Strobe	An active low input used to strobe data in memory and I/O cycles.
CPU-CLK	CPU Clock	A single-phase input clock signal (0-40MHz, 40% to 60% duty cycle.)
$\overline{\text{RESET}}$	Reset	An active low input that initializes the device.
AK_0 - AK_3	Access Key	Active high inputs used to match the access lock in the MMU page for memory accesses. A mismatch will cause the $\overline{\text{MEM PRT ERR}}$ signal to become active.
AS_0 - AS_3	Address State	Active high inputs that select the page register group in the MMU. In the DMA physical demultiplexed mode, AS(0:1) will receive the 9th and 10th most significant bits of the physical address for use in the BPU function.
EXT ADR_0 - EXT ADR_7	Extended Addresses Bus	A bi-directional active high bus. In CPU cycles, it is an output bus which is used to select one of 256 pages, 4K words each, expanding the direct addressing space to 1M word. In DMA cycles, indicated by DMA-ACK being active, it is also an output bus except when programmed for the physical demultiplexed DMA mode. In this case it becomes an input to receive the 8 most significant bits of the DMA physical address for use in the BPU function.
IB_0 - IB_{15}	Information Bus	An active high bi-directional time multiplexed address/data bus. IB_0 is the most significant bit.
EDC_0 - EDC_5	Detection/Correction Bus	An active high bi-directional bus used for detection of errors on the data bus (IB_0 - IB_{15}) and correction of single errors. When working in parity mode EDC_0 is the parity bit. EDC_0 - EDC_5 are undefined in this case.

PIN FUNCTIONS (Continued)

Symbol	Name	Description
$\overline{\text{MEM PRT ERR}}$	Memory Protect Error	An active low output generated by the MMU or BPU blocks to signal to the CPU a protected memory violation. The error is generated in one of the following conditions: a mismatch in the access keys in the MMU page, an access to an execution protected page during instruction cycles, an access to a write-protected page during data cycles, or an access to a page write-protected by the BPU.
$\overline{\text{MEM PAR ERR}}$	Memory Parity Error	An active low output which signals to the CPU an error on the data bus during a memory cycle. Two detection modes can be selected by programming the control register: EDAC mode (6 Hamming code parity bits) or single bit parity mode (even or odd parity). The signal is inactive when none of the above modes are selected (default after Reset).
$\overline{\text{EXT ADR ERR}}$	External Address Error	An active low output which signals to the CPU an unimplemented memory or illegal I/O access.
SING ERR	Single Error	An active high output to signal detection of a single error on the data bus in memory cycles. It is high impedance when the EDAC function is disabled by the program (default state after Reset).
RAM DIS	RAM-Disable	An active high input from the 5962-88642 device which enables the corrected data on the data bus when the EDAC function is enabled. An internal one clock delay is generated before the data is output on the bus to allow external memory to disconnect itself from the bus.
EX RDY	Data Ready	An active high output that indicates that no wait states are requested. It becomes inactive for one clock (inserting one wait state) whenever a memory page different than the current one is accessed (causing a miss).
RDYA	Address Ready	An active high output that indicates that no wait states are requested when STRBA is active. Wait states are inserted when this signal becomes inactive during STRBA. Up to three wait states can be inserted by programming an internal register. Three wait states are inserted after Reset (default).
$\overline{\text{WR PROT}}$/ PROT FLAG	Write Protected/ Protection Flag	Either an active low output (following $\overline{\text{STRBD}}$ timing) during legal memory write cycles, when no protection error occurs, or an active high level indicating a protection error in a write cycle. Each mode can be selected by programming the control register. Default mode after Reset is write-protected.
DMA ACK	DMA Acknowledge	An active high input from the DMA controller which indicates a DMA cycle. Used to select the DMA table in the BPU memory for protection. For example, this could allow the DMA channel to update the program which could be write-protected from the processor. In the physical DMA mode, it will cause the Extended Address Lines (EXT ADR_{0-7}) to become inputs, providing BPU protection of the DMA transfers.

Note:

1. Used for Bus Arbitration; only available on 68-lead devices.

Standardized Military Drawing PIN	Vendor CAGE Number	Vendor similar PIN
5962-8950501UX	75569	P1753-20QLMB
5962-8950501YX	75569	P1753-20QGMB
5962-8950501ZX	75569	P1753-20PGMB
5962-8950502UX	75569	P1753-30QLMB
5962-8950502YX	75569	P1753-30QGMB
5962-8950502ZX	75569	P1753-30PGMB
5962-8950503UX	75569	P1753-40QLMB
5962-8950503YX	75569	P1753-40QGMB
5962-8950503ZX	75569	P1753-40PGMB
5962-8950504TX	75569	P1753-20GMB
5962-8950504XX	75569	P1753-20CMB
5962-8950505TX	75569	P1753-30GMB
5962-8950505XX	75569	P1753-30CMB
5962-8950506TX	75569	P1753-40GMB
5962-8950506XX	75569	P1753-40CMB

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