MSC23136B/BL-xxBS12/DS12

1,048,576-Word by 36-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC23136B/BL-xxBS12/DS12 is a fully decoded 1,048,576-word x 36-bit CMOS Dynamic Random Access Memory Module composed of eight 4-Mb DRAMs in SOJ (MSM514400B/BL) packages and four 1-Mb DRAMs in PLCC (MSM511000B/BL) packages mounted with twelve 0.2 µF decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations. The low-power version (BL) offers reduced power consumption for mobile computing applications like laptops and palmtops..

FEATURES

- 1-Meg x 36-bit organization
- 72-pin socket insertable module
  - MSC23136B/BL-xxBS12: Gold tab
  - MSC23136B/BL-xxDS12: Solder tab
- Single +5 V supply ±10 % tolerance
- Access times: 60, 70, 80, 100 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 1024 cycles/16 ms (128 ms: L-version)
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$-only refresh capability

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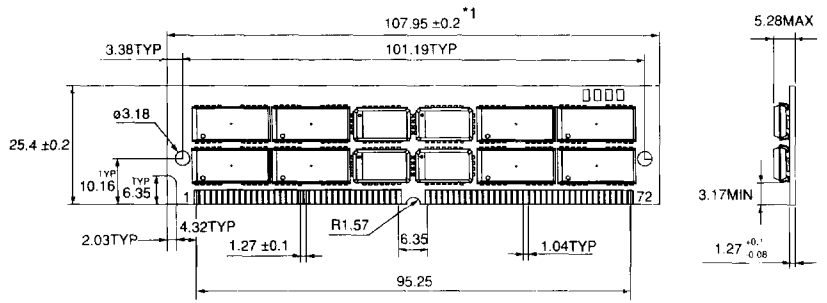
Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC23136B/BL-60BS12/DS12	60 ns	30 ns	15 ns	120 ns	6380 mW	66 mW
MSC23136B/BL-70BS12/DS12	70 ns	35 ns	20 ns	130 ns	5720 mW	
MSC23136B/BL-80BS12/DS12	80 ns	40 ns	20 ns	150 ns	5060 mW	13.2 mW (L-version)
MSC23136B/BL-10BS12/DS12	100 ns	50 ns	25 ns	190 ns	4400 mW	

PIN CONFIGURATION

MSC23136B/BL-xxBS12/DS12



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2. The value above 12.5mm is specified as ±0.5.

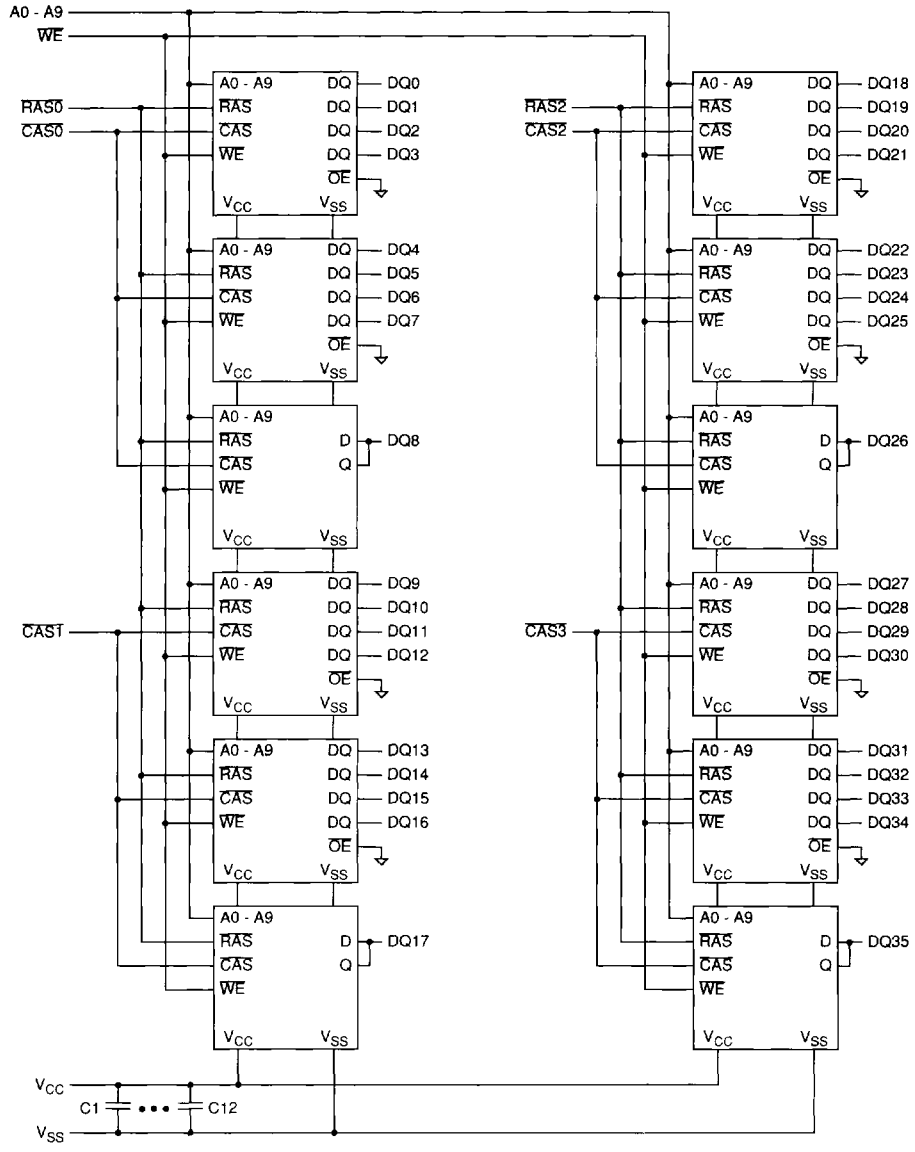
Pin Configuration

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{SS}	16	A4	31	A8	46	N.C.	61	DQ14
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	N.C.	48	N.C.	63	DQ15
4	DQ1	19	N.C.	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	N.C.
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	V_{SS}	54	DQ29	69	PD2
10	V_{CC}	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD3
11	N.C.	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	N.C.
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	N.C.	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	V_{CC}	45	N.C.	60	DQ32		

Presence Detect Pins

Pin Number	Pin Name	60 ns	70 ns	80 ns	100 ns
67	PD0	V_{SS}	V_{SS}	V_{SS}	V_{SS}
68	PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
69	PD2	N.C.	V_{SS}	N.C.	V_{SS}
70	PD3	N.C.	N.C.	V_{SS}	V_{SS}

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ +7.0	V
Voltage V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 ~ +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	12	W
Operating temperature	T_{OPR}	0 ~ +70	°C
Storage temperature	T_{STG}	-40 ~ +125	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	6.5	V
Input low voltage	V_{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) [1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A9)	C_{IN1}	-	102	pF
Input capacitance ($\overline{WE}$)	C_{IN2}	-	104	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	-	62	pF
Input capacitance ($\overline{CAS0}$ ~ $\overline{CAS3}$)	C_{IN4}	-	41	pF
I/O capacitance (DQ0~DQ7, DQ9 ~ DQ16, DQ18 ~ DQ25, DQ27 ~ DQ34)	C_{DQ1}	-	17	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	-	23	pF

1. Capacitance measured with Boonton Meter.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition		60 ns		70 ns		80 ns		100 ns		Unit	Note
				Min	Max	Min	Max	Min	Max	Min	Max		
Input leakage current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V		-120	120	-120	120	-120	120	-120	120	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V		-10	10	-10	10	-10	10	-10	10	µA	
Output high voltage	V_{OH}	I_{OH} = -5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min.		-	1160	-	1040	-	920	-	800	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z	TTL	-	24	-	24	-	24	-	24	mA	
			MOS	-	12	-	12	-	12	-	12	mA	
				-	2.4	-	2.4	-	2.4	-	2.4	mA	[3]
Average power supply current ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min.		-	1160	-	1040	-	920	-	800	mA	[1] [2]
Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.		-	1160	-	1040	-	920	-	800	mA	[1]
Average power supply current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min.		-	960	-	840	-	720	-	620	mA	[1] [4]
Average power supply current (Battery Backup)	I_{CC10}	t_{RC} = 125 µs, $\overline{CAS}$-before-$\overline{RAS}$ cycling		-	3.6	-	3.6	-	3.6	-	3.6	mA	[1] [3]

1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. L-version only t_{RAS}=t_{RAS} (min.) to 1 µs. Input voltage: All pins V_{IH} ≥ V_{CC} -0.2 V or V_{IL} ≤ 0.2 V
4. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

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AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3]

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	-	130	-	150	-	190	-	ns	
Fast Page Mode cycle time	t_{PC}	40	-	45	-	50	-	60	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	-	80	-	100	ns	[4] [5] [6]
Access time for $\overline{CAS}$	t_{CAC}	-	15	-	20	-	20	-	25	ns	[4] [5]
Access time from column address	t_{AA}	-	30	-	35	-	40	-	50	ns	[4] [6]
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	-	45	-	55	ns	[4]
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	20	0	25	ns	[7]
Transition time	t_T	3	50	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	16	-	16	-	16	-	16	ms	
Refresh period (L-version)	t_{REF}	-	128	-	128	-	128	-	128	ms	
$\overline{RAS}$ precharge time	t_{RP}	50	-	50	-	60	-	80	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	20	-	20	-	25	-	ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	-	70	-	80	-	100	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	25	75	ns	[5]
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	20	50	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	15	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	20	-	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	50	-	55	-	60	-	75	-	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	40	-	50	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	0	-	ns	[8]
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	0	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	15	-	20	-	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	50	-	55	-	60	-	75	-	ns	
Write command pulse width	t_{WP}	10	-	15	-	15	-	20	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	-	20	-	20	-	25	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	-	20	-	20	-	25	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	0	-	ns	

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] (Continued)

Parameter	Symbol	60 ns		70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15	-	15	-	15	-	20	-	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	50	-	55	-	60	-	75	-	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	-	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CSR}	10	-	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CHR}	30	-	30	-	30	-	30	-	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	40	-	50	-	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{WRP}	10	-	10	-	10	-	10	-	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{WRH}	10	-	10	-	10	-	10	-	ns	

1. A start-up delay of 200 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh) before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles is required.
2. AC measurements assume t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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See ADDENDUM D for AC Timing Waveforms