FUJITSU

CMOS 65536-BIT BI-CMOS STATIC RANDOM ACCESS MEMORY	MB82B75-15 MB82B75-20

TS270-A893
March 1989

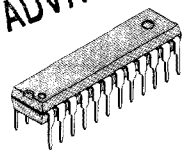
64K-BIT(16,384 x 4) Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

ADVANCE INFO.

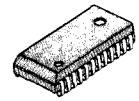
The Fujitsu MB82B75 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

MB82B75 has 300mil plastic DIP and plastic small outline J-lead(SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB82B75 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.



PLASTIC PACKAGE
DIP-24P-M03

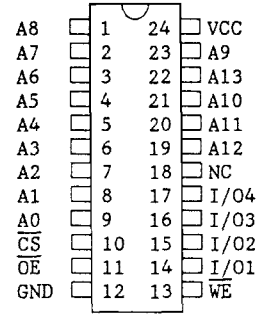


PLASTIC PACKAGE
LCC-24P-M02

- 16,384 words x 4 bits organization
- Fast access time:
  tAA=tACS=15ns max. / tOE=10ns max. (MB82B75-15)
  tAA=tACS=20ns max. / tOE=12ns max. (MB82B75-20)
- Bi-CMOS peripheral
- TTL compatible inputs/outputs
- Completely static operation: No clock required
- Three-state output
- Common data input/output
- Single=5V(±10%) power supply with low current drain
  Active operation = 120mA max.
  Standby operation = 15 mA max.(CMOS level)
  Standby operation = 25 mA max.(TTL level)
- Standard 24-pin plastic DIP package : Suffix -P-SK
- Standard 28-pad Leadless Chip Carrier:Suffix -CV
- Standard 24-pin plastic SOJ package : Suffix -PJ
- Pin compatible with MB81C75

PIN ASSIGNMENT

(TOP VIEW)



LCC: See page 9

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Values	Unit
Supply Voltage		VCC	-0.5 to +7.0	V
Input Voltage		VIN	-3.5 to +7.0	V
Output Voltage		VI/O	-0.5 to +7.0	V
Output Current		IOUT	±20	mA
Power Dissipation		PD	1.0	W
Temperature Under Bias		TBIAS	-10 to +85	°C
Storage Temperature Range	Ceramic	TSTG	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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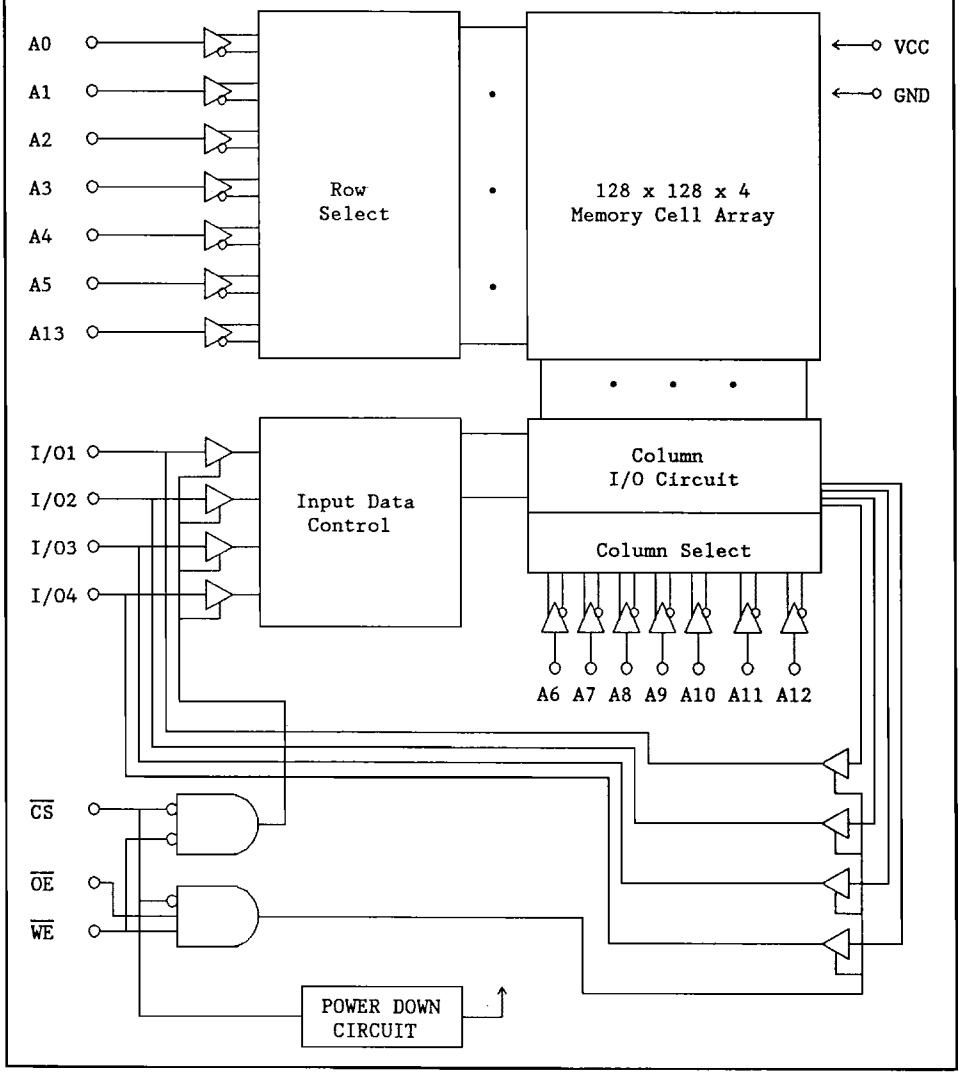
Fig. 1 - MB82B75 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance(V/CS=0V)	C/CS			6	pF
Input Capacitance(VIN=0V)	CIN			5	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A13	Address input.	$\overline{WE}$	Write Enable.
I/O1 to I/O4	Data input/output.	VCC	Power Supply(+5V±10%).
$\overline{CS}$	Chip Select 1.	GND	Ground.
NC	No Connect		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	Power Supply Current
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Disable	High-Z	Active
L	H	L	Read	DOUT	Active
L	L	X	Write	DIN	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

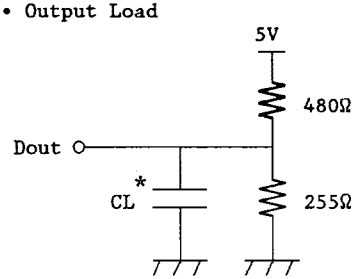
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-5	5	µA
Output Leakage Current	VI/O=GND to VCC $\overline{CS}$=VIH or $\overline{WE}$=VIL	ILI/O	-5	5	µA
Operating Supply Current	$\overline{CS}$=VIL, I/O=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{CS}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS}$=VIH VCC=min. to max.	ISB2		25	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	*1 -0.5	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{CS}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ
Load II	5pF	tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ

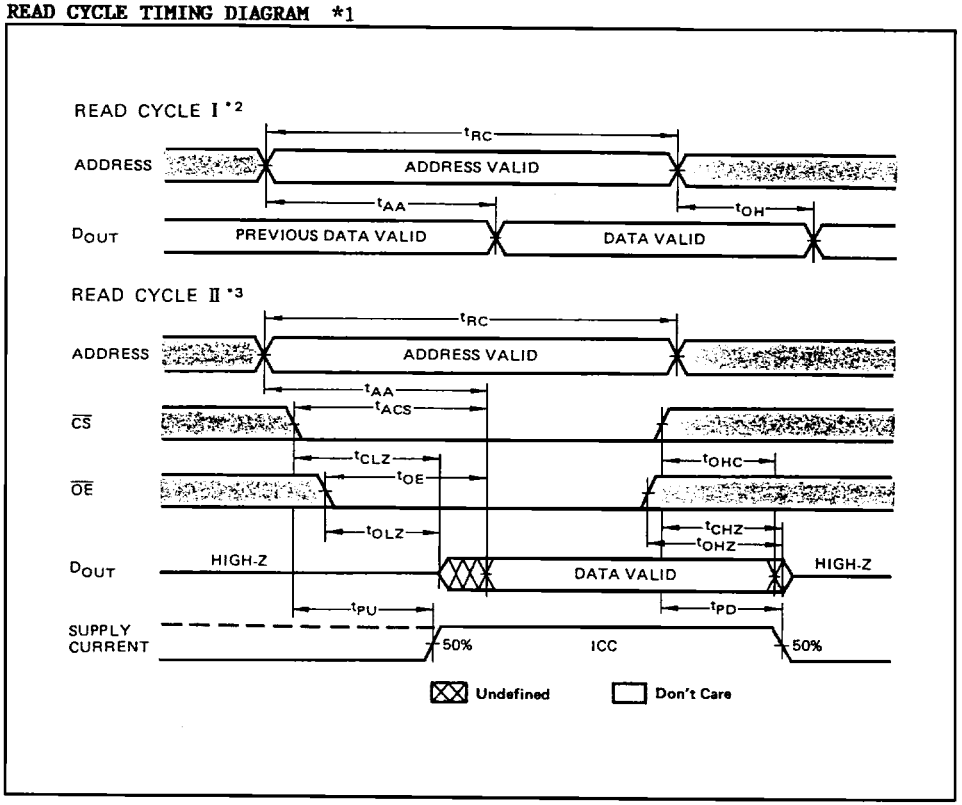
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B75-15		MB82B75-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time	tAA		15		20	ns
/CS Access Time	tACS		15		20	ns
/OE Access Time	tOE		10		12	ns
Output Hold from Address Change	tOH	3		3		ns
Output Hold from /CS	tOHC	2		2		ns
Output Low-Z from /CS	tCLZ	3		3		ns
Output Low-Z from /OE	tOLZ	2		2		ns
Output High-Z from /CS	tCHZ		8		10	ns
Output High-Z from /OE	tOHZ		8		10	ns
Power Up from /CS	tPU	0		0		ns
Power Down from /CS	tPD		15		15	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continously selected, $\overline{CS}$=VIL, $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE

Parameter	Symbol	MB82B75-15		MB82B75-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15		20		ns
Address Valid to End of Write	tAW	10		15		ns
/CS to End of Write	tCW	10		15		ns
Data Setup Time	tDW	7		10		ns
Data Hold Time	tDH	3		3		ns
Write Pulse Width	tWP	8		10		ns
Write Recovery Time	tWR	2		2		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from /WE	tWLZ	0		0		ns
Output High-Z from /WE	tWHZ		8		10	ns

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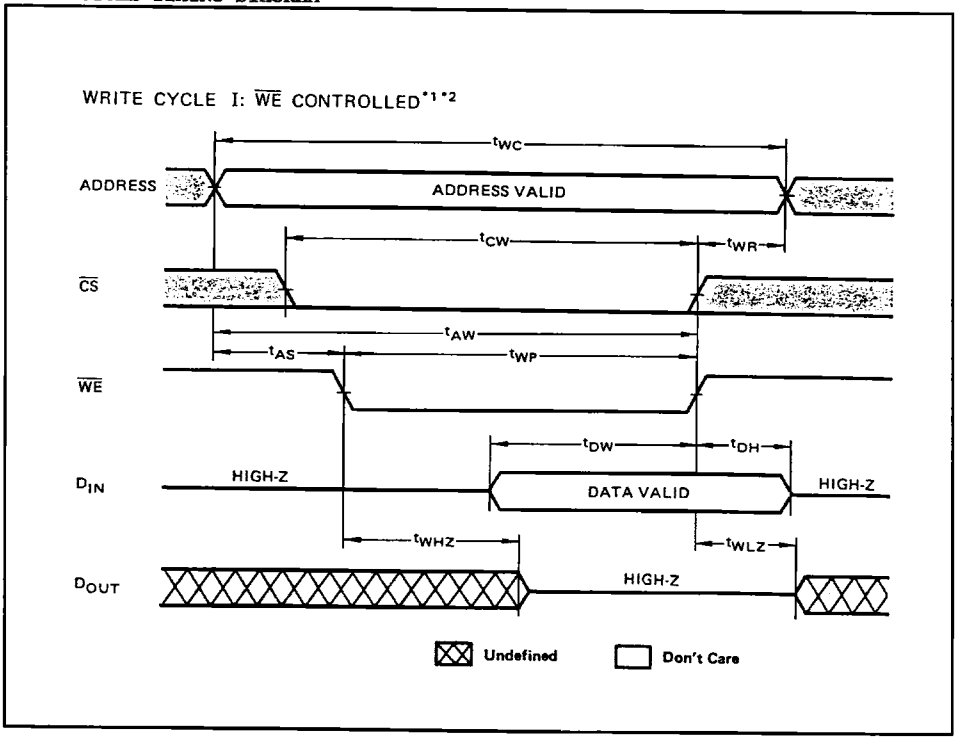
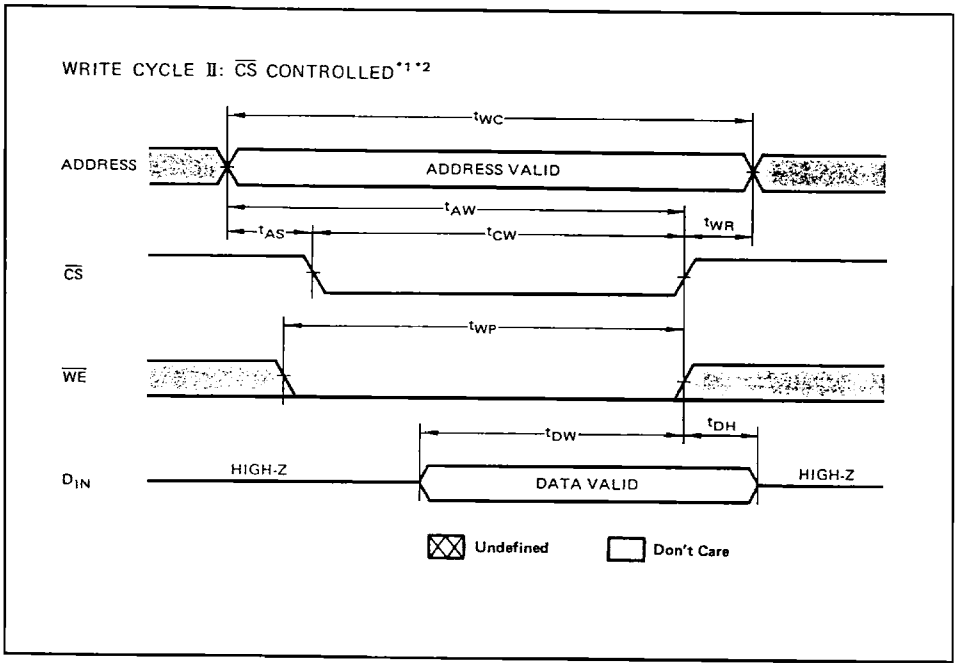
WRITE CYCLE TIMING DIAGRAM



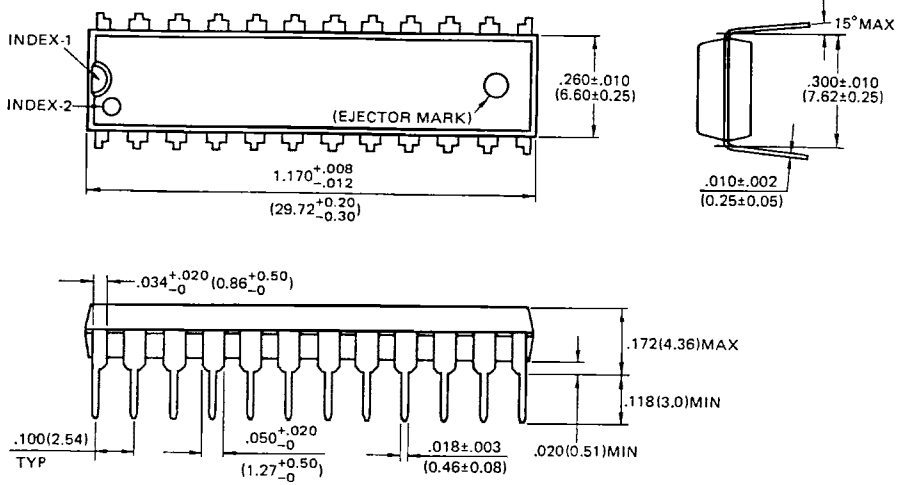
Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.

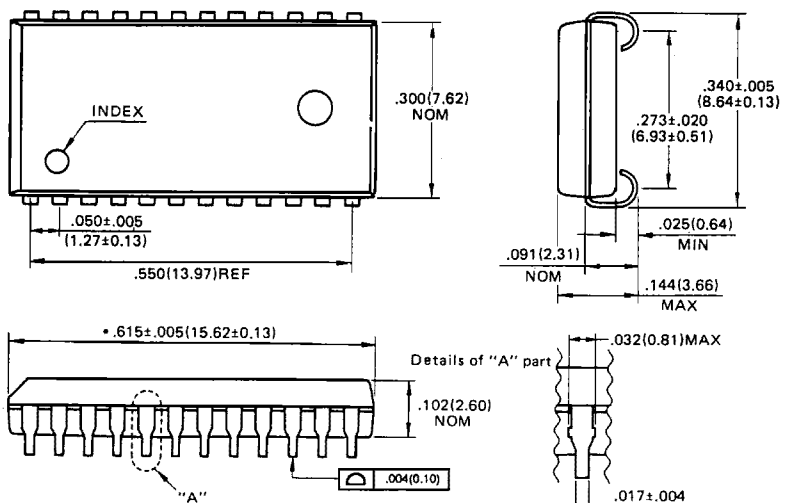
PACKAGE DIMENSIONS

24-LEADS PLASTIC DUAL-IN LINE PACKAGE
(CASE No.:DIP-24P-M03)



Dimensions in inches (millimeters)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

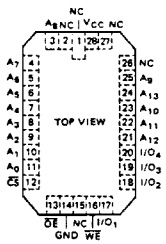


Dimensions in inches (millimeters)

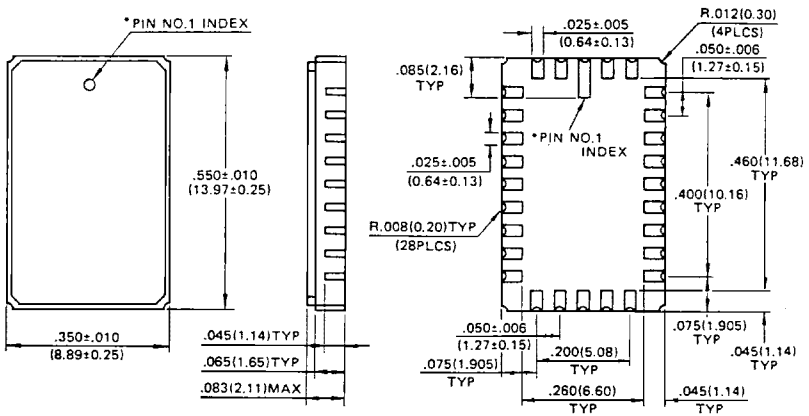
* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

PACKAGE DIMENSIONS

CERAMIC PACKAGE
LCC-28C-A03



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches
and (millimeters)