19-3802; Rev 2; 8/06

16-Channel Buffered CMOS Logic-Level Translators

General Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E 16-bit bidirectional CMOS logic-level translators provide the level shifting necessary to allow data transfer in multivoltage systems. These devices are inherently bidirectional due to their design and do not require the use of a direction input. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the devices. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when low, reduces the V_{CC} and V_L supply currents to less than 2µA. The MAX13108E features a multiplexing input (MULT) that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have ±15kV ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. Three different output configurations are available during shutdown, allowing the I/O on the V_{CC} side or the V_L side to be put in a high-impedance state or pulled to ground through an internal 6kΩ resistor.

The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept V_{CC} voltages from +1.65V to +5.5V and V_L voltages from +1.2V to V_{CC}, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are available in 36-bump UCSP™ and 40-pin TQFN packages, and operate over the extended -40°C to +85°C temperature range.

Applications

CMOS Logic-Level Translation

Portable Equipment

Cell Phones

PDAs

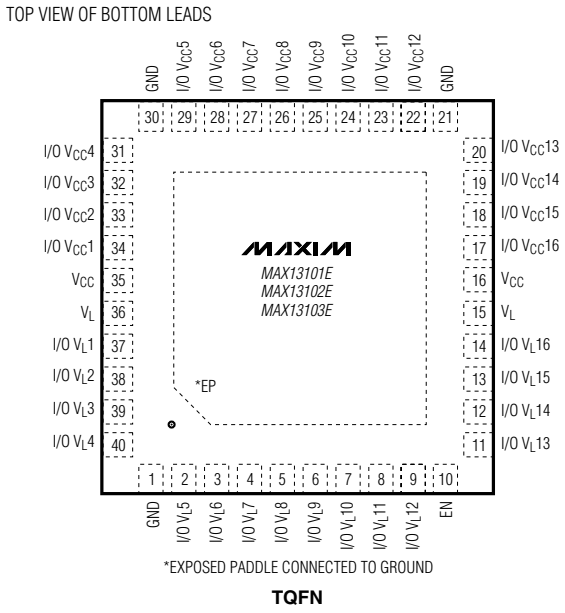
Digital Still Cameras

Smart Phones

Features

- **Wide Supply Voltage Range**
  V_{CC} Range of 1.65V to 5.5V
  V_L Range of 1.2V to V_{CC}
- **ESD Protection on I/O V_{CC} Lines**
  ±15kV Human Body Model
- **Up to 20Mbps Throughput**
- **Low 0.03µA Typical Quiescent Current**
- **UCSP and TQFN Packages**

Pin Configurations



Pin Configurations continued at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O V_L STATE DURING SHUTDOWN	I/O V_{CC} STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13101EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	6kΩ to GND	No	B36-1
MAX13101EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	6kΩ to GND	No	T4055-1

Note: All devices operate over the -40°C to +85°C operating temperature range.

**Future product—contact factory for availability.*

***UCSP bumps are in a 6 x 6 array.*

Ordering Information/Selector Guide continued at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

16-Channel Buffered CMOS Logic-Level Translators

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +6V
V_L.....-0.3V to +6V
I/O $V_{CC\_}$.....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$.....-0.3V to (V_L + 0.3V)
EN, MULT .....-0.3V to +6V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$ to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
36-Bump UCSP (derate 17.0mW/°C above +70°C) ..1361mW
40-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX13101E/MAX13102E/MAX13103E), MULT = V_L or GND (MAX13108E), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.2		V_{CC}	V
V_{CC} Supply Range	V_{CC}		1.65		5.50	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, EN = V_L, MULT = GND or V_L		0.03	10	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, EN = V_L, MULT = GND or V_L		0.03	20	µA
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = GND, I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND, MAX13101E/MAX13102E/MAX13103E		0.03	1	µA
V_L Shutdown Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = GND, I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND, MAX13101E/MAX13102E/MAX13103E		0.03	2	µA
I/O $V_{CC\_}$ Tri-State Output Leakage Current		T_A = +25°C, EN = GND, MAX13102E/MAX13103E		0.02	1	µA
		T_A = +25°C, MULT = GND (I/O V_{CC}1 - I/O V_{CC}8) or MULT = V_L (I/O V_{CC}9 - I/O V_{CC}16) MAX13108E		0.02	1	
I/O $V_{L\_}$ Tri-State Output Leakage Current		T_A = +25°C, EN = GND, MAX13101E/MAX13103E		0.02	1	µA
		T_A = +25°C, MULT = GND (I/O V_L1 - I/O V_L8) or MULT = V_L (I/OV_L9 - I/O V_L16) MAX13108E		0.02	1	
I/O $V_{L\_}$ Pulldown Resistance During Shutdown		EN = GND, MAX13102E	4		10	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX13101E/MAX13102E/MAX13103E), MULT = V_L or GND (MAX13108E), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Pulldown Resistance During Shutdown		EN = GND, MAX13101E	4		10	kΩ
EN or MULT Input Leakage Current		T_A = +25°C			1	µA
LOGIC-LEVEL THRESHOLDS						
I/O $V_{L\_}$ Input-Voltage High Threshold	V_{IHL}				2/3 x V_L	V
I/O $V_{L\_}$ Input-Voltage Low Threshold	V_{ILL}		1/3 x V_L			V
I/O $V_{CC\_}$ Input-Voltage High Threshold	V_{IHC}				2/3 x V_{CC}	V
I/O $V_{CC\_}$ Input-Voltage Low Threshold	V_{ILC}		1/3 x V_{CC}			V
EN, MULT Input-Voltage High Threshold	$V_{IH-SHDN}$				V_L - 0.4	V
EN, MULT Input-Voltage Low Threshold	$V_{IL-SHDN}$		0.4			V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA, I/O $V_{CC\_} \geq V_{IHC}$	V_L - 0.4			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA, I/O $V_{CC\_} \leq V_{ILC}$			0.4	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA, I/O $V_{L\_} \geq V_{IHL}$	V_{CC} - 0.4			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 20µA, I/O $V_{L\_} \leq V_{ILL}$			0.4	V
RISE/FALL-TIME ACCELERATOR STAGE						
Transition-Detect Threshold		I/O V_{CC} side		V_{CC} / 2		V
		I/O V_L side		V_L / 2		
Accelerator Pulse Duration		V_L = 1.2V, V_{CC} = 1.65V		20		ns
I/O $V_{L\_}$ Output-Accelerator Sink Impedance		V_L = 1.2V, V_{CC} = 1.65V		60		Ω
		V_L = 5V, V_{CC} = 5V		5		
I/O $V_{CC\_}$ Output-Accelerator Sink Impedance		V_L = 1.2V, V_{CC} = 1.65V		15		Ω
		V_L = 5V, V_{CC} = 5V		5		
I/O $V_{L\_}$ Output-Accelerator Source Impedance		V_L = 1.2V, V_{CC} = 1.65V		30		Ω
		V_L = 5V, V_{CC} = 5V		5		
I/O $V_{CC\_}$ Output-Accelerator Source Impedance		V_L = 1.2V, V_{CC} = 1.65V		20		Ω
		V_L = 5V, V_{CC} = 5V		7		
ESD PROTECTION						
I/O $V_{CC\_}$		Human Body Model		±15		kV

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX13101E/MAX13102E/MAX13103E), MULT = V_L or GND (MAX13108E), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V_L_ Rise Time	t_{RVL}	R_S = 50Ω, $C_{I/OVL\_}$ = 15pF, t_{RISE} ≤ 3ns, (Figures 2a, 2b)			15	ns
I/O V_L_ Fall Time	t_{FVL}	R_S = 50Ω, $C_{I/OVL\_}$ = 15pF, t_{FALL} ≤ 3ns, (Figures 2a, 2b)			15	ns
I/O V_{CC}_ Rise Time	t_{RVCC}	R_S = 50Ω, $C_{I/OVCC\_}$ = 50pF, t_{RISE} ≤ 3ns, (Figures 1a, 1b)			15	ns
I/O V_{CC}_ Fall Time	t_{FVCC}	R_S = 50Ω, $C_{I/OVCC\_}$ = 50pF, t_{FALL} ≤ 3ns, (Figures 1a, 1b)			15	ns
Propagation Delay (Driving I/O V_L_)	$t_{PVL-VCC}$	R_S = 50Ω, $C_{I/OVCC\_}$ = 50pF, t_{RISE} ≤ 3ns, (Figures 1a, 1b)			20	ns
Propagation Delay (Driving I/O V_{CC}_)	$t_{PVCC-VL}$	R_S = 50Ω, $C_{I/OVL\_}$ = 15pF, t_{RISE} ≤ 3ns, (Figures 2a, 2b)			20	ns
Channel-to-Channel Skew	t_{SKEW}	R_S = 50Ω, $C_{I/OVCC\_}$ = 50pF, $C_{I/OVL\_}$ = 15pF, t_{RISE} ≤ 3ns			5	ns
Part-to-Part Skew	t_{PPSKEW}	R_S = 50Ω, $C_{I/OVCC\_}$ = 50pF, $C_{I/OVL\_}$ = 15pF, t_{RISE} ≤ 3ns, ΔT_A = +20°C (Notes 3, 4)			10	ns
Propagation Delay from I/O V_L_ to I/O V_{CC}_ After EN	t_{EN-VCC}	$C_{I/OVCC\_}$ = 50pF (Figure 3)			1	µs
Propagation Delay from I/O V_{CC}_ to I/O V_L_ After EN	t_{EN-VL}	$C_{I/OVL\_}$ = 15pF (Figure 4)			1	µs
Maximum Data Rate		R_{SOURCE} = 50Ω, $C_{I/OVCC\_}$ = 50pF, $C_{I/OVL\_}$ = 15pF, t_{RISE} ≤ 3ns	20			Mbps

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: For normal operation, ensure that V_L < (V_{CC} + 0.3V). During power-up, V_L > (V_{CC} + 0.3V) does not damage the device.

Note 3: V_{CC} from device 1 must equal V_{CC} of device 2. V_L from device 1 must equal V_L of device 2.

Note 4: Guaranteed by design, not production tested.

Test Circuits/Timing Diagrams

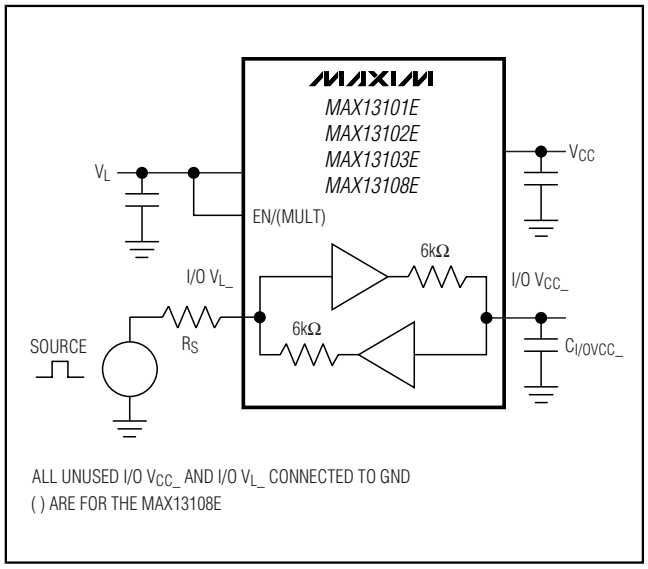


Figure 1a. Driving I/O $V_{L\_}$

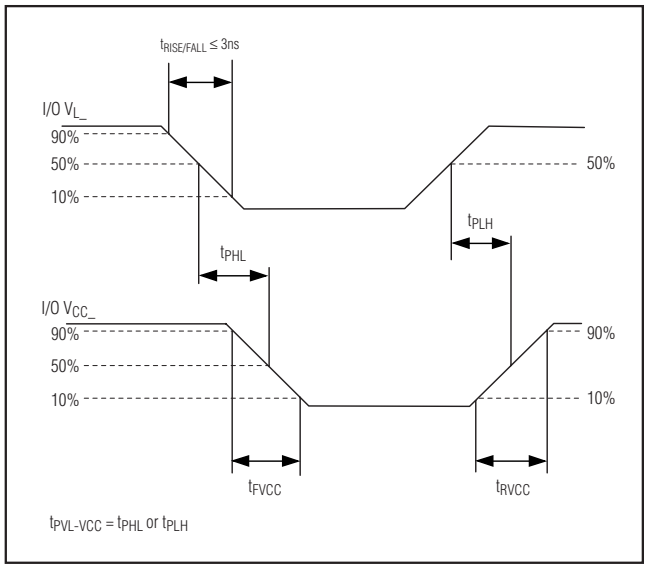


Figure 1b. Timing for Driving I/O $V_{L\_}$

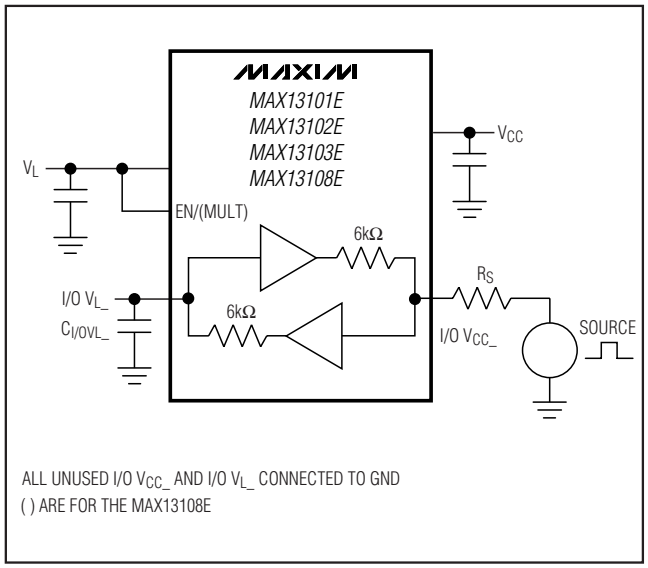


Figure 2a. Driving I/O $V_{CC\_}$

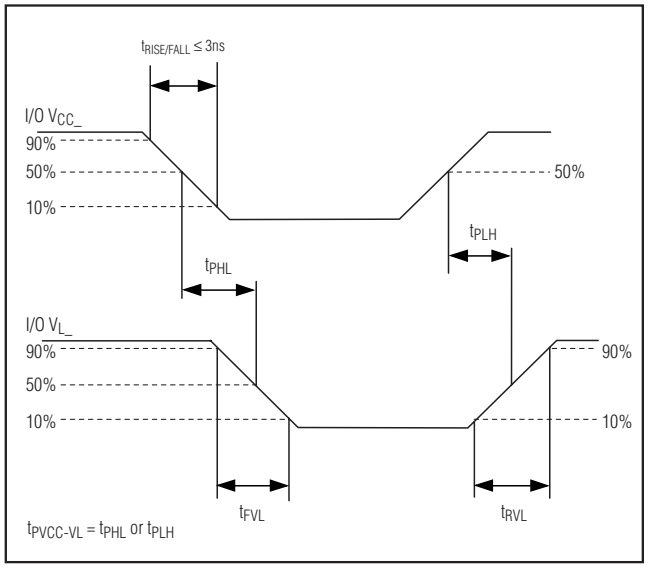


Figure 2b. Timing for Driving I/O $V_{CC\_}$

Test Circuits/Timing Diagrams (continued)

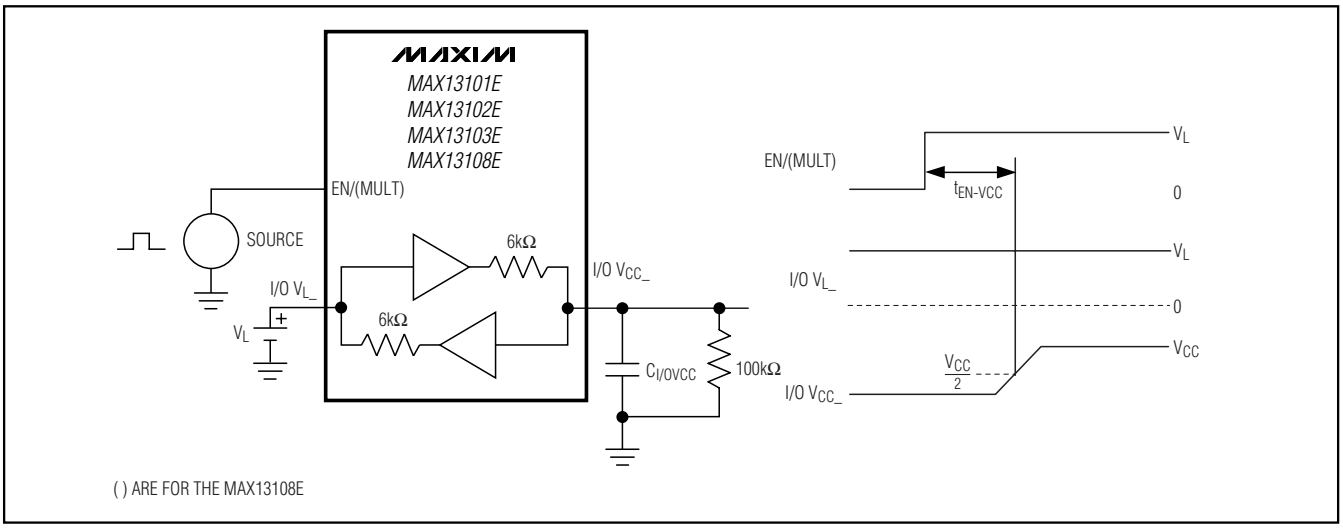


Figure 3. Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ After EN

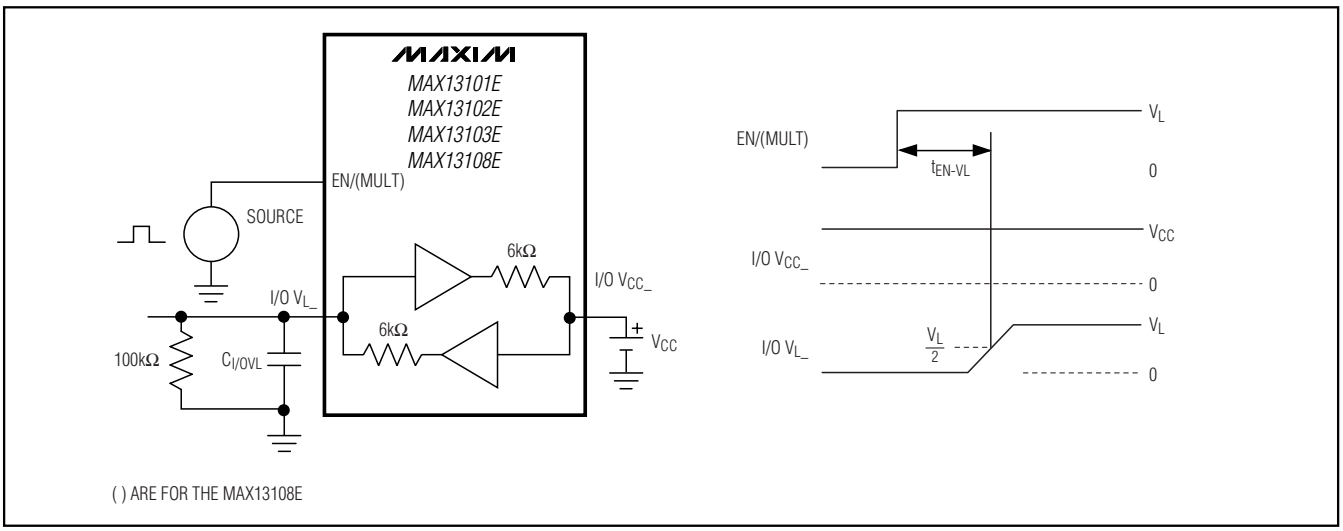
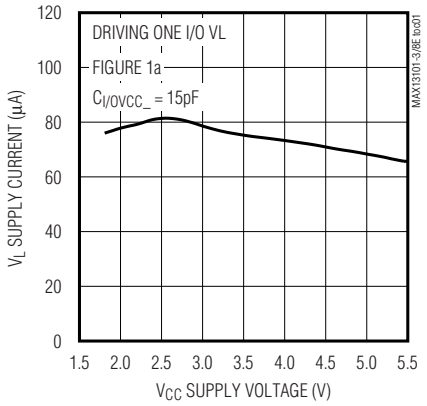


Figure 4. Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ After EN

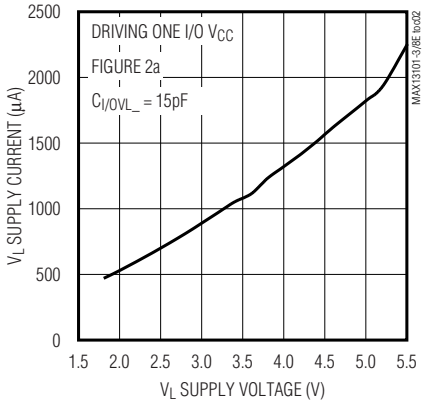
Typical Operating Characteristics

(V_{CC} = 3.3V, V_L = 1.8V, data rate = 20Mbps, T_A = +25°C, unless otherwise noted.)

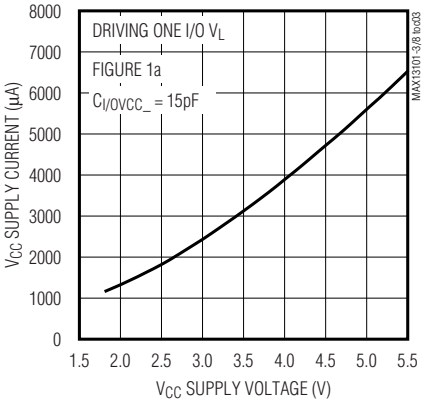
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING I/O V_L_, V_L = 1.8V)



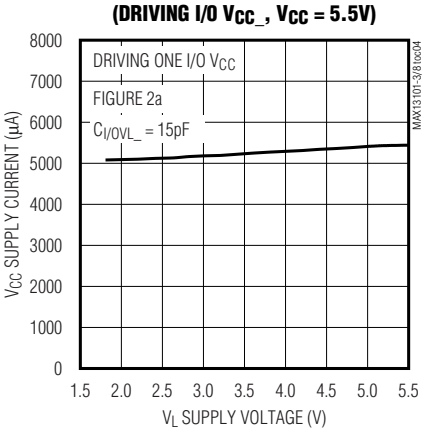
V_L SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING I/O V_{CC}_, V_{CC} = 5.5V)



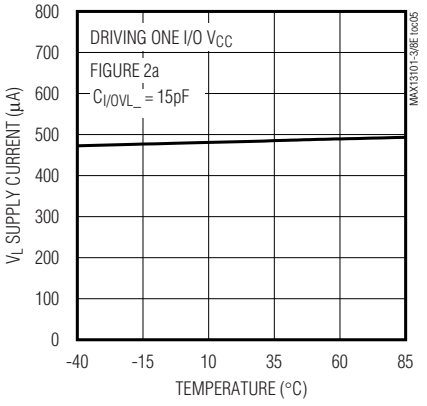
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING I/O V_L_, V_L = 1.8V)



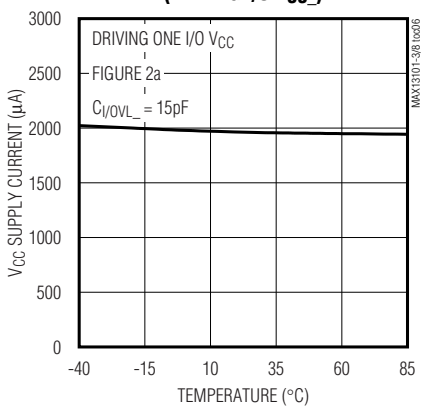
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING I/O V_{CC}_, V_{CC} = 5.5V)



V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}_)



V_{CC} SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}_)

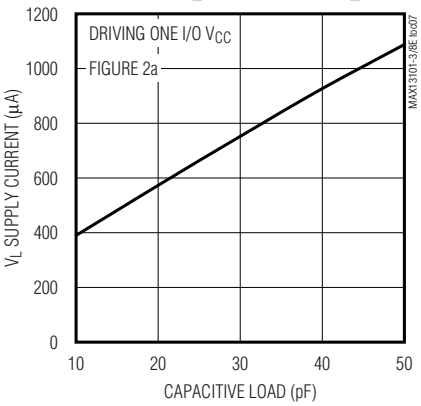


16-Channel Buffered CMOS Logic-Level Translators

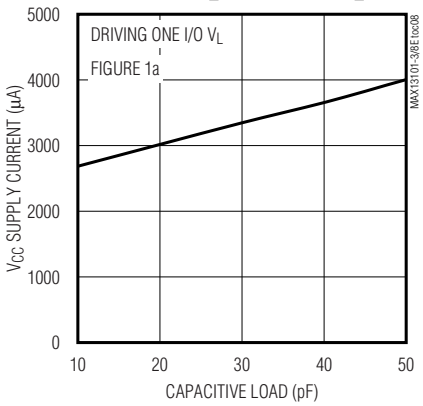
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_L = 1.8V, data rate = 20Mbps, T_A = +25°C, unless otherwise noted.)

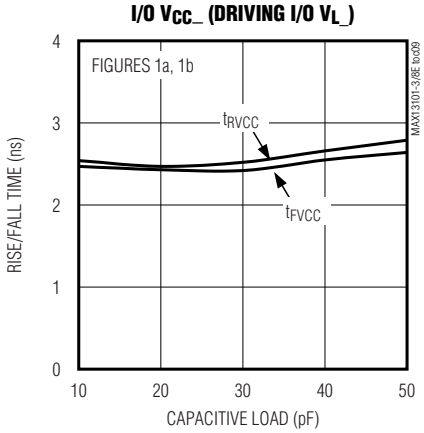
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)



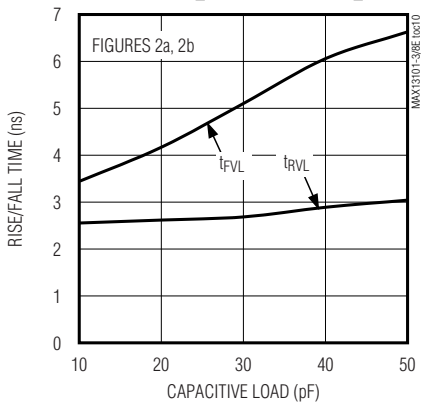
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



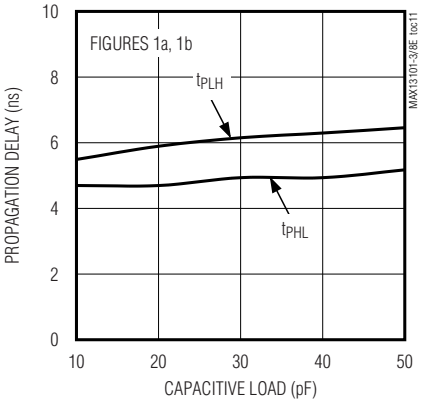
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)



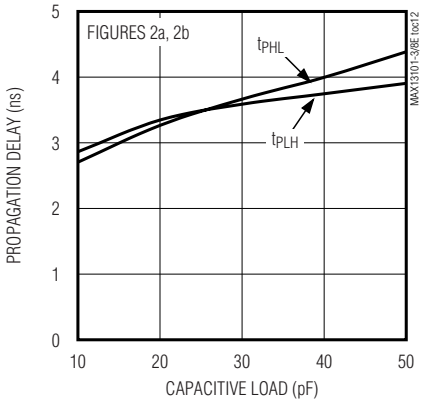
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



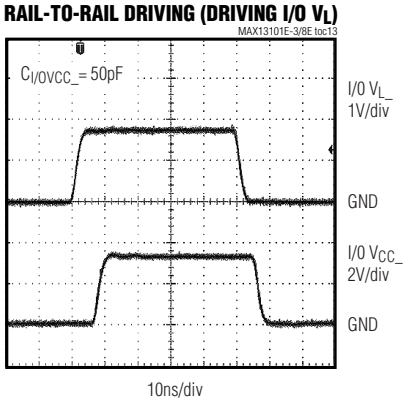
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_L = 1.8V, data rate = 20Mbps, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L_ (DRIVING I/O V_{CC}_)



RAIL-TO-RAIL DRIVING (DRIVING I/O V_L)



Pin Description—MAX13101E/MAX13102E/MAX13103E

PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O V_L5	Input/Output 5. Referenced to V_L.
3	A3	I/O V_L6	Input/Output 6. Referenced to V_L.
4	B3	I/O V_L7	Input/Output 7. Referenced to V_L.
5	C3	I/O V_L8	Input/Output 8. Referenced to V_L.
6	A4	I/O V_L9	Input/Output 9. Referenced to V_L.
7	B4	I/O V_L10	Input/Output 10. Referenced to V_L.
8	C4	I/O V_L11	Input/Output 11. Referenced to V_L.
9	A5	I/O V_L12	Input/Output 12. Referenced to V_L.
10	C6	EN	Global Enable Input. Pull EN low for shutdown. Drive EN to V_{CC} or V_L for normal operation.
11	B5	I/O V_L13	Input/Output 13. Referenced to V_L.
12	C5	I/O V_L14	Input/Output 14. Referenced to V_L.
13	A6	I/O V_L15	Input/Output 15. Referenced to V_L.
14	B6	I/O V_L16	Input/Output 16. Referenced to V_L.
15, 36	A1	V_L	Logic Supply Voltage, +1.2V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
16, 35	F1	V_{CC}	V_{CC} Supply Voltage, +1.65V ≤ V_{CC} ≤ +5.5V. Bypass V_{CC} to GND with a 0.1µF capacitor. For full ESD protection, connect a 1.0µF capacitor from V_{CC} to GND, located as close to the V_{CC} input as possible.
17	E6	I/O V_{CC}16	Input/Output 16. Referenced to V_{CC}.
18	F6	I/O V_{CC}15	Input/Output 15. Referenced to V_{CC}.

Pin Description—MAX13101E/MAX13102E/MAX13103E (continued)

PIN		NAME	FUNCTION
TQFN	UCSP		
19	D5	I/O V_{CC}14	Input/Output 14. Referenced to V_{CC}.
20	E5	I/O V_{CC}13	Input/Output 13. Referenced to V_{CC}.
22	F5	I/O V_{CC}12	Input/Output 12. Referenced to V_{CC}.
23	D4	I/O V_{CC}11	Input/Output 11. Referenced to V_{CC}.
24	E4	I/O V_{CC}10	Input/Output 10. Referenced to V_{CC}.
25	F4	I/O V_{CC}9	Input/Output 9. Referenced to V_{CC}.
26	D3	I/O V_{CC}8	Input/Output 8. Referenced to V_{CC}.
27	E3	I/O V_{CC}7	Input/Output 7. Referenced to V_{CC}.
28	F3	I/O V_{CC}6	Input/Output 6. Referenced to V_{CC}.
29	D2	I/O V_{CC}5	Input/Output 5. Referenced to V_{CC}.
31	E2	I/O V_{CC}4	Input/Output 4. Referenced to V_{CC}.
32	F2	I/O V_{CC}3	Input/Output 3. Referenced to V_{CC}.
33	D1	I/O V_{CC}2	Input/Output 2. Referenced to V_{CC}.
34	E1	I/O V_{CC}1	Input/Output 1. Referenced to V_{CC}.
37	B1	I/O V_L1	Input/Output 1. Referenced to V_L.
38	C1	I/O V_L2	Input/Output 2. Referenced to V_L.
39	A2	I/O V_L3	Input/Output 3. Referenced to V_L.
40	B2	I/O V_L4	Input/Output 4. Referenced to V_L.
EP	—	EP	Exposed Paddle. Connect EP to GND.

Pin Description—MAX13108E

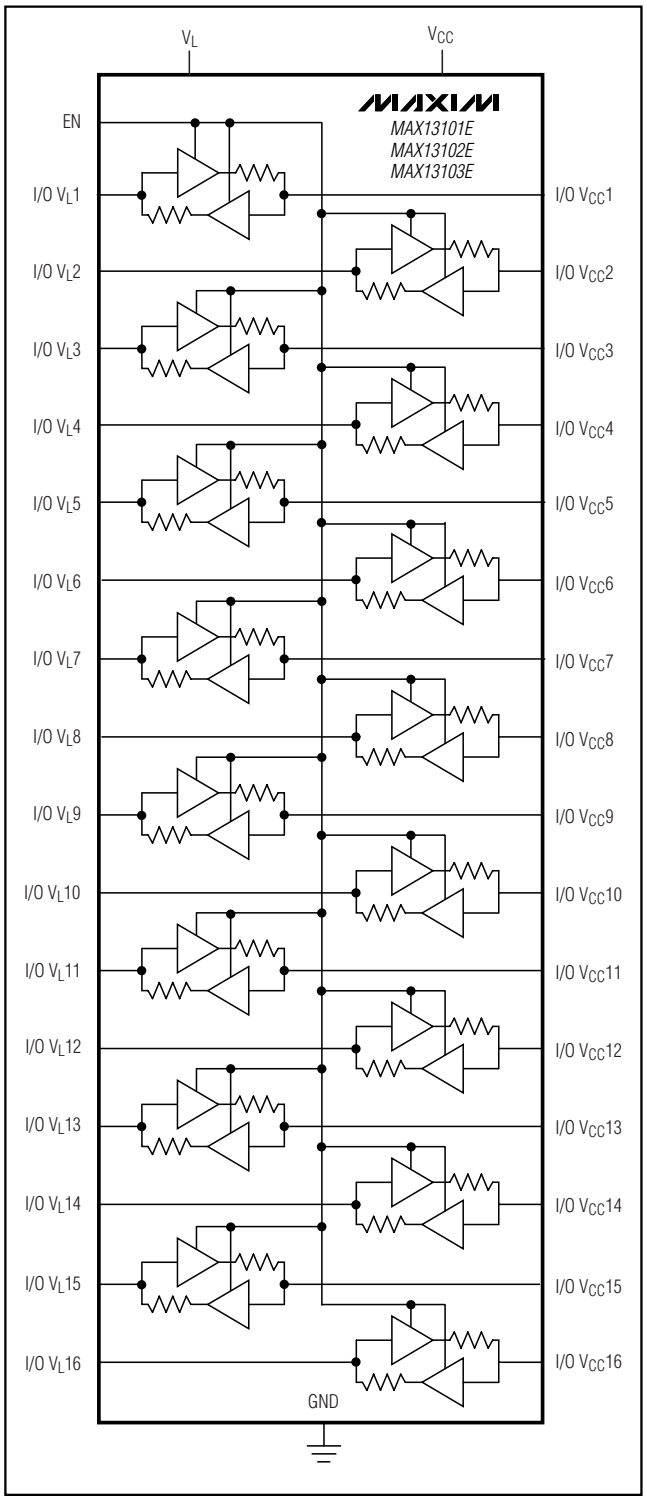
PIN		NAME	FUNCTION
TQFN	UCSP		
1, 21, 30	D6	GND	Ground
2	C2	I/O V_L5	Input/Output 5. Referenced to V_L.
3	A3	I/O V_L6	Input/Output 6. Referenced to V_L.
4	B3	I/O V_L7	Input/Output 7. Referenced to V_L.
5	C3	I/O V_L8	Input/Output 8. Referenced to V_L.
6	A4	I/O V_L9	Input/Output 9. Referenced to V_L.
7	B4	I/O V_L10	Input/Output 10. Referenced to V_L.
8	C4	I/O V_L11	Input/Output 11. Referenced to V_L.
9	A5	I/O V_L12	Input/Output 12. Referenced to V_L.

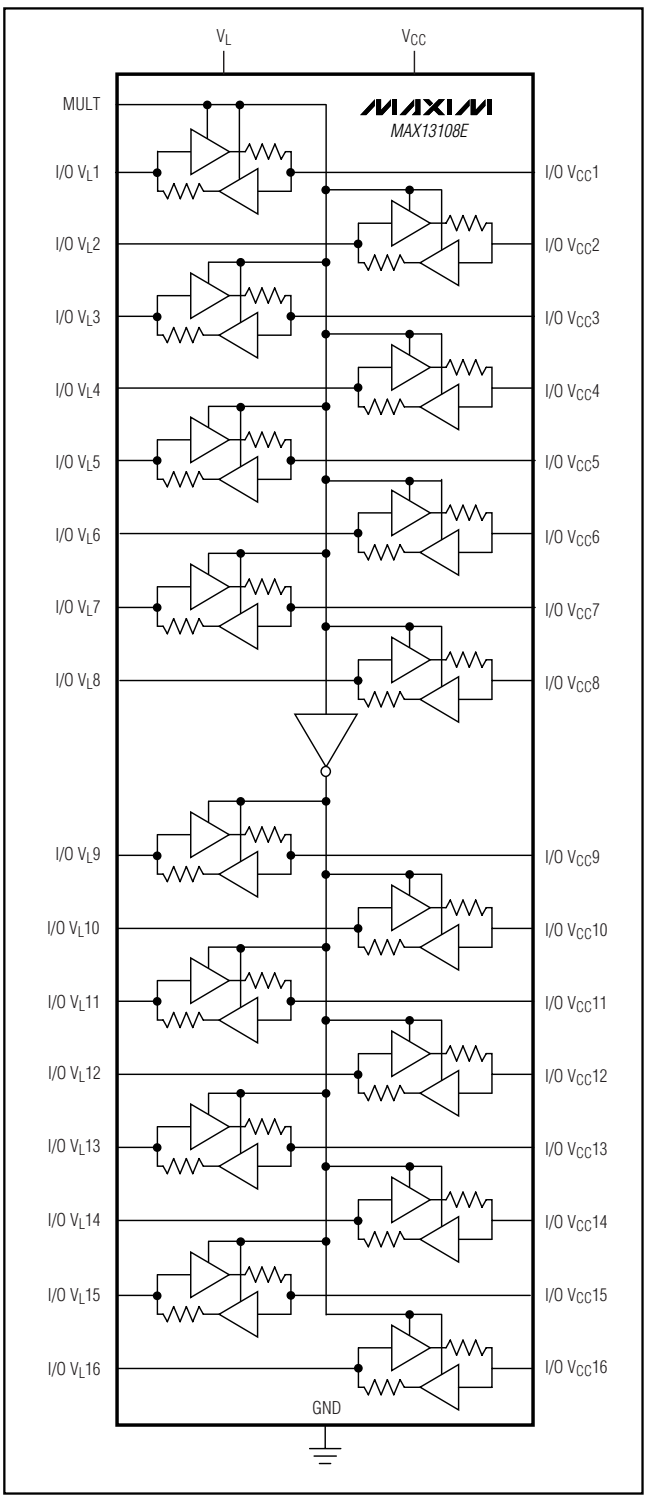
Pin Description—MAX13108E (continued)

PIN		NAME	FUNCTION
TQFN	UCSP		
10	C6	MULT	Multiplexing Input. Drive MULT low to enable channels 9 to 16. Driving MULT low puts channels 1 to 8 into tri-state. Drive MULT to V_{CC} or V_L to enable channels 1 to 8. Driving MULT to V_{CC} or V_L puts channels 9 to 16 into tri-state.
11	B5	I/O V_L13	Input/Output 13. Referenced to V_L.
12	C5	I/O V_L14	Input/Output 14. Referenced to V_L.
13	A6	I/O V_L15	Input/Output 15. Referenced to V_L.
14	B6	I/O V_L16	Input/Output 16. Referenced to V_L.
15, 36	A1	V_L	Logic Supply Voltage, $+1.2V \le V_L \le V_{CC}$. Bypass V_L to GND with a 0.1µF capacitor.
16, 35	F1	V_{CC}	V_{CC} Supply Voltage, $+1.65V \le V_{CC} \le +5.5V$. Bypass V_{CC} to GND with a 0.1µF capacitor. For full ESD protection, connect a 1.0µF capacitor from V_{CC} to GND, located as close to the V_{CC} input as possible.
17	E6	I/O V_{CC}16	Input/Output 16. Referenced to V_{CC}.
18	F6	I/O V_{CC}15	Input/Output 15. Referenced to V_{CC}.
19	D5	I/O V_{CC}14	Input/Output 14. Referenced to V_{CC}.
20	E5	I/O V_{CC}13	Input/Output 13. Referenced to V_{CC}.
22	F5	I/O V_{CC}12	Input/Output 12. Referenced to V_{CC}.
23	D4	I/O V_{CC}11	Input/Output 11. Referenced to V_{CC}.
24	E4	I/O V_{CC}10	Input/Output 10. Referenced to V_{CC}.
25	F4	I/O V_{CC}9	Input/Output 9. Referenced to V_{CC}.
26	D3	I/O V_{CC}8	Input/Output 8. Referenced to V_{CC}.
27	E3	I/O V_{CC}7	Input/Output 7. Referenced to V_{CC}.
28	F3	I/O V_{CC}6	Input/Output 6. Referenced to V_{CC}.
29	D2	I/O V_{CC}5	Input/Output 5. Referenced to V_{CC}.
31	E2	I/O V_{CC}4	Input/Output 4. Referenced to V_{CC}.
32	F2	I/O V_{CC}3	Input/Output 3. Referenced to V_{CC}.
33	D1	I/O V_{CC}2	Input/Output 2. Referenced to V_{CC}.
34	E1	I/O V_{CC}1	Input/Output 1. Referenced to V_{CC}.
37	B1	I/O V_L1	Input/Output 1. Referenced to V_L.
38	C1	I/O V_L2	Input/Output 2. Referenced to V_L.
39	A2	I/O V_L3	Input/Output 3. Referenced to V_L.
40	B2	I/O V_L4	Input/Output 4. Referenced to V_L.
EP	—	EP	Exposed Paddle. Connect EP to GND.

16-Channel Buffered CMOS Logic-Level Translators

Functional Diagrams





Detailed Description

The MAX13101E/MAX13102E/MAX13103E/MAX13108E logic-level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are bidirectional level translators allowing data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept V_L from +1.2V to V_{CC}. All devices have a V_{CC} range from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13101E/MAX13102E/MAX13103E feature an output enable mode that reduces V_{CC} supply current to less than 1µA, and V_L supply current to less than 2µA when in shutdown. The MAX13108E features a multiplexing input that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have ±15kV ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. The MAX13101E/MAX13102E/MAX13103E/MAX13108E operate at a guaranteed data rate of 20Mbps. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics*) and the output impedance of the external driver.

Power-Supply Sequencing

For proper operation, ensure that $+1.65V \le V_{CC} \le +5.5V$, $+1.2V \le V_L \le +5.5V$, and $V_L \le V_{CC}$. During power-up sequencing, $V_L \ge V_{CC}$ does not damage the device. When V_{CC} is disconnected and V_L is powering up, up to 10mA of current can be sourced to each load on the V_L side, yet the device does not latch up. To guarantee that no excess leakage current flows and that the device does not interfere with the I/O on the V_L side, V_{CC} should be connected to GND with a max 50Ω resistor when the V_{CC} supply is not present (Figure 5).

Input Driver Requirements

The MAX13101E/MAX13102E/MAX13103E/MAX13108E architecture is based on a one-shot accelerator output stage (Figure 6). Accelerator output stages are always in tri-state except when there is a transition on any of the translators on the input side, either I/O $V_{L\_}$ or I/O $V_{CC\_}$. Then a short pulse is generated, during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to the bidirectional nature, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

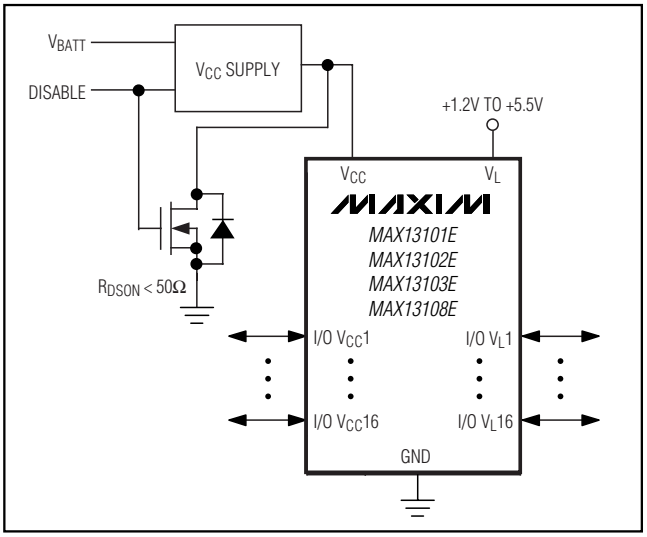


Figure 5. Recommended Circuit for Powering Down V_{CC}

For proper full-speed operation, the output current of a device that drives the inputs of the MAX13101E/MAX13102E/MAX13103E/MAX13108E should meet the following requirement:

$$i > 10^8 \times V \times (C + 10pF)$$

where, i is the driver output current, V is the logic-supply voltage (i.e., V_L or V_{CC}) and C is the parasitic capacitance of the signal line.

Enable Output Mode (EN)

The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when driven low, places the device into shutdown mode. During shutdown, the MAX13101E I/O $V_{CC\_}$ ports are pulled down to ground with internal 6kΩ resistors and the I/O $V_{L\_}$ ports enter tri-state. MAX13102E I/O $V_{CC\_}$ lines enter tri-state and the I/O$V_{L_}$ lines are pulled down to ground with internal 6kΩ resistors. All I/O $V_{CC\_}$ and I/O $V_{L\_}$ lines on the MAX13103E enter tri-state while the device is in shutdown mode. During shutdown, the V_{CC} supply current reduces to less than 1µA, and the V_L supply current reduces to less than 2µA. To guarantee minimum shutdown supply current, all I/O $V_{L\_}$ need to be driven to GND or V_L, or pulled to GND or V_L through 100kΩ resistors. All I/O $V_{CC\_}$ need to be driven to GND or V_{CC}, or pulled to GND or V_{CC} through 100kΩ resistors. Drive EN to logic-high (V_L or V_{CC}) for normal operation.

16-Channel Buffered CMOS Logic-Level Translators

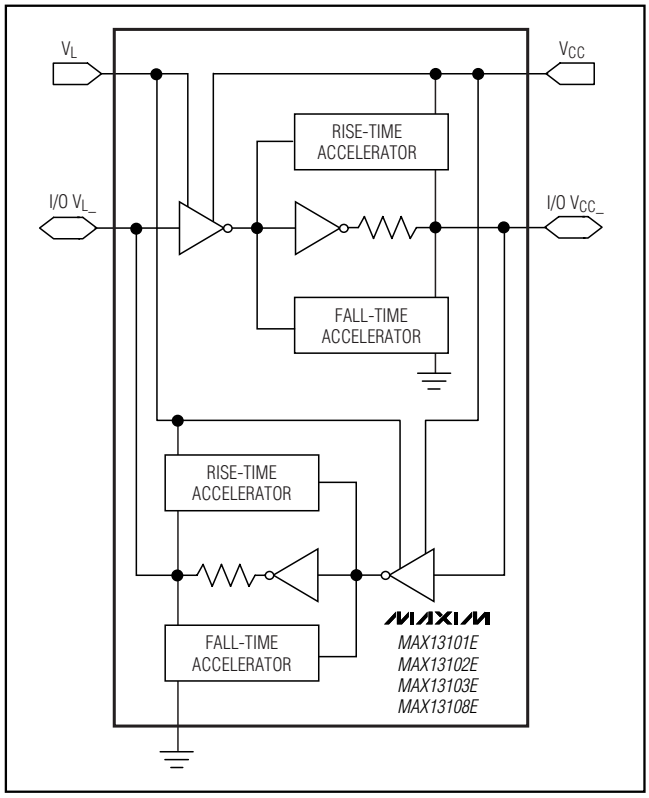


Figure 6. Simplified Diagram (1 I/O Line)

Multiplexing Input (MULT)

The MAX13108E features a multiplexing input (MULT) that enables 8 of the 16 channels and places the remaining 8 into tri-state. Figure 7 depicts a typical multiplexing configuration using the MAX13108E. Drive MULT high to enable I/O $V_{CC}1$ through I/O $V_{CC}8$ and I/O V_L1 through I/O V_L8. Driving MULT high sets I/O $V_{CC}9$ through I/O $V_{CC}16$ and I/O V_L9 through I/O V_L16 into tri-state. Drive MULT low to enable I/O $V_{CC}9$ through I/O $V_{CC}16$ and I/O V_L9 through I/O V_L16. Driving MULT low sets I/O $V_{CC}1$ through I/O $V_{CC}8$ and I/O V_L1 through I/O V_L8 into tri-state.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V_{CC}_ lines have extra protection against static discharge. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, tri-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove the latchup condition.

ESD protection can be tested in various ways. The I/O V_{CC}_ lines of the MAX13101E/ MAX13102E/ MAX13103E/MAX13108E are characterized for protection to ±15kV using the Human Body Model.

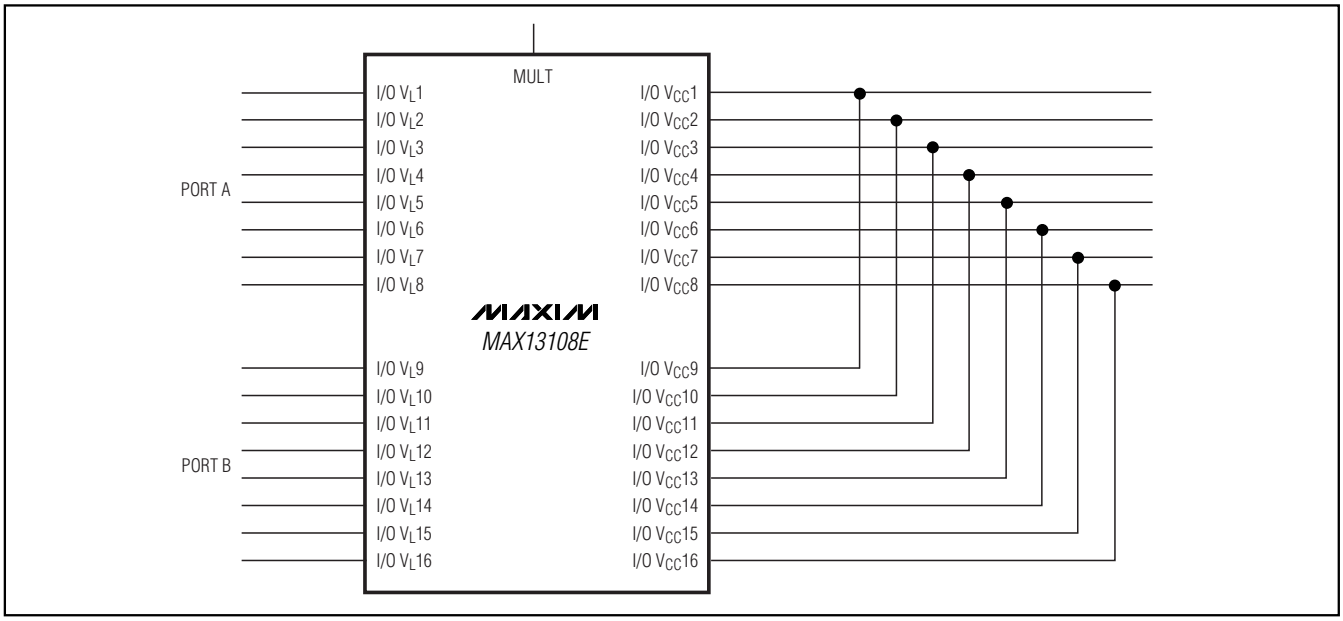


Figure 7. MAX13108E Multiplexing Configuration

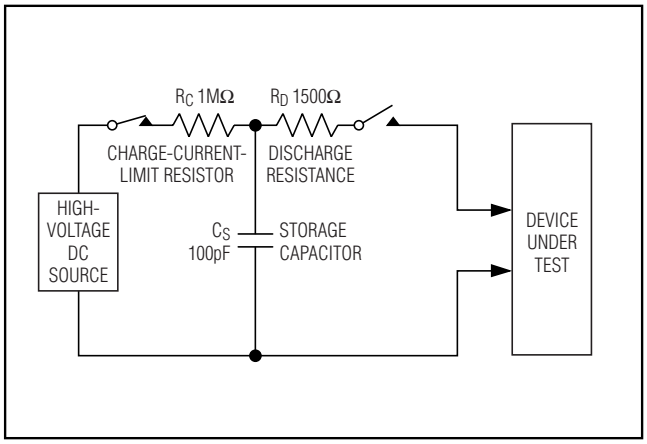


Figure 8a. Human Body ESD Test Model

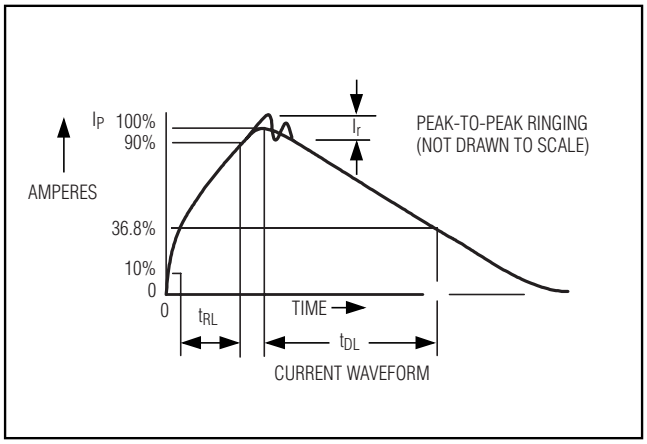


Figure 8b. Human Body Model Current Waveform

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8a shows the Human Body Model and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with 0.1µF capacitors. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF ceramic capacitor. Place all capacitors as close to the power-supply inputs as possible.

Capacitive Loading

Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13101E/MAX13102E/MAX13103E/MAX13108E when driving the signal lines. The actual rise time is a function of the parasitic capacitance, the supply voltage, and the drive impedance of the MAX13101E/MAX13102E/MAX13103E/MAX13108E. For proper operation, the signal must reach the V_{OH} as required before the rise-time accelerators turn off.

16-Channel Buffered CMOS Logic-Level Translators

Ordering Information/Selector Guide (continued)

PART	PIN-PACKAGE	DATA RATE (Mbps)	I/O V_L STATE DURING SHUTDOWN	I/O V_{CC} STATE DURING SHUTDOWN	MULTIPLEXER FEATURE	PKG CODE
MAX13102EEBX*	36 UCSP** 3.06mm x 3.06mm	20	6kΩ to GND	High impedance	No	B36-1
MAX13102EETL	40 TQFN 5mm x 5mm x 0.8mm	20	6kΩ to GND	High impedance	No	T4055-1
MAX13103EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	No	B36-1
MAX13103EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	No	T4055-1
MAX13108EEBX*	36 UCSP** 3.06mm x 3.06mm	20	High impedance	High impedance	Yes	B36-1
MAX13108EETL	40 TQFN 5mm x 5mm x 0.8mm	20	High impedance	High impedance	Yes	T4055-1

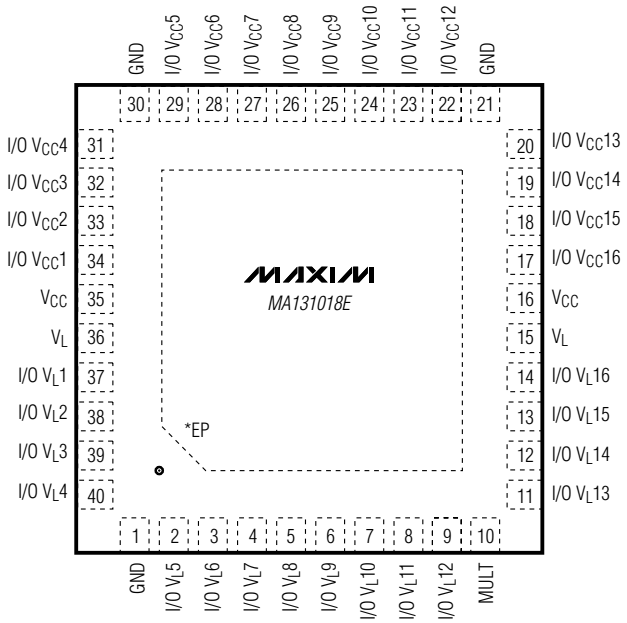
Note: All devices operate over the -40°C to +85°C operating temperature range.

**Future Product—contact factory for availability.*

***UCSP bumps are in a 6 x 6 array.*

Pin Configurations (continued)

TOP VIEW OF BOTTOM LEADS

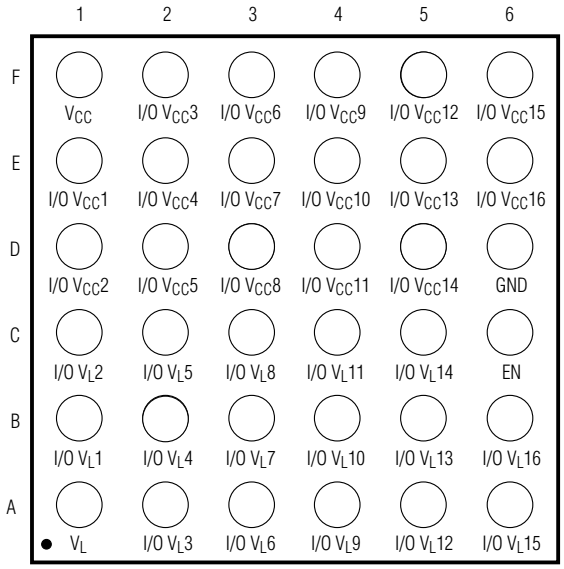


* EXPOSED PADDLE CONNECTED TO GROUND

TQFN

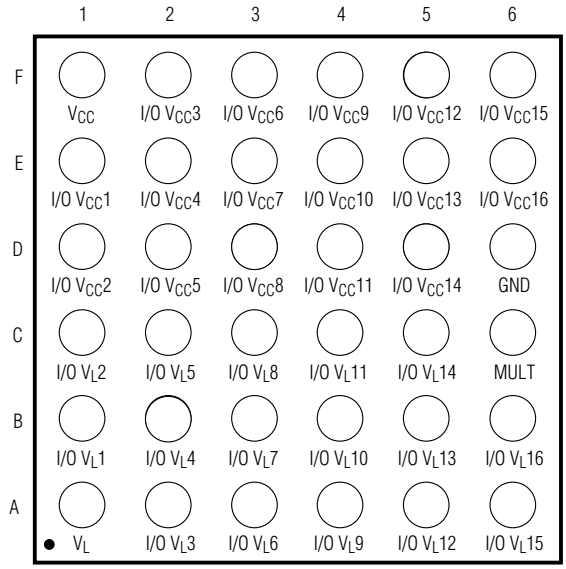
Pin Configurations (continued)

MAXIM
MAX13101E/MAX13102E/MAX13103E



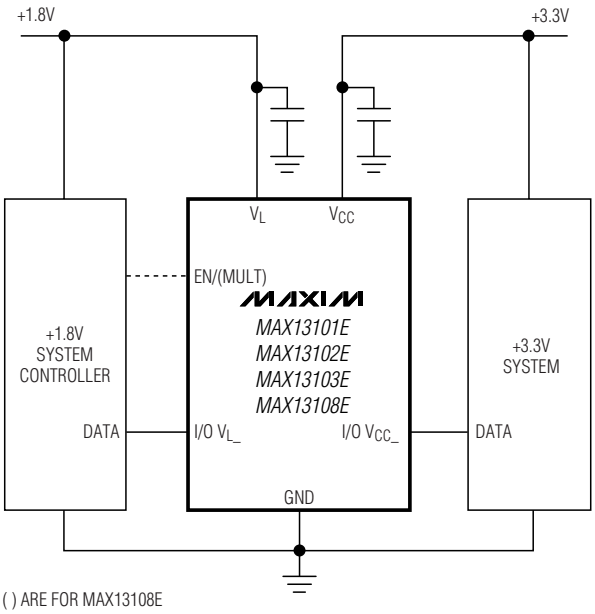
UCSP
(BOTTOM VIEW)

MAXIM
MAX13108E



UCSP
(BOTTOM VIEW)

Typical Operating Circuit



( ) ARE FOR MAX13108E

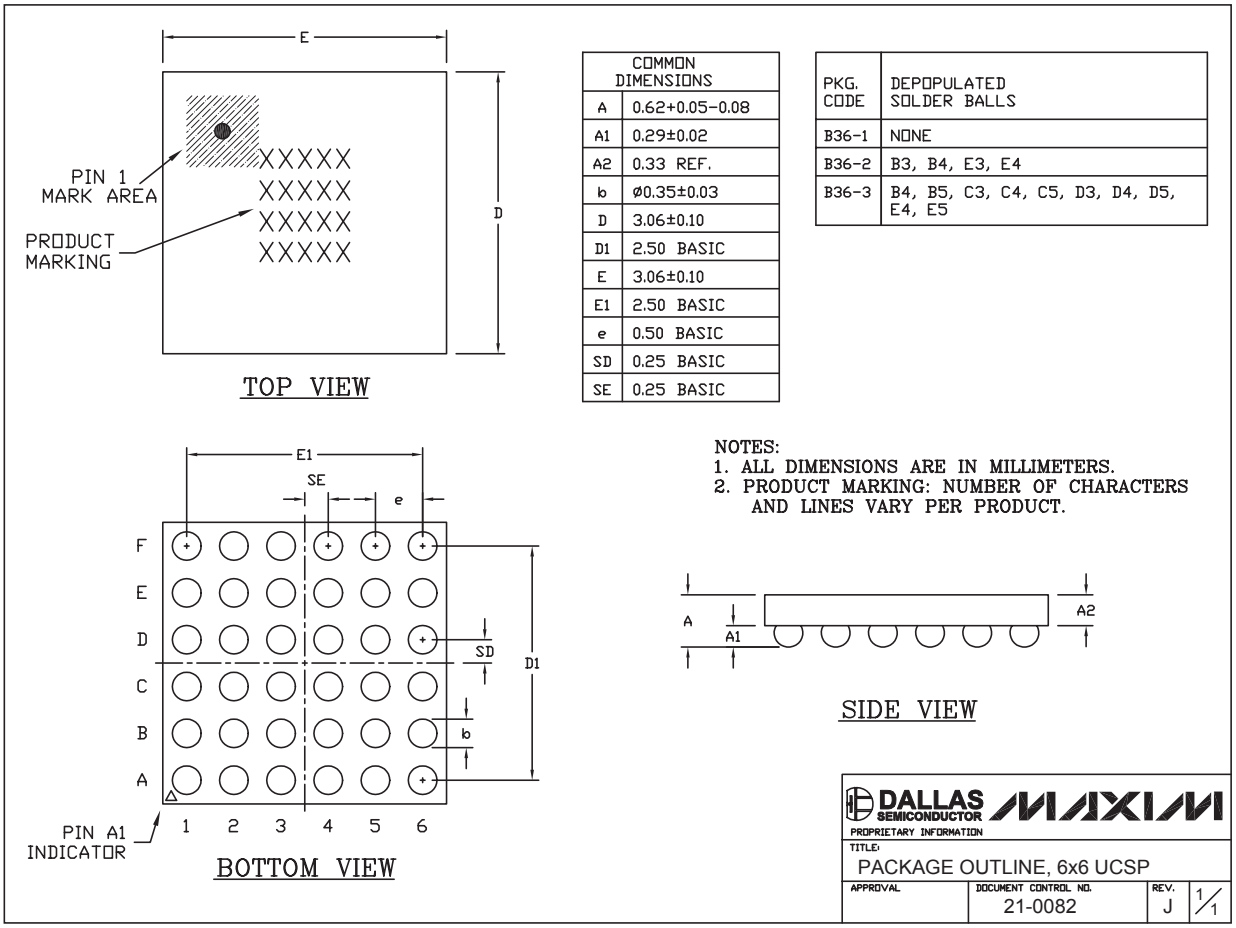
Chip Information

PROCESS: BiCMOS

16-Channel Buffered CMOS Logic-Level Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D	3.06±0.10
D1	2.50 BASIC
E	3.06±0.10
E1	2.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	DEPOPULATED SOLDER BALLS
B36-1	NONE
B36-2	B3, B4, E3, E4
B36-3	B4, B5, C3, C4, C5, D3, D4, D5, E4, E5

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

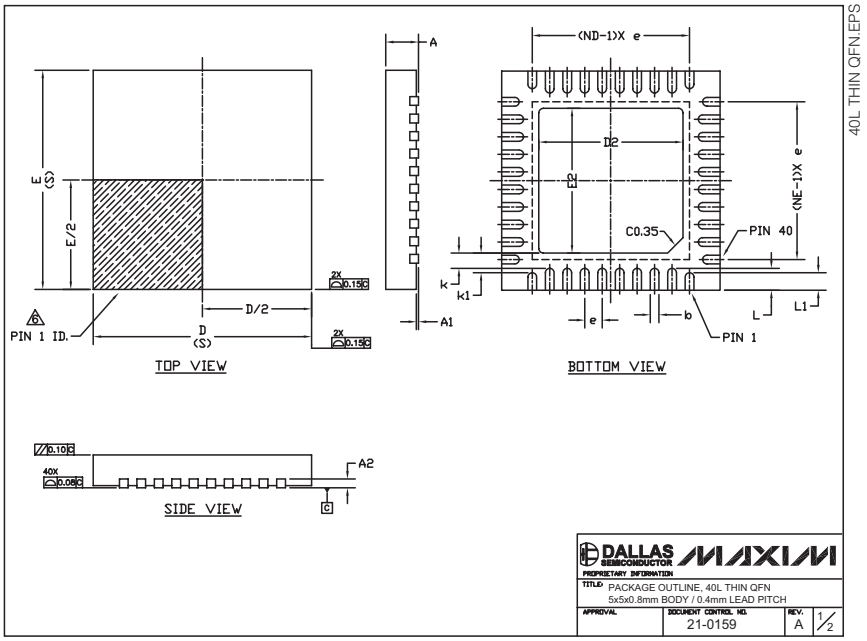
DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 6x6 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0082	J	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTICS. (S)
5. REFER TO JEDEC MO-220.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

	COMMON DIMENSIONS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.700	0.750	0.800
A1	0.000	-- --	0.050
A2		0.200 REF.	
b	0.150	0.200	0.250
D	4.900	5.000	5.100
e		0.400 TYP.	
E	4.900	5.000	5.100
k	0.250	0.350	0.450
k1	0.350	0.450	0.550
L	0.400	0.500	0.600
L1	0.300	0.400	0.500
N		40	
ND		10	
NE		10	

	EXPOSED PAD VARIATONS					
PKG. CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 40L THIN QFN
5x5x0.8mm BODY / 0.4mm LEAD PITCH
APPROVAL
DOCUMENT CONTROL NO. 21-0159
REV. A
2/2

MAX13101E, MAX13102E, MAX13103E, MAX13108E

16-Channel Buffered CMOS Logic-Level Translators

QuickView | Technical Documents | Ordering Info | More Information | All

Ordering Information

Notes:

1. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
2. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
3. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: SeeFull Data Sheet or Part Naming Conventions.
4. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Devices: 1-14 of 14

MAX13101E	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX13101EETL+T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13101EETL+			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13101EETL			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX13101EETL-T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX13102E	**Free Sample**	**Buy**	**Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR ***	**Temp**	**RoHS/Lead-Free? Materials Analysis**
MAX13102EETL+T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13102EETL+			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13103E	**Free Sample**	**Buy**	**Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR ***	**Temp**	**RoHS/Lead-Free? Materials Analysis**
MAX13103EETL+T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13103EETL+			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13103EETL-T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX13103EETL			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX13108E	**Free Sample**	**Buy**	**Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR ***	**Temp**	**RoHS/Lead-Free? Materials Analysis**

MAX13108EETL+			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13108EETL+T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055+1*	-40C to +85C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX13108EETL-T			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis
MAX13108EETL			THIN QFN;40 pin;26 mm Dwg: 21-0140L (PDF) Use pkgcode/variation: T4055-1*	-40C to +85C	RoHS/Lead-Free: No Materials Analysis

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