DESCRIPTION

The HY62U8100B is a high speed, low power and 1M bit CMOS SRAM organized as 131,072 words by 8bit. The HY62U8100B uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particulary well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

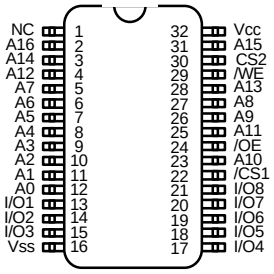
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
  -. 2.0V(min) data retention
- Standard pin configuration
  -. 32 - SOP - 525mil
  -. 32 - TSOP-I - 8X20(Standard and Reversed)
  -. 32 - sTSOP-I - 8X13.4
  (Standard and Reversed)

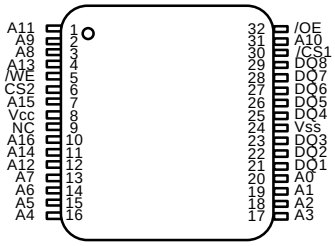
Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA) LL	Temperature (°C)
HY62U8100B	2.7~3.3	85/100/120	5	10	0~70
HY62U8100B-E	2.7~3.3	85/100/120	5	15	-25~85(E)
HY62U8100B-I	2.7~3.3	85/100/120	5	15	-40~85(I)

Note 1. Blank : Commercial, E : Extended, I : Industrial
2. Current value is max.

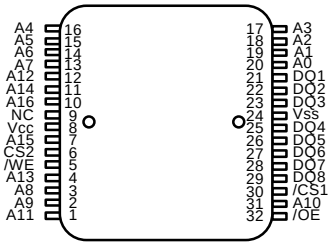
PIN CONNECTION



SOP



sTSOP-I / TSOP-I
(Standard)

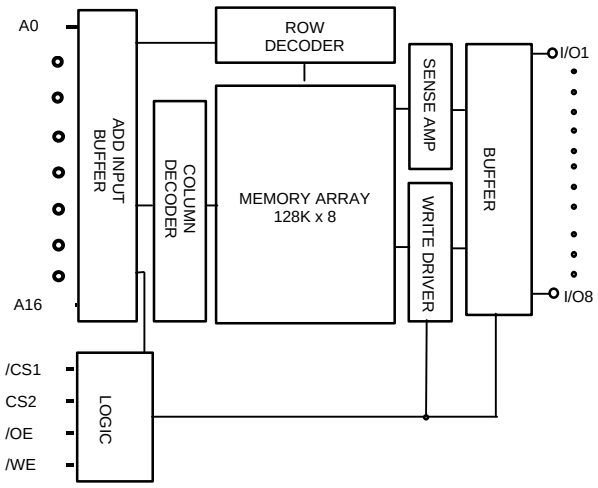


sTSOP-I / TSOP-I
(Reversed)

PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
Vcc	Power(2.7V~3.3V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62V8100BLLG	70/85/100	LL-part		SOP
HY62U8100BLLT1	85/100/120	LL-part		TSOP-I(Standard)
HY62U8100BLLR1	85/100/120	LL-part		TSOP-I(Reversed)
HY62U8100BLLST	85/100/120	LL-part		smaller TSOP-I(Standard)
HY62U8100BLLSR	85/100/120	LL-part		smaller TSOP-I(Reversed)
HY62V8100BLLG-E	70/85/100	LL-part	E	SOP
HY62U8100BLLT1-E	85/100/120	LL-part	E	TSOP-I(Standard)
HY62U8100BLLR1-E	85/100/120	LL-part	E	TSOP-I(Reversed)
HY62U8100BLLST-E	85/100/120	LL-part	E	Smaller TSOP-I(Standard)
HY62U8100BLLSR-E	85/100/120	LL-part	E	Smaller TSOP-I(Reversed)
HY62V8100BLLG-I	70/85/100	LL-part	I	SOP
HY62U8100BLLT1-I	85/100/120	LL-part	I	TSOP-I(Standard)
HY62U8100BLLR1-I	85/100/120	LL-part	I	TSOP-I(Reversed)
HY62U8100BLLST-I	85/100/120	LL-part	I	Smaller TSOP-I(Standard)
HY62U8100BLLSR-I	85/100/120	LL-part	I	Smaller TSOP-I(Reversed)

Note 1. Blank : Commercial, E : Extended, I : Industrial

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.3 to 4.6	V	
T_A	Operating Temperature	0 to 70	°C	HY62U8100B
		-25 to 85	°C	HY62U8100B-E
		-40 to 85	°C	HY62U8100B-I
T_{STG}	Storage Temperature	-65 to 125	°C	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	Mode	I/O	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	Standby
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	Data Out	Active
L	H	L	X	Write	Data In	Active

Note :
1. H=V_{IH}, L=V_{IL}, X=don't care(V_{IH} or V_{IL})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	2.7	3.0	3.3	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.6	V

Note :
1. V_{IL} = -1.5V for pulse width less than 30ns and not 100% tested

DC ELECTRICAL CHARACTERISTICS

Vcc = 2.7V~3.3V, T_A = 0°C to 70°C / -25°C to 85°C (E) / -40¡ Ëto 85¡ Ë(I), unless otherwise specified

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss ≤ V_{IN} ≤ Vcc	-1	-	1	uA
I_{LO}	Output Leakage Current		Vss ≤V_{OUT} ≤ Vcc, /CS1 = V_{IH} or CS2 = V_{IL} or /OE = V_{IH} or /WE = V_{IL}	-1	-	1	uA
Icc	Operating Power Supply Current		/CS1 = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA	-	-	5	mA
I_{CC1}	Average Operating Current		/CS1 = V_{IL}, CS2 = V_{IH}, VIN = V_{IH} or V_{IL} Cycle Time = Min, 100% duty, I_{IO} = 0mA	-	-	30	mA
I_{SB}	TTL Standby Current (TTL Input)		/CS1 = V_{IH} or CS2 = V_{IL}	-	-	0.5	mA
I_{SB1}	Standby Current (CMOS Input)	HY62U8100B	/CS1 ≥ Vcc - 0.2V CS2 ≤ 0.2V or CS2 ≥ Vcc - 0.2V	-	0.5	10	uA
		HY62U8100B-E		-	0.5	15	uA
		HY62U8100B-I		-	0.5	15	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1.0mA	2.2	-	-	V

Note : Typical values are at Vcc = 3.0V, T_A = 25°C

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vcc = 2.7V~3.3V, T_A = 0°C to 70°C / -25°C to 85°C (E) / -40¡ ëto 85¡ ë(é), unless otherwise specified

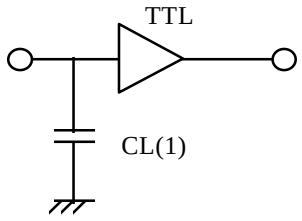
#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	20	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
9	tOH	Output Hold from Address Change	10	-	15	-	15	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	85	-	100	-	120	-	ns
11	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
12	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	55	-	75	-	85	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	30	0	35	0	40	ns
17	tDW	Data to Write Time Overlap	40	-	45	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C / -25°C to 85°C (E) / -40¡ ëto 85¡ ë(é), unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

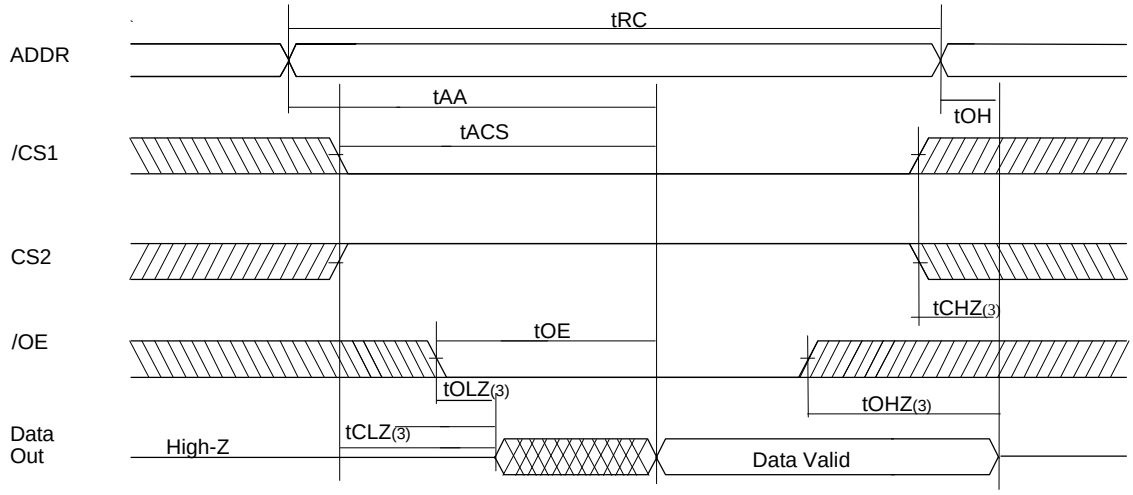
AC TEST LOADS



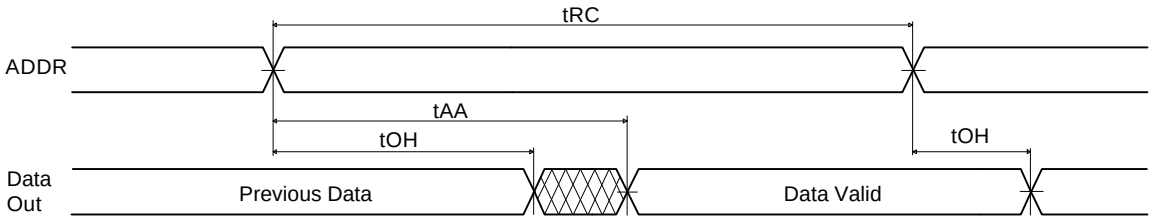
Note : 1 Including jig and scope capacitance

TIMING DIAGRAM

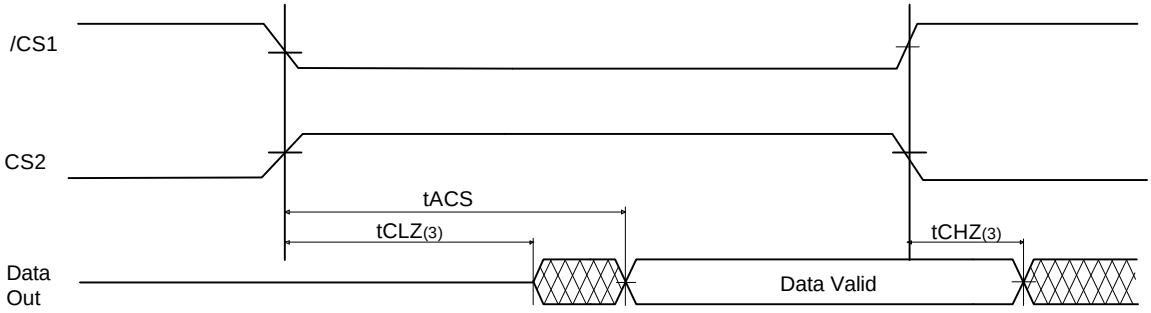
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 1,2,4)

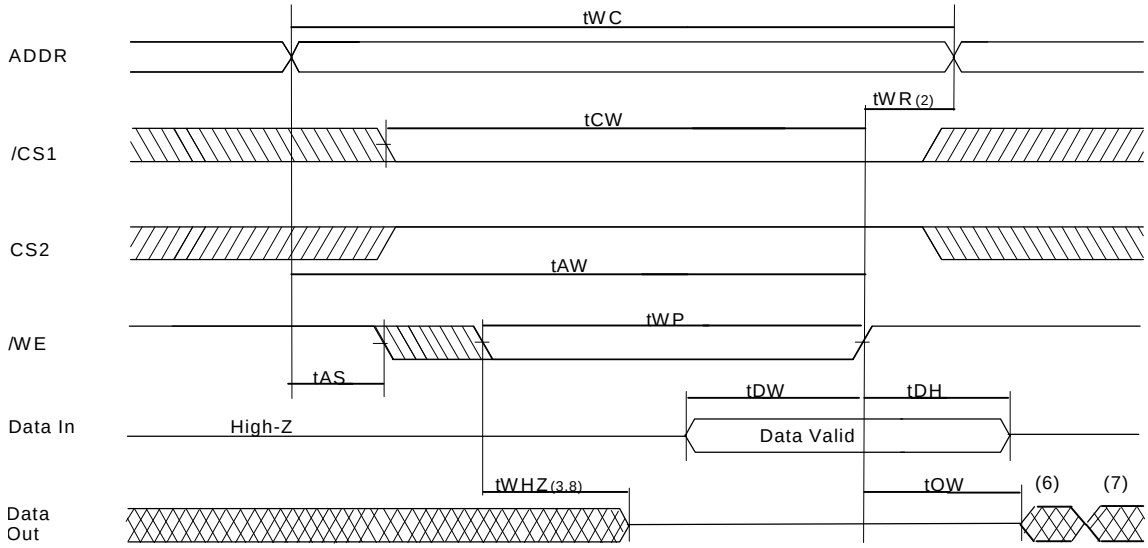


READ CYCLE 3(Note 1,2,4)

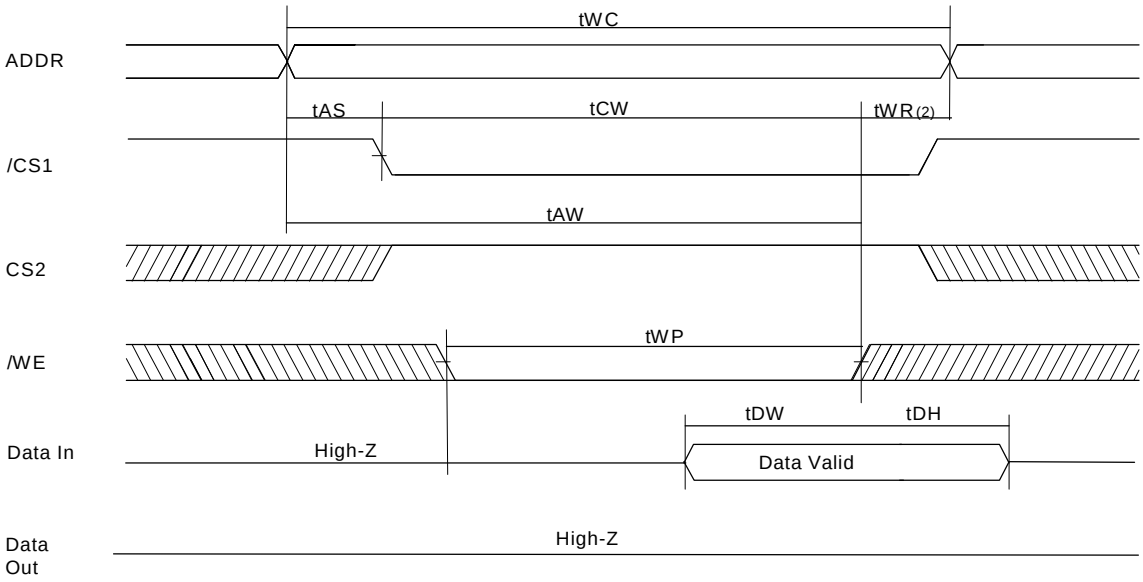


Notes:
1. Read Cycle occurs whenever a high on the /WE and /OE is low /CS1 and CS2 are in active status.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active
   CS2 in low for the standby, high for active

WRITE CYCLE 1(1,4,5,9) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,5,9) (/CS1, CS2 Controlled)



Notes:
1. A write occurs whenever a low on the /WE and /OE is low /CS1 and CS2 are in active state.
2. tWR is measured from the earlier of /CS1 or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the the /CS1 low transition and CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. Transition is measured ±200mV from steady state.
   This parameter is sampled and not 100% tested.
9. /CS1 in high for the standby, low for active
   CS2 in low for the standby, high for active

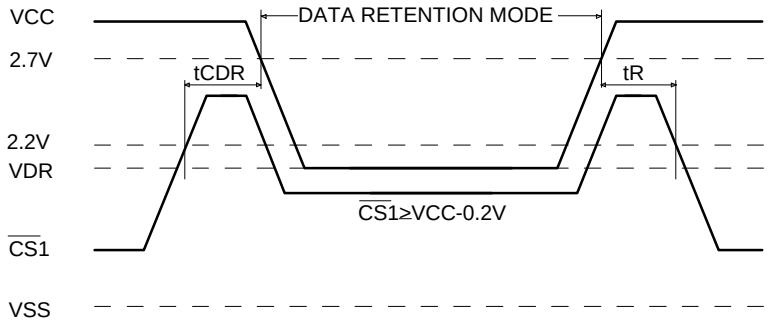
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A=0°C to 70°C / -25°C to 85°C (E) /-40°C to 85°C (I)

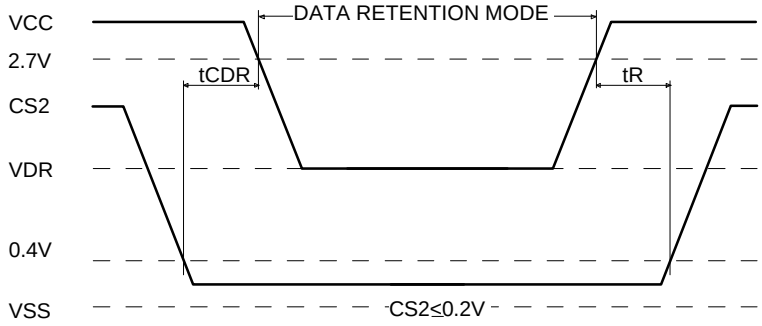
Sym	Parameter		Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention		/CS1≥Vcc-0.2V, CS2≤0.2V or Vcc – 0.2V, Vss≤V_{IN}≤Vcc	2.0	-	-	V
I_{CCDR}	Data Retention Current	HY62U8100B	Vcc=3.0V, /CS1≥Vcc - 0.2V, CS2≤0.2V or ≥ Vcc - 0.2V, Vss≤ V_{IN} ≤Vcc	-	0.5	10	uA
		HY62U8100B-E		-	0.5	15	uA
		HY62U8100B-I		-	0.5	15	uA
tCDR	Chip Deselect to Data Retention Time		See Data Retention Timing Diagram	0	-	-	ns
tR	Operating Recovery Time			t_{RC}(2)	-	-	ns

Notes:
1. Typical values are under the condition of T_A = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1

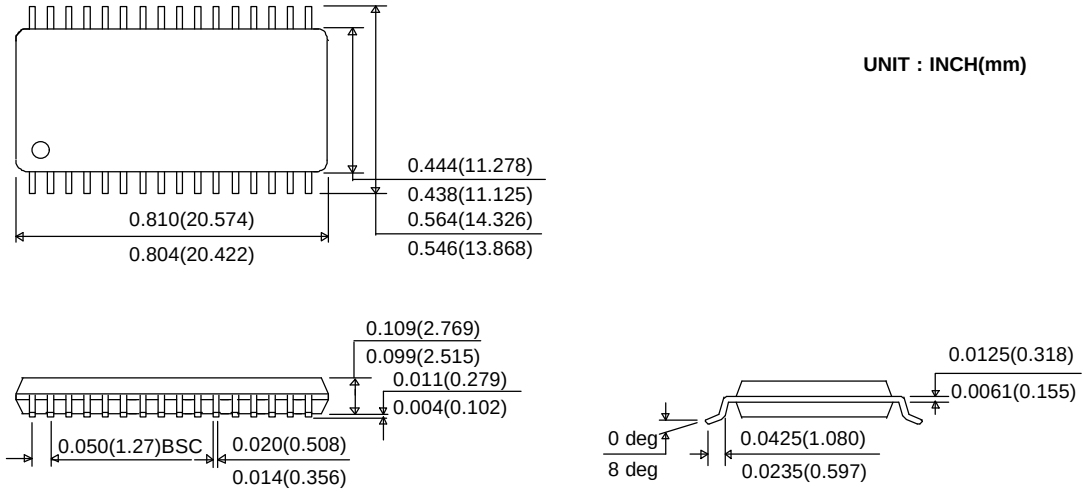


DATA RETENTION TIMING DIAGRAM 2

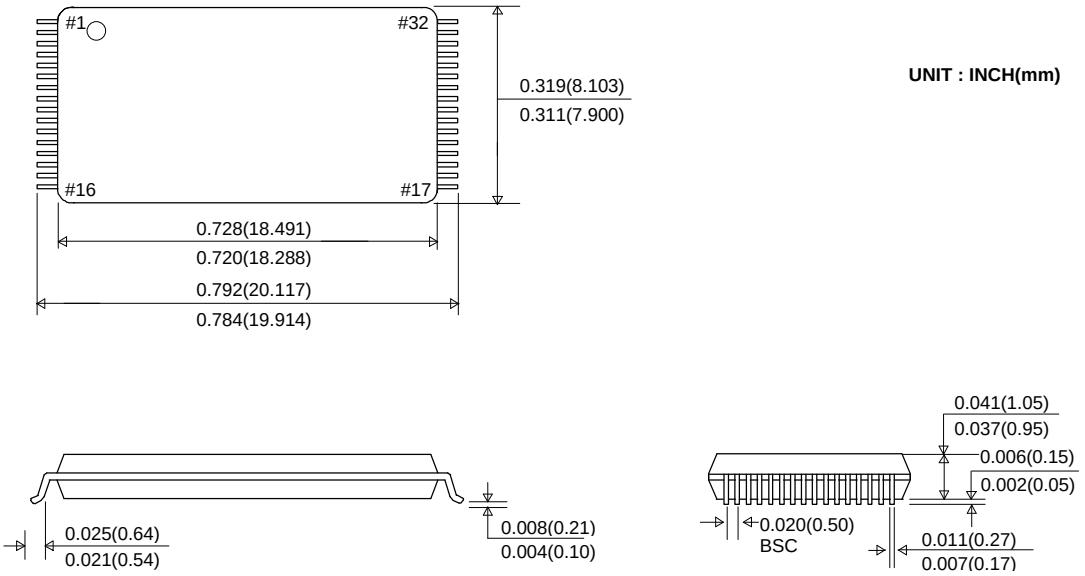


PACKAGE INFORMATION

32pin 525mil Small Outline Package(G)

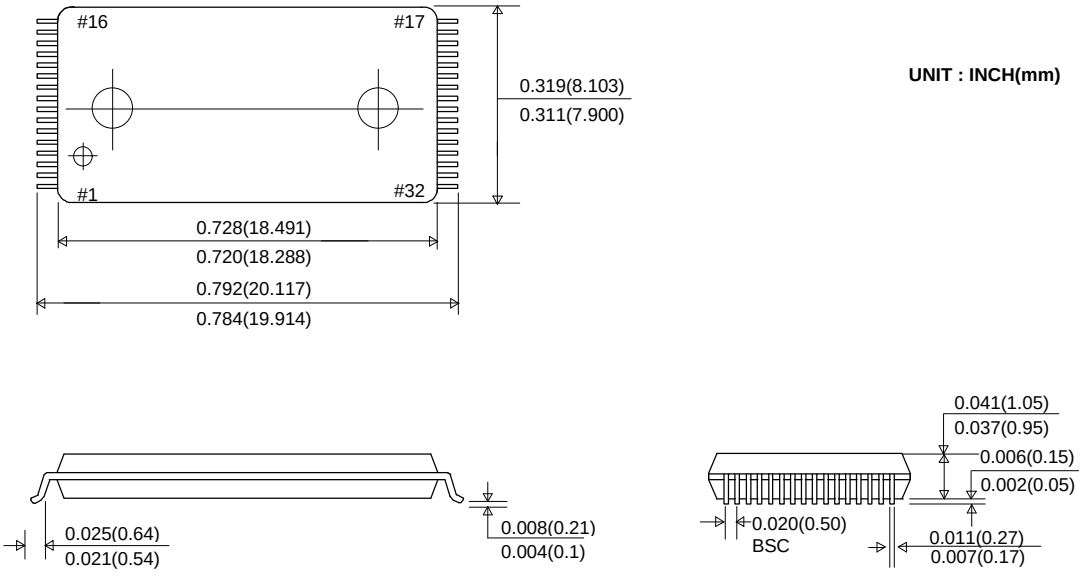


32pin 8x20mm Thin Small Outline Package Standard(T1)



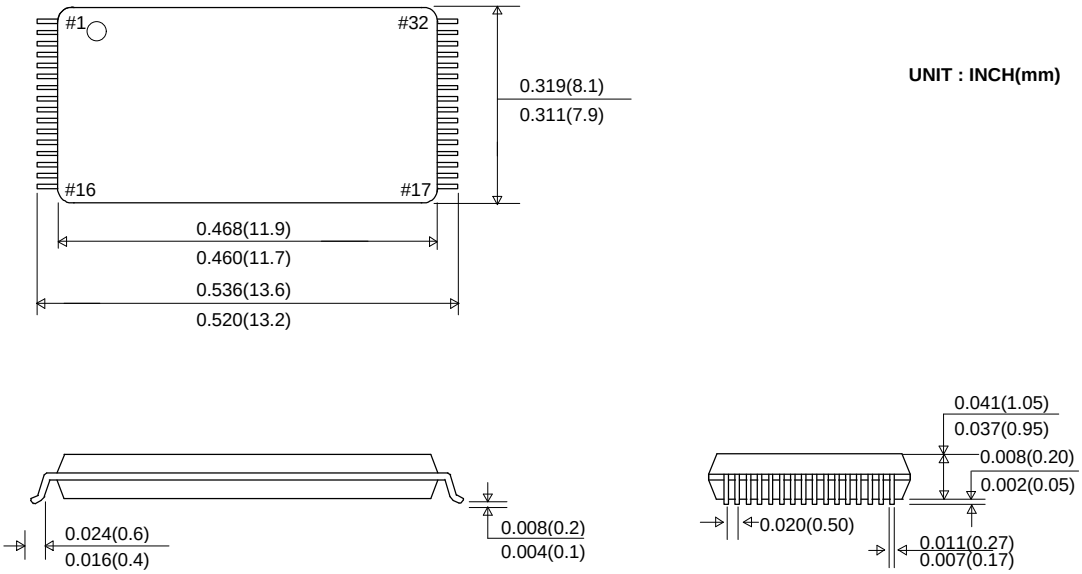
UNIT : INCH(mm)

32pin 8x20mm Thin Small Outline Package Reversed(R1)



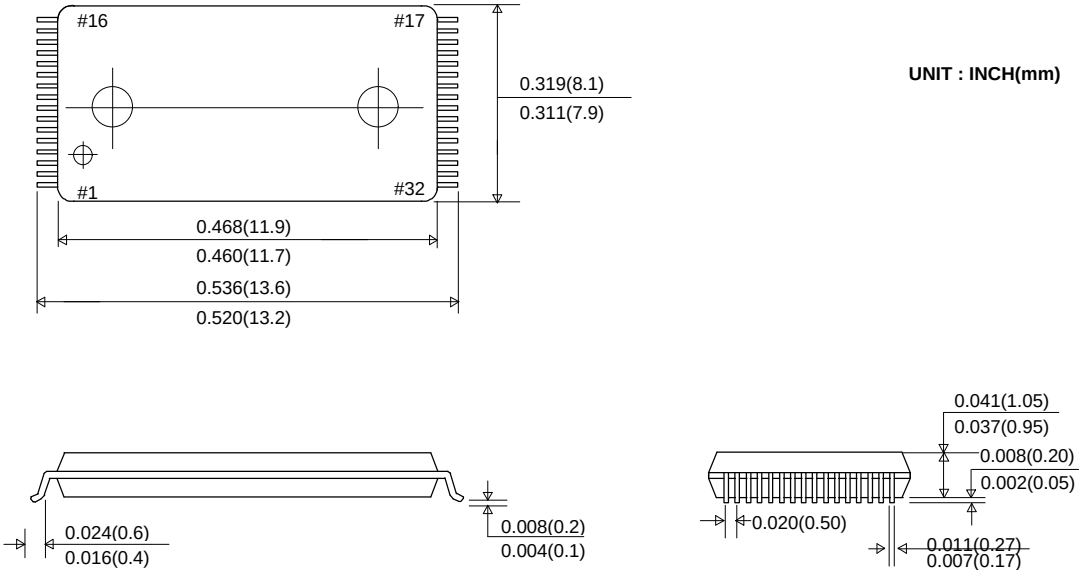
UNIT : INCH(mm)

32pin 8x13.4mm Smaller Thin Small Outline Package Standard(ST)



UNIT : INCH(mm)

32pin 8x13.4mm Thin Small Outline Package Reversed(SR)



UNIT : INCH(mm)