FAIRCHILD SEMICONDUCTOR TM

September 2000

FDS6984S

Dual Notebook Power Supply N-Channel PowerTrench® SyncFET™

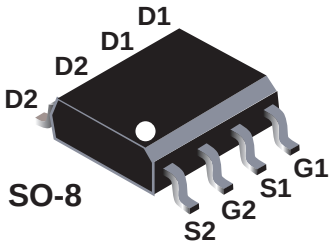
General Description

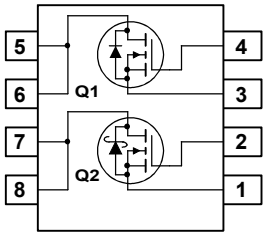
The FDS6984S is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6984S contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

Features

- **Q2**: Optimized to minimize conduction losses
  Includes SyncFET Schottky diode
  8.5A, 30V $R_{DS(on)}$ = 19 mΩ @ V_{GS} = 10V
  $R_{DS(on)}$ = 28 mΩ @ V_{GS} = 4.5V
- **Q1**: Optimized for low switching losses
  Low gate charge (5 nC typical)
  5.5A, 30V $R_{DS(on)}$ = 0.040Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.055Ω @ V_{GS} = 4.5V





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	8.5	5.5	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6984S	FDS6984S	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	Q2	30			V
		V_{GS} = 0 V, I_D = 250 µA	Q1	30			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q2			500	µA
			Q1			1	
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	Q2	1		3	V
		V_{DS} = V_{GS}, I_D = 250 µA	Q1	1		3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	Q2		-6		mV/°C
		I_D = 250 uA, Referenced to 25°C	Q1		-4		
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8.5 A	Q2		16	19	mΩ
		V_{GS} = 10 V, I_D = 8.5 A, T_J = 125°C			24	32	
		V_{GS} = 4.5 V, I_D = 7 A			23	28	
		V_{GS} = 10 V, I_D = 5.5 A	Q1		35	40	
		V_{GS} = 10 V, I_D = 5.5 A, T_J = 125°C			53	60	
		V_{GS} = 4.5 V, I_D = 4.6 A			48	55	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2	30			A
			Q1	20			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8.5 A	Q2		26		S
		V_{DS} = 5 V, I_D = 5.5 A	Q1		40		
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	Q2		1233		pF
			Q1		462		
C_{oss}	Output Capacitance		Q2		344		pF
			Q1		113		
C_{rss}	Reverse Transfer Capacitance		Q2		106		pF
			Q1		40		
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q2		8	16	ns
			Q1		10	18	
t_r	Turn-On Rise Time		Q2		5	10	ns
			Q1		14	25	
$t_{d(off)}$	Turn-Off Delay Time		Q2		25	40	ns
			Q1		21	34	
t_f	Turn-Off Fall Time		Q2		11	20	ns
			Q1		7	14	
Q_g	Total Gate Charge	Q2 V_{DS} = 15 V, I_D = 8.5 A, V_{GS} =5V	Q2		11	16	nC
			Q1		8.5	12	
Q_{gs}	Gate-Source Charge	Q1 V_{DS} = 15 V, I_D = 5.5 A, V_{GS} = 5 V	Q2		5		nC
			Q1		2.4		
Q_{gd}	Gate-Drain Charge		Q2		4		nC
			Q1		3.1		

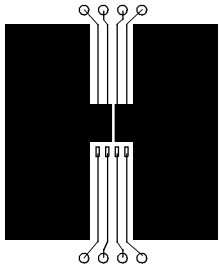
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

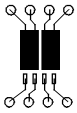
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			3.0 1.3	A
t_{rr}	Reverse Recovery Time	I_F = 10A,	Q2		17		ns
Q_{rr}	Reverse Recovery Charge	d_{iF}/d_t = 300 A/µs (Note 3)			12.5		nC
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.5 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q2 Q1		0.5 0.74	0.7 1.2	V

Notes:

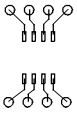
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in^2 pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. See "SyncFET Schottky body diode characteristics" below.

3. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: Q2

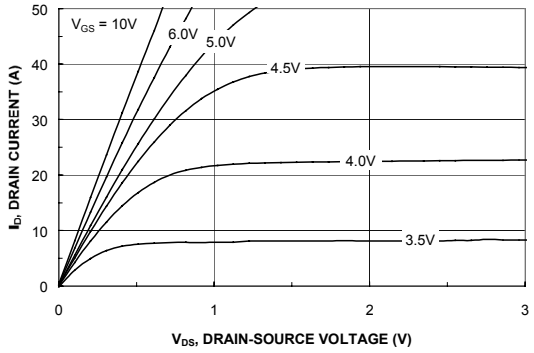


Figure 1. On-Region Characteristics.

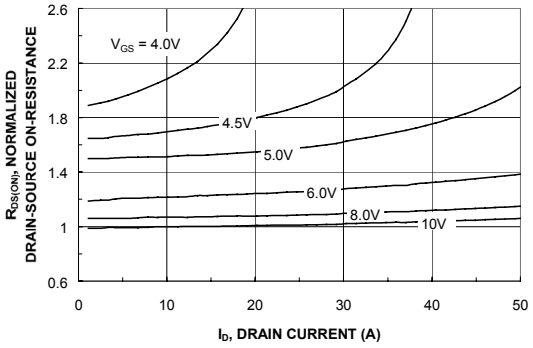


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

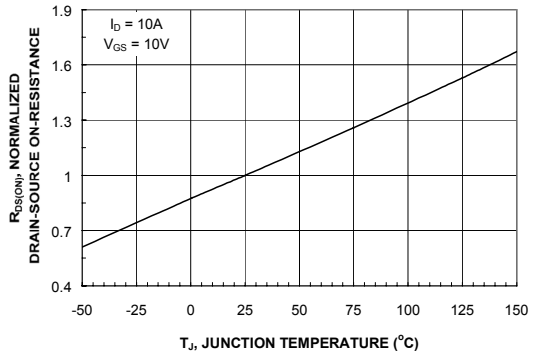


Figure 3. On-Resistance Variation with Temperature.

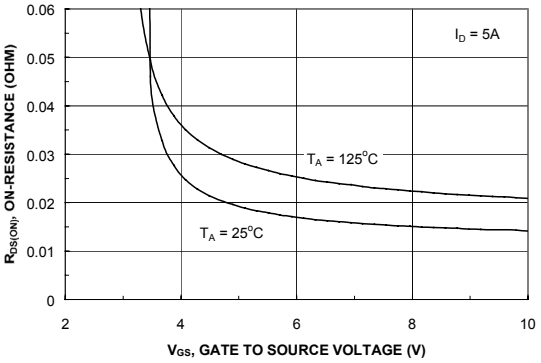


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

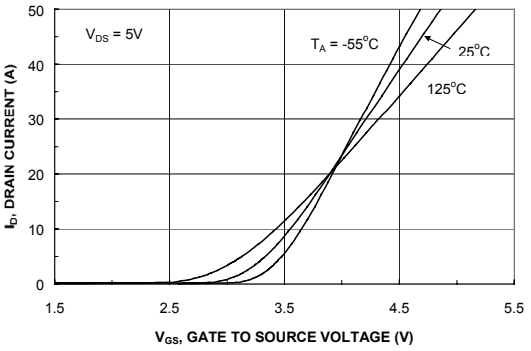


Figure 5. Transfer Characteristics.

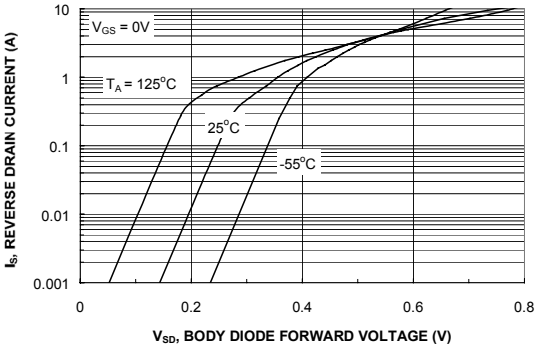


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

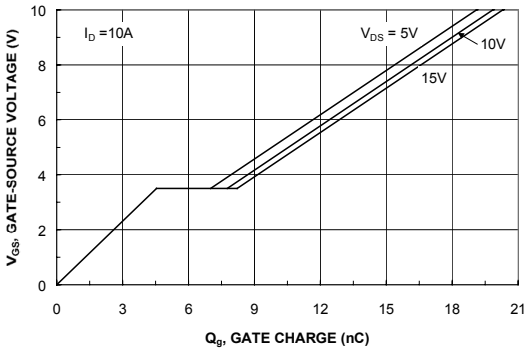


Figure 7. Gate Charge Characteristics.

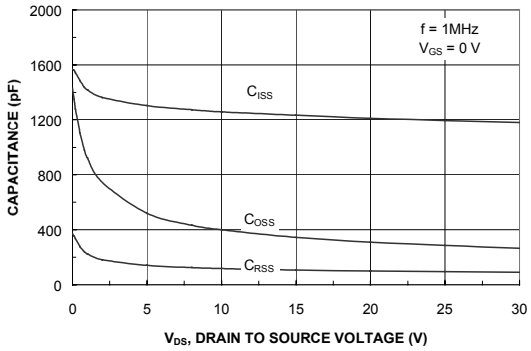


Figure 8. Capacitance Characteristics.

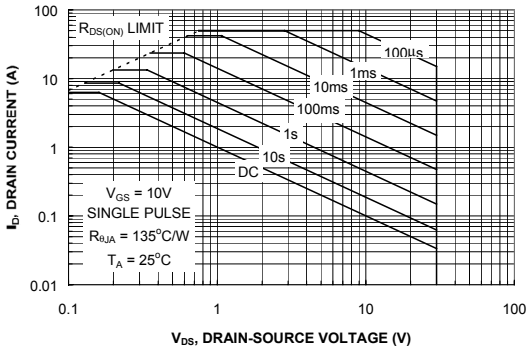


Figure 9. Maximum Safe Operating Area.

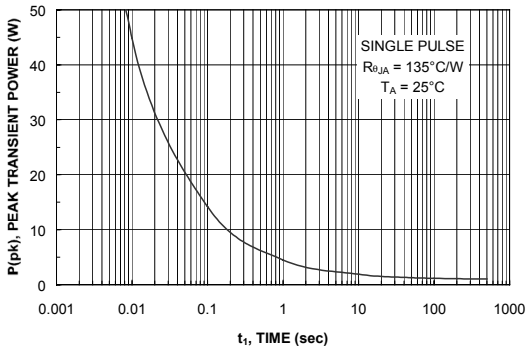


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics Q1

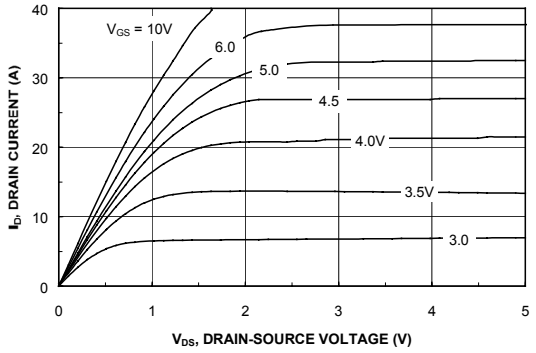


Figure 11. On-Region Characteristics.

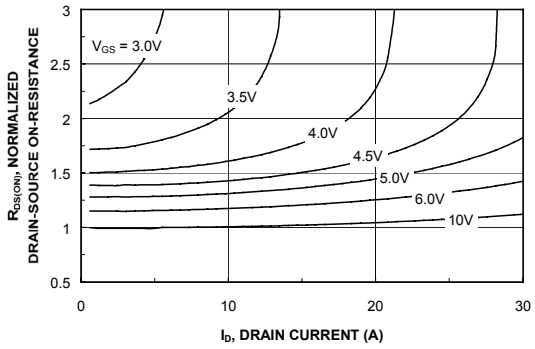


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

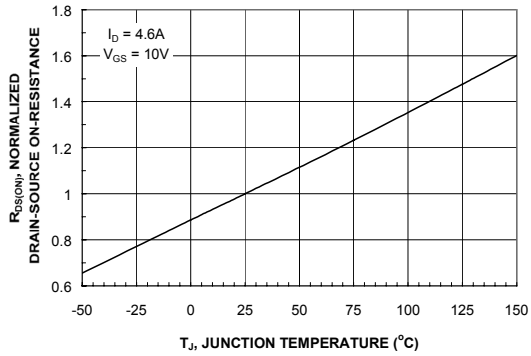


Figure 13. On-Resistance Variation with Temperature.

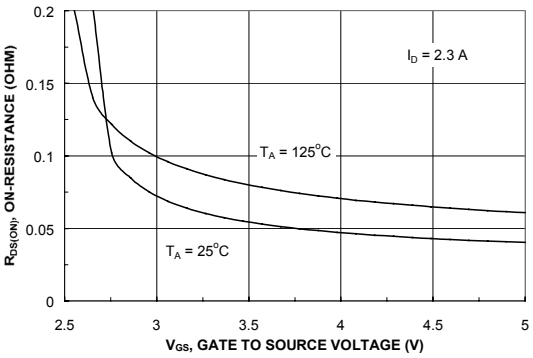


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

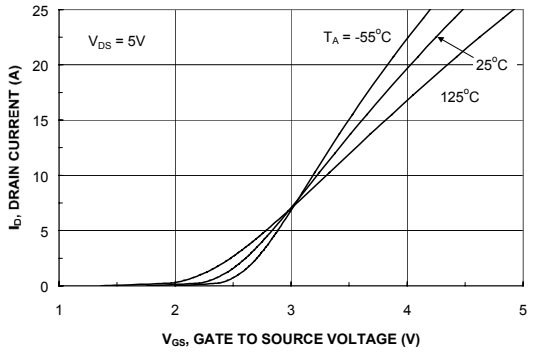


Figure 15. Transfer Characteristics.

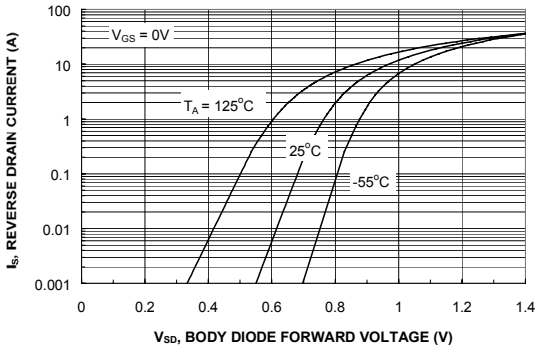


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

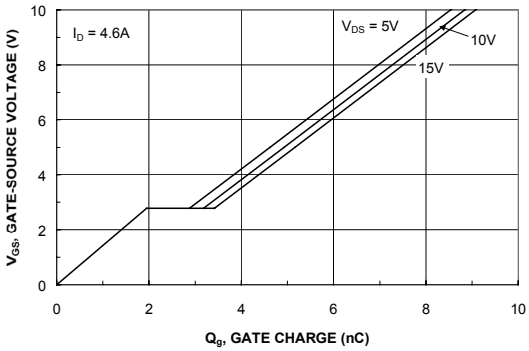


Figure 17. Gate Charge Characteristics.

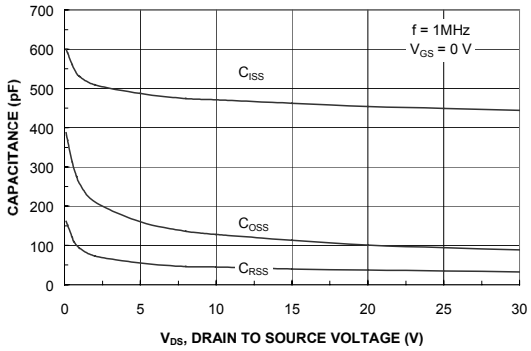


Figure 18. Capacitance Characteristics.

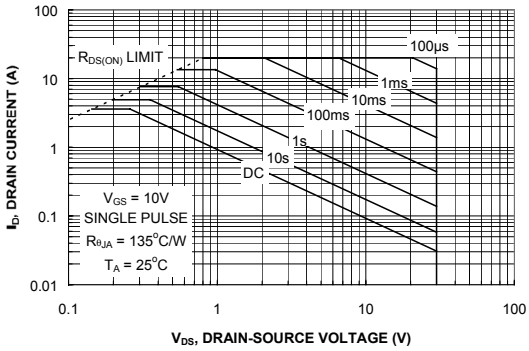


Figure 19. Maximum Safe Operating Area.

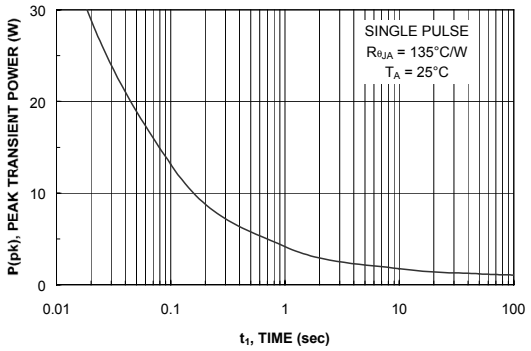


Figure 20. Single Pulse Maximum Power Dissipation.

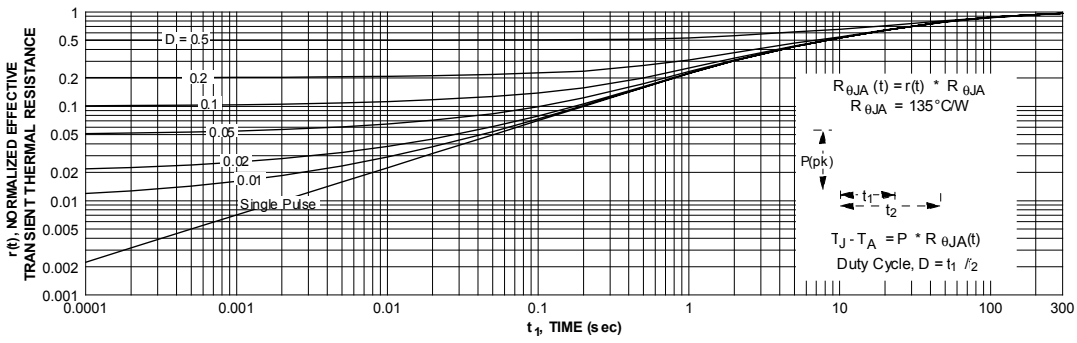


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDS6984S.

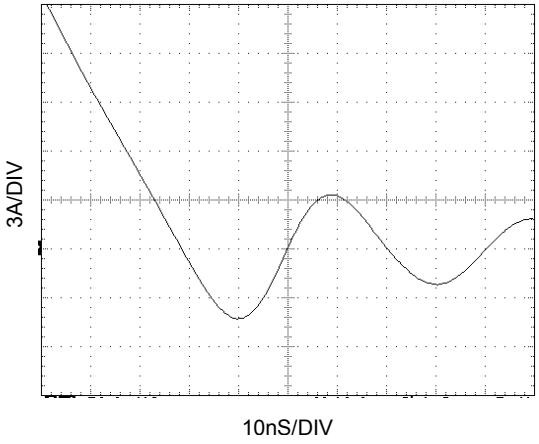


Figure 22. FDS6984S SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690A).

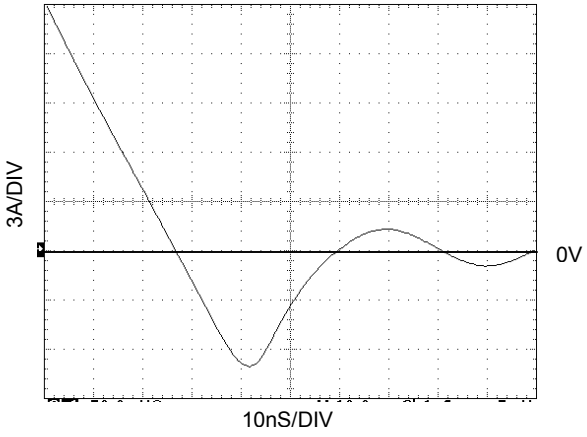


Figure 23. Non-SyncFET (FDS6690A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

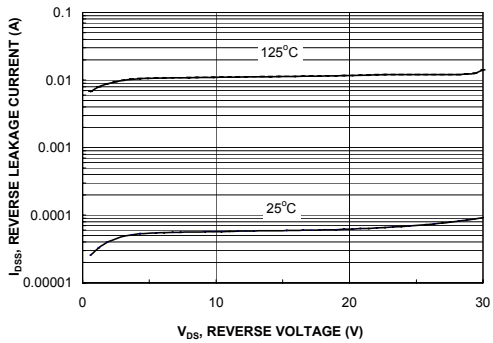
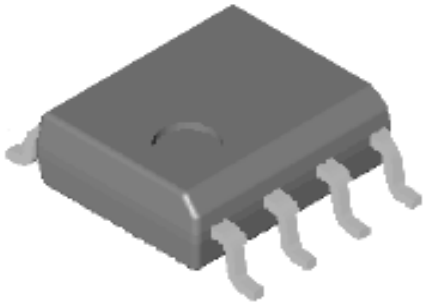


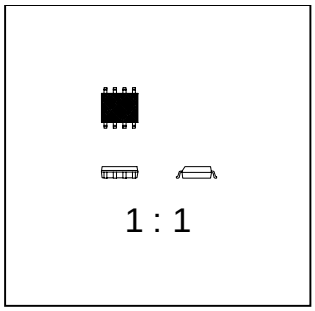
Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature.

SOIC-8 Package Dimensions

FAIRCHILD SEMICONDUCTOR™

SOIC-8 (FS PKG Code S1)

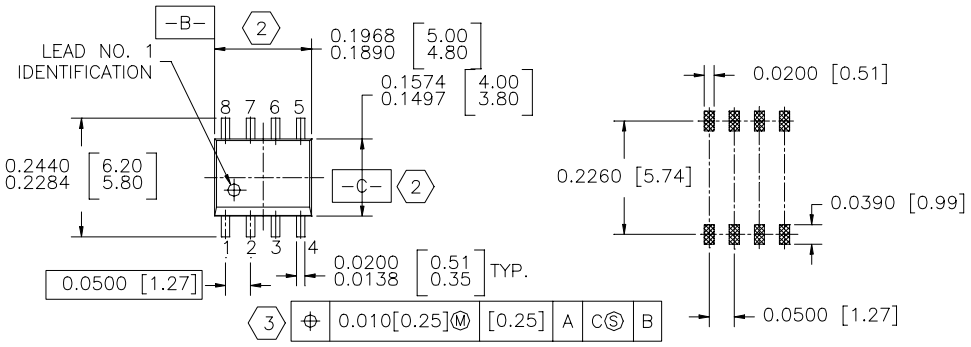


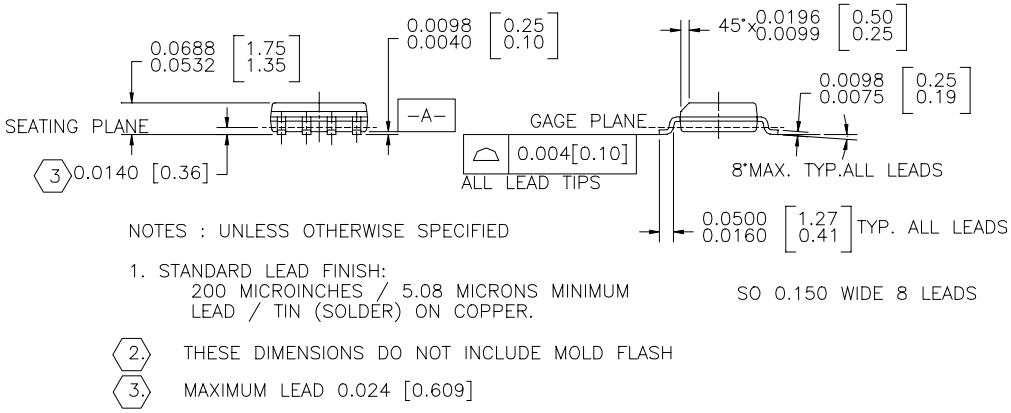


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774





NOTES : UNLESS OTHERWISE SPECIFIED

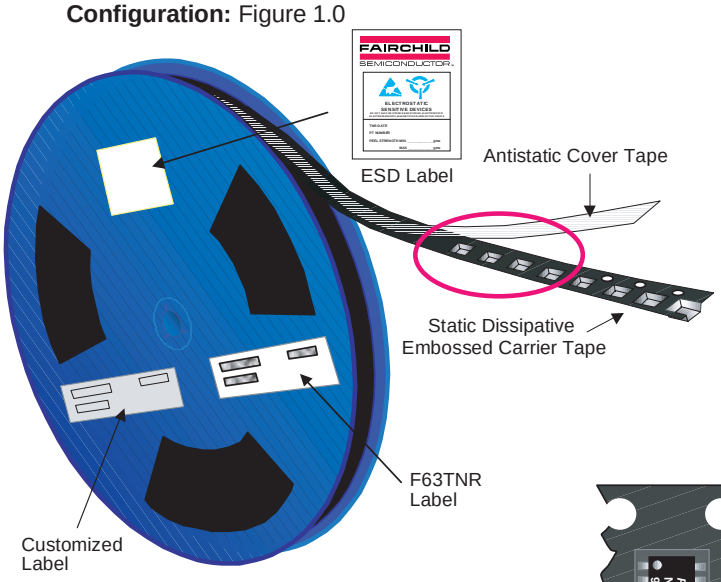
1. STANDARD LEAD FINISH:
   200 MICROINCHES / 5.08 MICRONS MINIMUM
   LEAD / TIN (SOLDER) ON COPPER.

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

SOIC-8 Tape and Reel Data

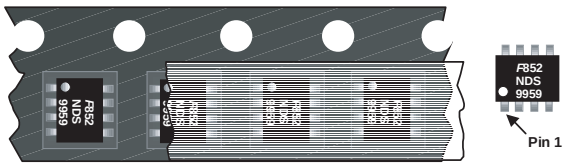
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

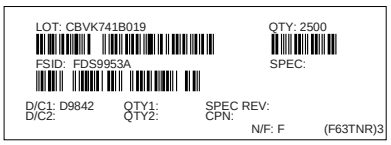
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

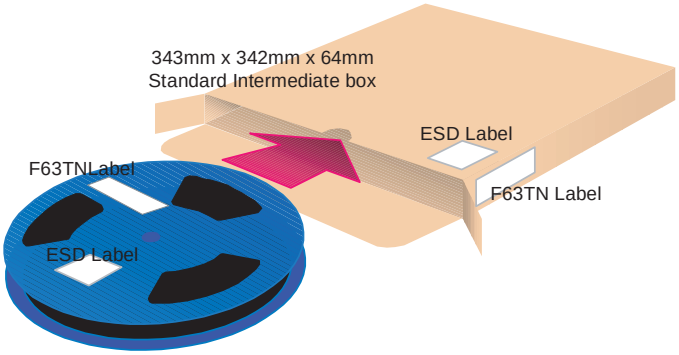


SOIC-8 Unit Orientation

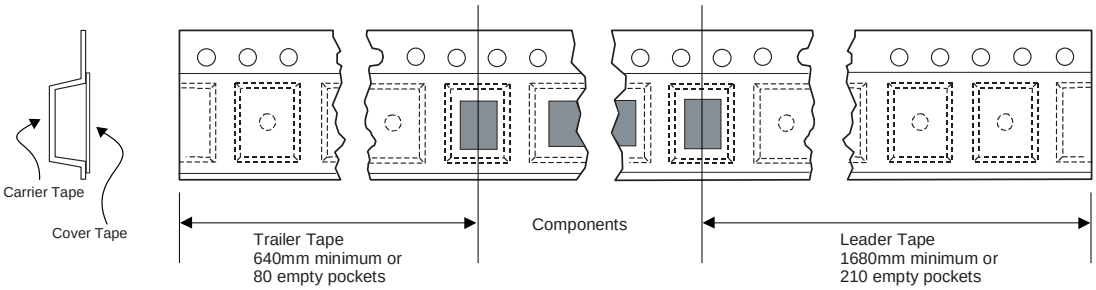
SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample



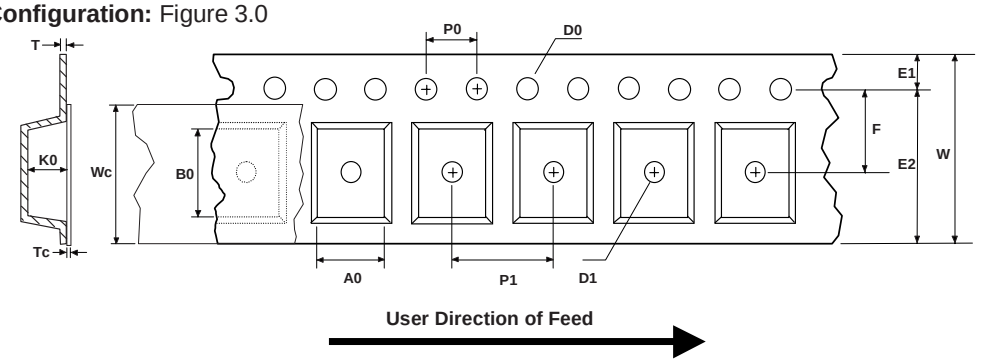


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



SOIC-8 Tape and Reel Data, continued

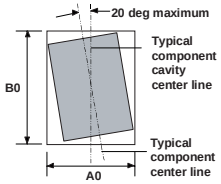
SOIC(8lds) Embossed Carrier Tape
Configuration: Figure 3.0



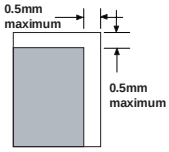
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

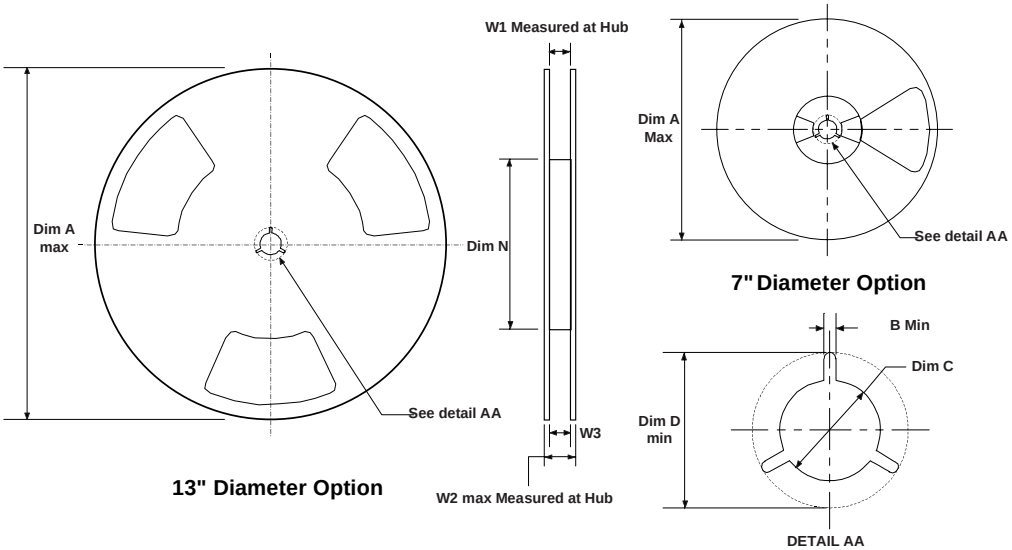


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

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HiSeC™
ISOPLANAR™
MICROWIRE™
OPTOLOGIC™
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