intel.

Intel® 82545GM Gigabit Ethernet Controller
High-Performance Gigabit Connectivity

Intel in Communications

Product Overview

The Intelligent Way to Connect

- Footprint compatibility allows for flexible designs
- Reduced power usage and heat generation for lower system costs and higher density
- Enhanced manageability and system health monitoring with ASF 1.0 and SMBus 2.0

The Intel® 82545GM Gigabit Ethernet Controller incorporates integrated Gigabit Ethernet MAC and PHY layer functions and Serializer/Deserializer (SerDes) in a single, compact component. Packaged in a 21x21mm TFBGA, the Intel 82545GM Gigabit Ethernet Controller is physically and electrically compatible with the Intel® 82546GB Dual Port Gigabit Ethernet Controller, allowing for a flexible, single-port or dual-port, multipurpose design.
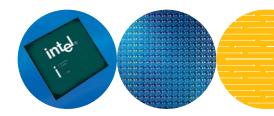
The Intel 82545GM integrates Intel's fourth-generation Gigabit MAC design with fully integrated, physical-layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, 802.3ab). For Ethernet on the backplane and fiber-optic applications, the Intel 82545GM's integrated SerDes supports 1000BASE-X (802.3z). In addition, the controller provides a direct Peripheral Component Interconnect (PCI) 2.3 and PCI-X 1.0a compliant bus at clock frequencies up to 133MHz.

The Intel 82545GM on-board SMBus port enables enhanced manageability and system health monitoring via the LAN: management packets can be routed to or from a management processor. The SMBus port enables implementation of industry standards such as IPMI (Intelligent Platform Management Interface). In addition, ASF 1.0 (Alert Standard Format) circuitry provides alerting and remote-control capabilities with standardized interfaces.

The Intel 82545GM Gigabit Ethernet Controller architecture is optimized to deliver both high-performance networking and PCI/PCI-X bus efficiency. Using state-logic design with a pipelined DMA Unit and 128-bit-wide buses for the fastest performance, the 82545GM controller handles Gigabit Ethernet traffic with low network latency and minimal internal processing overhead. The controller's architecture includes independent transmit and receive queues to limit PCI bus traffic, and a PCI interface that maximizes the use of bursts for efficient bus usage. The Intel 82545GM Gigabit Ethernet Controller prefetches up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage. A 64KB on-chip packet buffer maintains superior performance as available PCI bandwidth changes. Advanced interrupt moderation hardware manages interrupts generated by the 82545GM controller to further improve system efficiency. In addition, using hardware acceleration, the controller also offloads tasks from the host processor, such as TCP/UDP/IP checksum calculations and TCP segmentation.

Applications

The Intel 82545GM Gigabit Ethernet Controller is designed for use in the following applications:

- LAN on Motherboard (LOM) in dense, space-constrained systems such as rack-mounted servers and high-density blade servers
- Communications platform using dual Gigabit Ethernet on the backplane (PICMG 3.1 compliant or 1000BASE-X)
- Internet infrastructure devices with high-speed requirements and limited board real estate, such as switches, routers and load balancers

Features	Benefits
PCI/PCI-X Features	
133MHz PCI-X bus	▪ Supports bandwidth to allow wire-speed performance of two Gigabit Ethernet connections
Multi-function PCI device	▪ Lowest latency solution – a PCI/PCI-X bridge component is not required to implement a dual port design
PCI revision 2.3, 32/64-bit, 33/66MHz	▪ Application flexibility in LOM or embedded use ▪ 64-bit addressing for systems with more than 4GB of physical memory
Gigabit MAC/PHY/SerDes Advanced Features	
64KB configurable RX and TX packet FIFOs	▪ No external FIFO memory requirements; ▪ FIFO size tunable to the application
IEEE 802.3x compliant flow control support with software controllable thresholds	▪ Reduced frame loss due to receive FIFO overrun
Caches up to 64 packet descriptors in a single burst	▪ Efficient PCI-bandwidth usage
Programmable host memory receive buffers (256B to 16KB)	▪ Efficient usage of PCI bandwidth
Interrupt moderation controls	▪ Reduces the number of interrupts generated by receive and transmit operations ▪ Improves throughput performance and CPU utilization
Jumbo frame support up to 16KB	▪ High throughput for large data transfers on networks supporting jumbo frames
IEEE 802.1Q VLAN support with VLAN tag insertion and stripping and packet filtering for up to 4096 VLAN tags	▪ Enables IT staff to easily create multiple virtual LAN segments
Integrated PHYs for 10/100/1000Mb/s full- and half-duplex operation	▪ Reduced board space and lower power dissipation
IEEE 802.3ab Auto-Negotiation	▪ Automatic link configuration including speed, duplex, and flow control
State-of-the-art DSP architecture implements digital adaptive equalization, echo, cross-talk and baseline wander cancellation	▪ Robust 1000Mb/s performance in noisy environments and despite severe cable installation problems
PHY detects polarity, MDI-X, 2 pair vs. 4 pair and 3 pair vs. 4 pair cables	▪ Easier network installation and maintenance
Integrated Serializer-Deserializers (SerDes) PICMG 3.1 compliant	▪ Solution for server blade backplane connections and Fiber Gigabit Ethernet
Host Offloading Features	
Transmit TCP segmentation, and IP, TCP, and UDP checksum off-loading capabilities on RX and TX	▪ Increased throughput and lower CPU utilization. Compatible with large send offload feature found in Windows* 2000 and Windows* XP
Advanced packet filtering	▪ 16 exact matched (unicast or multicast) ▪ Promiscuous (unicast/multicast) transfer mode
Manageability Features (available on both ports)	
On-chip SMBus 2.0 port	▪ Enables IPMI, and ASF implementations
ASF 1.0	▪ Provides alerting and remote-control capabilities with standardized interfaces
Compliance with PCI Power Management v1.1/ACPI v2.0	▪ PCI power management capability requirements for PC and embedded applications
Wake on LAN (WoL) support	▪ Packet recognition and wakeup for network adapter and LOM applications
Automatic link speed switching from 1000Mb/s down to 10 or 100Mb/s in standby	▪ Low power in standby states ▪ Supports power-down states without software assistance
Additional Features	
Four programmable LED outputs ID on each port	▪ Indications for link speed, activity, duplex, collisions, pause by flow control, PCI speed, PCI width, and port ID on each port ▪ Allows design customization without affecting software drivers
On-chip power regulator control circuitry	▪ Simplified power supply design

Characteristics

Electrical	
PCI Signaling	3.3V and 5V
Power Dissipation	1.6W (typical)
Environmental	
Operating temperature	0°C to 70°C (maximum); Does not require a heat sink or forced airflow
Storage temperature	-65°C to 140°C
Physical	
Package	364-pin TFBGA. 1mm ball pitch, 21 x 21mm (Saves critical space on LOM board designs)
Footprint-compatible with Intel® 82546EB dual-port Gigabit Ethernet Controller	Enables a single-port or dual-port implementation on the same board

Order Code   ▪ RC82545GM