TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WT125FU

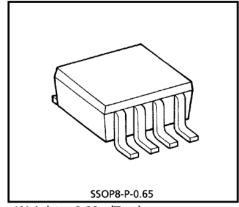
DUAL BUS BUFFER

The TC7WT125FU is a high speed CMOS DUAL BUS BUFFERS fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The input threshold levels are compatible with TTL output voltage.

The require 3-state control input \overline{G} to be set high to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

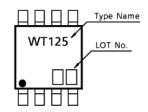


Weight: 0.02g (Typ.)

FEATURES

- High Speed $\cdots t_{pd} = 13 \text{ns} (Typ.)$ at $V_{CC} = 5 \text{V}$
- Low Power Dissipation $\cdots I_{CC} = 2\mu A$ (Max.) at $Ta = 25^{\circ}C$
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.), V_{IH} = 2.0V (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance… |IOH| = IOL = 6mA (Min.)

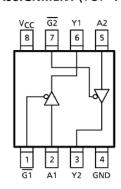
MARKING



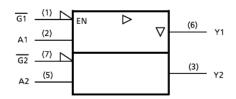
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~7	V
DC Input Voltage	VIN	-0.5~V _{CC} +0.5	V
DC Output Voltage	Vout	-0.5~V _{CC} +0.5	٧
Input Diode Current	lK	± 20	mA
Output Diode Current	loк	± 20	mA
DC Output Current	IOUT	± 35	mA
DC V _{CC} /Ground Current	lcc	± 37.5	mA
Power Dissipation	PD	300	mW
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10 s)	TL	260	°C

PIN ASSIGNMENT (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLE

INP	UTS	OUTPUTS			
G	Α	Y			
Н	×	Z			
L	L	L			
L	Н	Н			

x : Don't Care Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	4.5~5.5	V
Input Voltage	VIN	0~V _{CC}	V
Output Voltage	VOUT	0~V _{CC}	V
Operating Temperature	T _{opr}	- 40∼85	°C
Input Rise and Fall Time	t _r , t _f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC SYMBOL		TEST CONDITION		Vсс (V)	Ta = 25°C		C	Ta = -4	UNIT	
		IESI C	TEST CONDITION		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High-Level Input Voltage	VIH			4.5~ 5.5	2.0	_	_	2.0	_	٧
Low-Level Input Voltage	VIL			4.5~ 5.5	_	_	0.8	_	0.8	٧
High-Level		$V_{IN} = V_{IH}$	$I_{OH} = -20\mu A$	4.5	4.4	4.5	_	4.4	_	V
Output Voltage	Vон	or V _{IL}	I _{OH} = -6mA	4.5	4.18	4.31	_	4.13	_	
Low-Level		V. V.	$I_{OL} = 20 \mu A$	4.5	_	0.0	0.10	_	0.10	v
Output Voltage	VOL	$V_{IN} = V_{IL}$	I _{OL} = 6mA	4.5	_	0.17	0.26	_	0.33	V
3-State Output Off-State Current	loz	V _{IN} = = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	_	_	± 0.5	_	± 5.0	μΑ
Input Leakage Current	IN	V _{IN} = V _{CC} or GND		5.5	_	_	± 0.1	_	± 1.0	μΑ
	lcc	V _{IN} = V _{CC} or GND		5.5	_	_	2.0	_	20.0	μΑ
Quiescent Supply Current	Ісст	PER INPUT OTHER INPU	: V _{IN} = 0.5V or 2.4V JT: V _{CC} or GND	5.5	_	_	2.0	_	2.9	mA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

CHADACTERISTIC	CVMDOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT		
CHARACTERISTIC	SYMBOL		CL	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNII	
Output Transition	tTLH	tTLH			4.5	_	7	12	_	15	
Time	tTHL	_	50	5.5	_	6	11	_	14	ns	
		_	50	4.5	_	15	25	_	31	ns	
Propagation Delay	t _{pLH}			5.5	_	13	22	_	28		
Time	t _{pHL}		150	4.5	_	21	33	_	41		
	"			5.5	_	18	29	_	37		
	^t pZL ^t pZH	$R_L = 1k\Omega$	50 150	4.5	_	17	30	_	38	- ns	
Output Enable Time				5.5	_	14	27	_	34		
				4.5	_	23	38	_	48		
				5.5	_	20	34	_	43		
Output Disable Time	t _{pLZ}	$R_L = 1k\Omega$	50	4.5	_	16	30	_	38		
				5.5	_	13	27	_	34	ns	
Input Capacitance	CIN	_	_	_	_	5	10	_	10	pF	
Output Capacitance	COUT	_	_	_		10	_	_	_	pF	
Power Dissipation Capacitance	C _{PD}	(Note 1)	-	_	_	32	_	_	_	pF	

(Note 1): CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

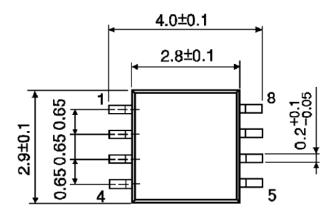
ICC (opr) = CpD · VCC · fIN + ICC / 2 (per Gate)

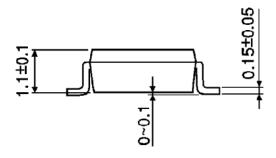
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PACKAGE DIMENSIONS

SSOP8-P-0.65

Unit: mm





Weight: 0.02g (Typ.)

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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