MX23C4111

4M-BIT [512K x 8/256K x 16] CMOS MASK ROM with page mode

FEATURES

- With page mode function
- Switchable organization
  - 512K x 8 (byte mode)
  - 256K x 16 (word mode)
- Single +5V power supply
- Fast access time:100/120/150/200ns
- Fast page mode access time:60/70ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package
  - 40 pin DIP (600 mil)
  - 40 pin SOP (500 mil)

GENERAL DESCRIPTION

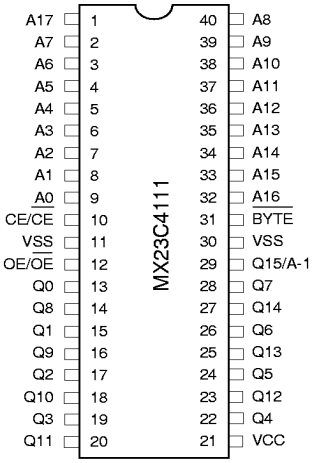
The MX23C4111 is a 5V only, 4M-bit, Read Only Memory with page mode. It is organized as 512Kx8 bits (byte mode) or as 256Kx16 bit (word mode) depending on $\overline{BYTE}$ (pin 31) voltage level. MX23C4111 has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C4111 offers automatic power-down, with power-down controlled by the chip enable (CE/$\overline{CE}$) input. When CE/$\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/$\overline{CE}$ stays in the unselected mode.

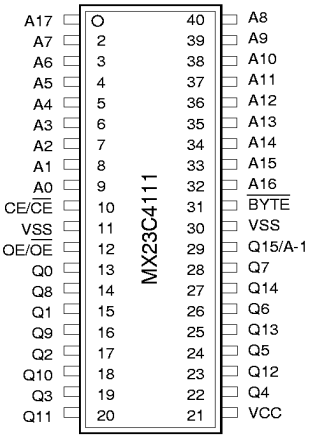
The OE/$\overline{OE}$ input as well as CE/$\overline{OE}$ input may be programmed active Low.

PIN CONFIGURATION

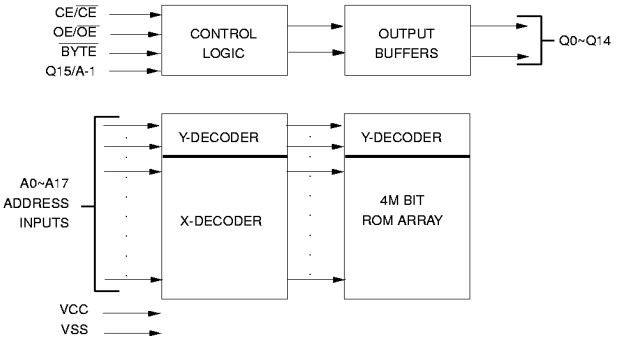
40 PDIP



40 SOP



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Input
Q0~Q14	Data Output
CE/$\overline{CE}$	Chip Enable Input
OE/$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection
Q15/A-1	Q15(Word mode)/LSB address(Byte mode)
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

BYTE MODE ($\overline{BYTE}$=VSS)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High Z	Standby (ICC2)	1
L	L/H	X	Non selected	High Z	Operating (ICC1)	1
L	H/L	A-1 input	Selected	DOUT	Operating (ICC1)	1

WORD MODE ($\overline{BYTE}$=VCC)

$\overline{CE}$	OE/$\overline{OE}$	D15/A-1	MODE	D0-D7	SUPPLY CURRENT	NOTE
H	X	High Z	Non selected	High Z	Standby (ICC2)	1
L	L/H	High Z	Non selected	High Z	Operating (ICC1)	1
L	H/L	DOUT	Selected	DOUT	Operating (ICC1)	1

NOTE1:X=H or L

ABSOLUTE MAXIMUM RATINGS*

RATING	VALUE
Ambient Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
Power Dissipation	1.0W

*Note:
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	VIN=0 to 5.5V
Output Leakage Current	ILO	-	10uA	VOUT=0 to 5.5V
Power-Down Supply Current	ICC3	-	100uA	$\overline{CE}$>VCC-0.2V
Standby Supply Current	ICC2	-	1.0mA	$\overline{CE}$ = VIH
Operating Supply Current	ICC1	-	60mA	Note 1

CAPACITANCE (Ta = 25℃, f=1.0MHz (Note 2))

Item	Symbol	MIN.	MAX.	UNIT	Conditions
Input Capacitance	CIN	-	8	pF	VIN=0V
Output Capacitance	COUT	-	8	pF	VOUT=0V

AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

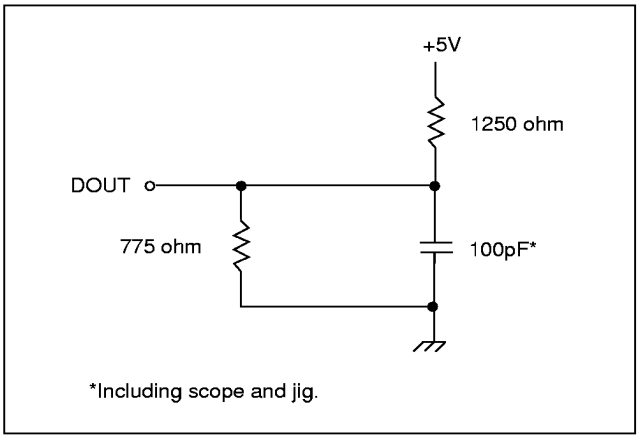
Item	Symbol	23C4111-10		23C4111-12		23C4111-15		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	CONDITIONS
Cycle Time	tCYC	100ns	-	120ns	-	150ns	-	
Address Access Time	tAA	-	100ns	-	120ns	-	150ns	
Output Hold Time After Address Change	tOH	0ns	-	0ns	-	0ns	-	
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns	
Output Enable/Chip Select Access Time	tAOE	-	70ns	-	80ns	-	90ns	
Output Low Z Delay	tLZ	0ns	-	0ns	-	0ns	-	Note 3
Output High Z Delay	tHZ	-	70ns	-	70ns	-	70ns	Note 4
$\overline{BYTE}$ Access Time	tBHA	-	100ns	-	120ns	-	150ns	
$\overline{BYTE}$ Output Hold Time	tOHB	0ns	-	0ns	-	0ns	-	
$\overline{BYTE}$ Output Delay Time	tBHZ	-	70ns	-	70ns	-	70ns	
$\overline{BYTE}$ Output Set Time	tBLZ	10ns	-	10ns	-	10ns	-	
Page Mode Access Time	tPA	-	60ns	-	60ns	-	70ns	

Note:
1. Measured with device selected at f=5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% teseted.
3. Output low-impedance delay (tLA) is measured from $\overline{CE}$ going low.
4. Output high-impedance delay (tHZ) is measured from $\overline{CE}$ going high.

AC Test Conditions

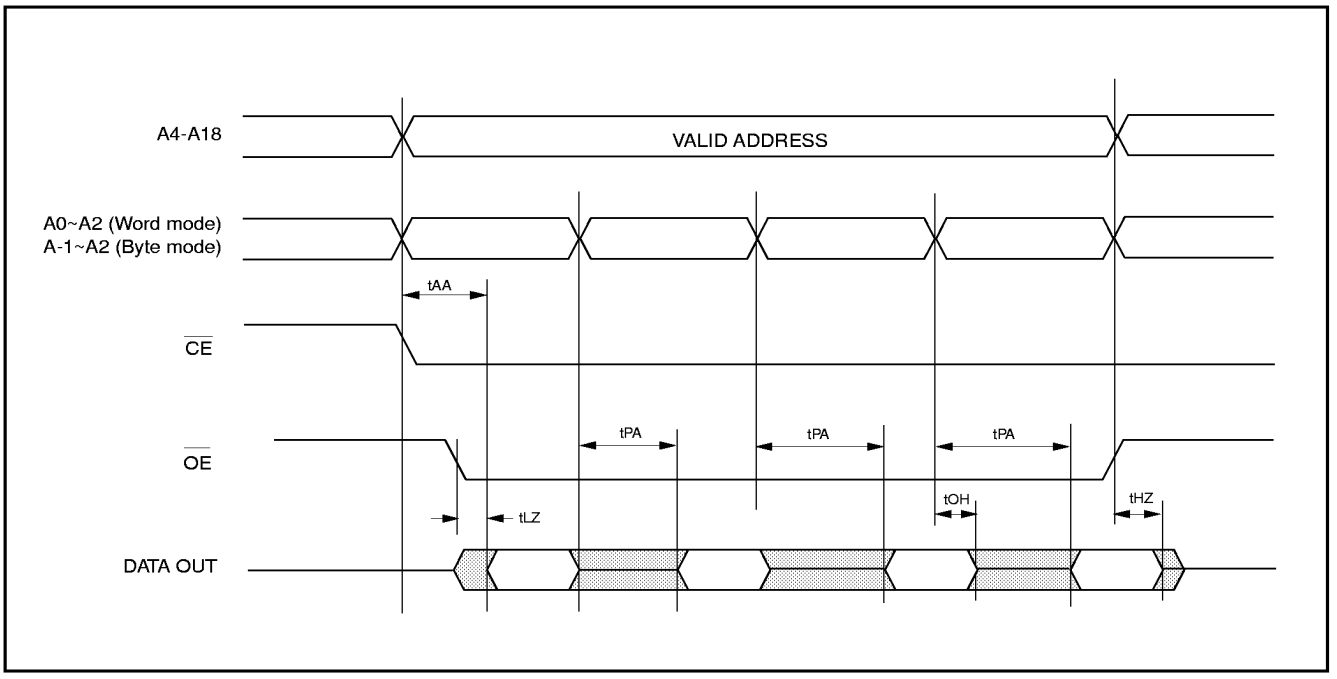
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	1TLL+100pF

FIG.1 OUTPUT LOAD CIRCUIT

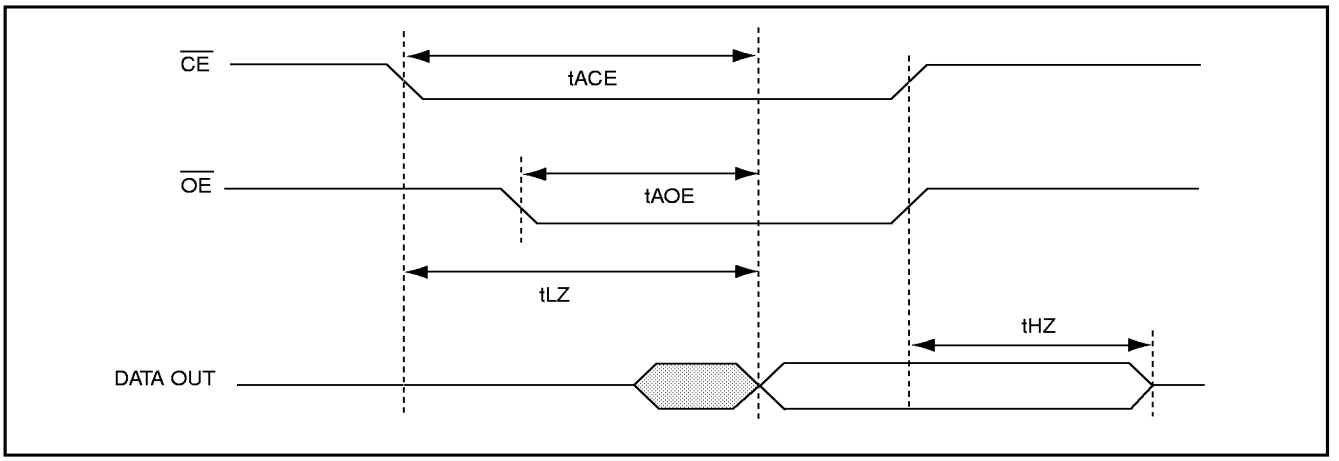


TIMING DIAGRAM

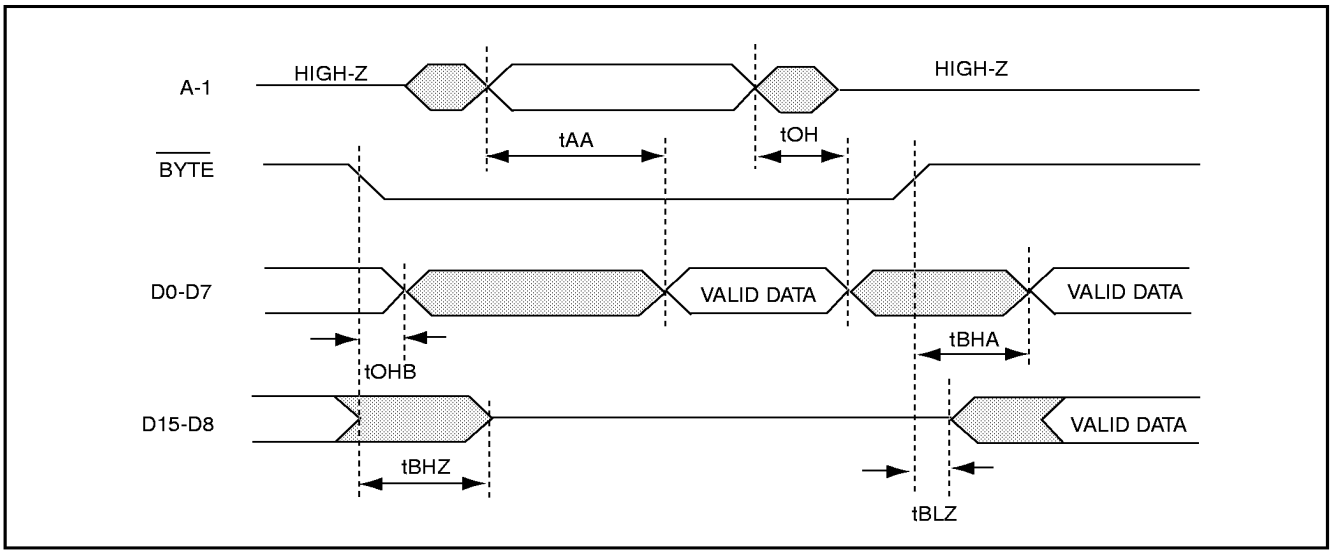
PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$=ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDER INFORMATION

Part No.	Access Time	Operating Current MAX.	Standby Current MAX.	Package
MX23C4111PC-10	100ns	60mA	100uA	40 pin DIP
MX23C4111MC-10	100ns	60mA	100uA	40 pin SOP
MX23C4111PC-12	120ns	60mA	100uA	40 pin DIP
MX23C4111MC-12	120ns	60mA	100uA	40 pin SOP
MX23C4111PC-15	150ns	60mA	100uA	40 pin DIP
MX23C4111MC-15	150ns	60mA	100uA	40 pin SOP

REVISION HISTORY

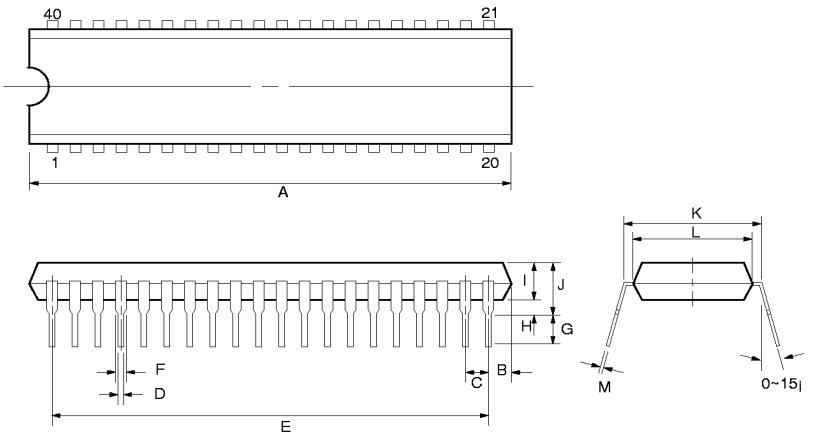
REVISION	DESCRIPTION	PAGE	DATE
1.1	AC CHARACTERISTICS tOH 10ns-->0ns	P3	JAN/29/1999

PACKAGE INFORMATION

40-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	48.22	1.900
F	1.52 [Typ.]	.060 [Typ.]
G	3.30±.25	.130±.010
H	.51 [REF]	.020 [REF]
I	3.94±.25	1.55±.010
J	5.33 max.	.210 max.
K	15.22±.25	.600±.010
L	13.97±.25	.550±.010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



40-PIN PLASTIC SOP

ITEM	MILLIMETERS	INCHES
A	26.16 max.	1.030 max.
B	1.00 [REF]	.038 [REF]
C	1.27 [TP]	.050 [TP]
D	.43 [Typ.]	.017 [Typ.]
E	.102 min.	.004 min.
F	2.54 max.	.100 max.
G	2.24±.05	.088±.002
H	14.22±.08	.560±.007
I	11.18±.12	.440±.005
J	1.52	.060
K	.15 [Typ.]	.006 [Typ.]
L	.79	.031

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.