DRAM

256K x 16 DRAM

5V, EDO PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 300mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- Extended Data-Out (EDO) PAGE MODE access cycle
- BYTE WRITE and BYTE READ access cycles

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Write Cycle Access	
BYTE or WORD via $\overline{\text{CAS}}$	16270
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4C16270DJ-7

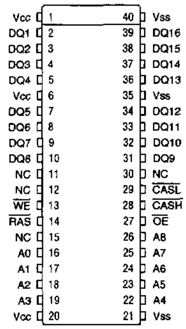
*60ns specifications are limited to a Vcc range of ±5%. Contact factory for availability of 60ns.

KEY TIMING PARAMETERS

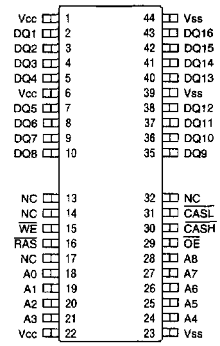
SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns
-8	150ns	80ns	33ns	40ns	20ns	12ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(DA-7)



40/44-Pin TSOP
(DB-4)



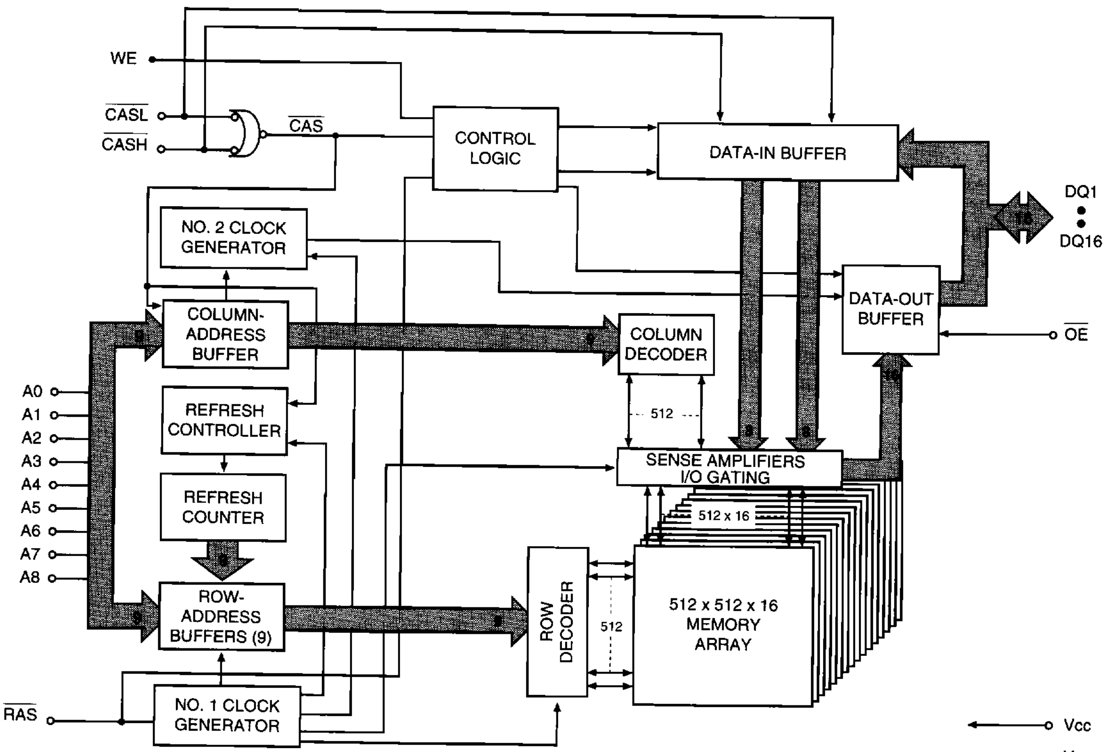
GENERAL DESCRIPTION

The MT4C16270 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins.

The MT4C16270 offers an accelerated cycle access called EDO PAGE MODE.

The MT4C16270 $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and by the last to transition back HIGH. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ function in an identical manner to $\overline{\text{CAS}}$ in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate an internal $\overline{\text{CAS}}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4C16270 has two CAS controls, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE and RAS). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4C16270 CAS function is determined by the first CAS (CASL or CASH) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the MT4C16270 both byte READ and byte WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE , WE and RAS.

EDO PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the EDO PAGE MODE operation.

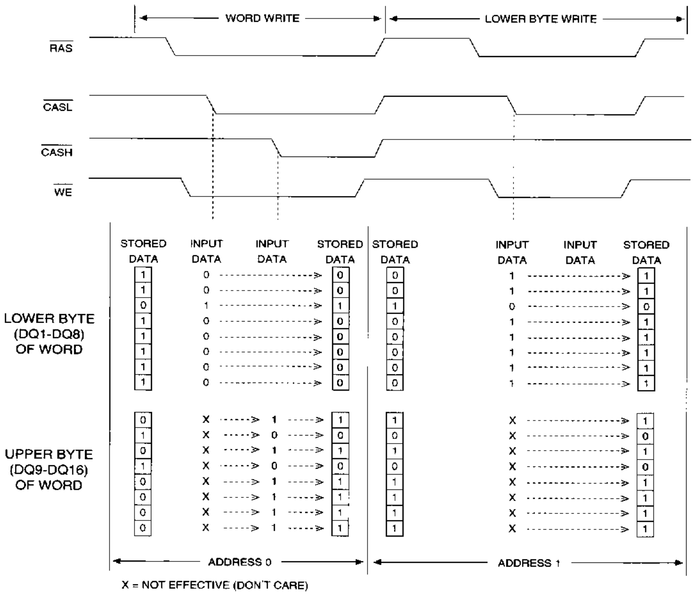


Figure 1
WORD AND BYTE WRITE EXAMPLE

EDO DRAM

BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4C16270 can be viewed as two 256K x 8 DRAMs which have common input controls. Figure 1 illustrates the MT4C16270 BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. If CAS goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4C16270 offers an accelerated PAGE MODE cycle by eliminating output disable from CAS HIGH. This option is called EDO and it allows CAS precharge time (ᵗCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ᵗOEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ᵗOEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 2 for further detail on the

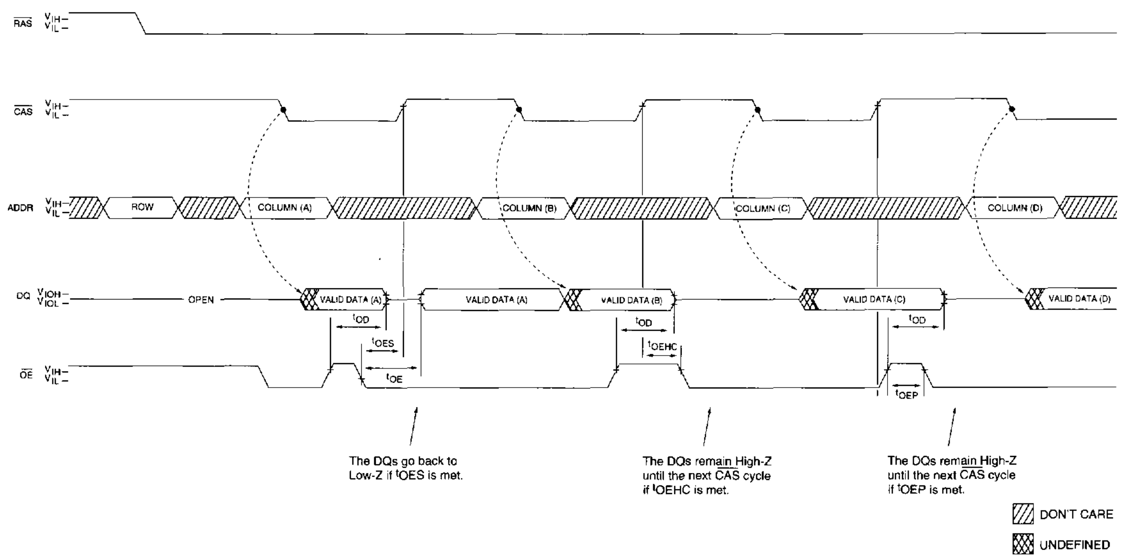


Figure 2
OUTPUT ENABLE AND DISABLE

toggling $\overline{OE}$ condition). During other cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or ^tWHZ after $\overline{WE}$ transitions LOW. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 3.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

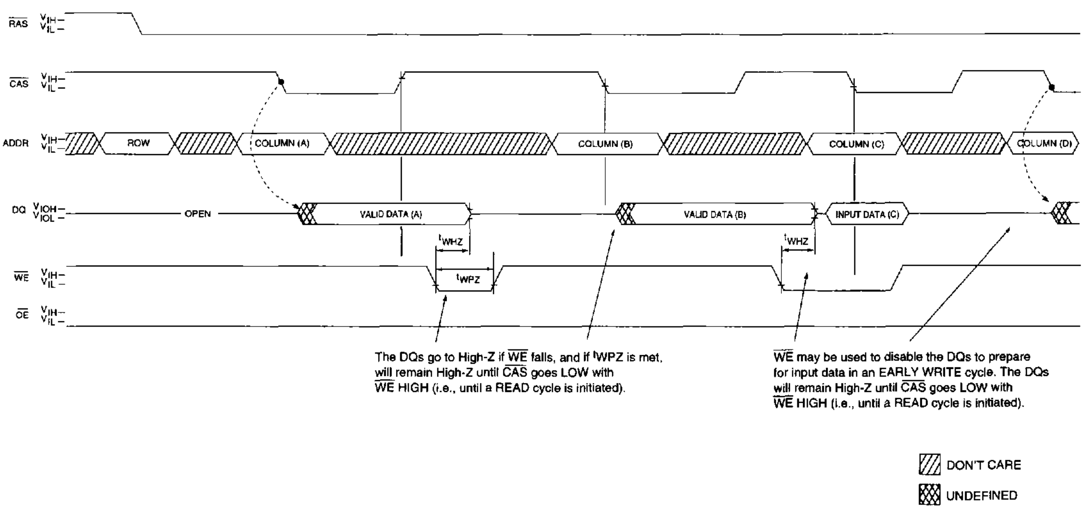


Figure 3
OUTPUT ENABLE AND DISABLE WITH $\overline{WE}$

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{CASL}$ or $\overline{CASH}$).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.1mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	195	175	160	mA	3, 4, 40
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	130	125	120	mA	3, 4, 40
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC [MIN])	ICC5	195	175	160	mA	3
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS, CASL, CASH, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35		40	ns	
Column-address setup to CAS precharge during WRITE	^{t}ACH	15		15		20		ns	
Column-address hold time (referenced to RAS)	^{t}AR	40		40		55		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	29
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to WE delay time	^{t}AWD	55		60		65		ns	21
Access time from CAS	^{t}CAC		15		20		20	ns	15, 31
Column-address hold time	^{t}CAH	10		12		15		ns	29
CAS pulse width	^{t}CAS	10	10,000	12	10,000	12	10,000	ns	37
CAS hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5, 30
Last CAS going LOW to first CAS returning HIGH	^{t}CLCH	10		10		10		ns	32
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	31, 41
Data output hold after CAS LOW	^{t}COH	5		5		5		ns	
CAS precharge time	^{t}CP	10		10		10		ns	16, 34
Access time from CAS precharge	^{t}CPA		35		40		45	ns	31
CAS to RAS precharge time	^{t}CRP	5		5		5		ns	30
CAS hold time	^{t}CSH	40		40		60		ns	30
CAS setup time (CBR REFRESH)	^{t}CSR	10		10		110		ns	5, 29
CAS to WE delay time	^{t}CWD	40		45		45		ns	21, 29
Write command to CAS lead time	^{t}CWL	10		12		12		ns	26, 30
Data-in hold time	^{t}DH	10		15		15		ns	22, 31
Data-in hold time (referenced to RAS)	^{t}DHR	40		40		60		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22, 31
Output disable time	^{t}OD	3	15	3	15	3	15	ns	28, 39, 41
Output Enable time	^{t}OE		15		20		20	ns	23, 31
OE hold time from WE during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	27
OE HIGH hold time from CAS HIGH	^{t}OEHC	10		10		10		ns	
OE HIGH pulse width	^{t}OEP	10		10		10		ns	
OE LOW to CAS HIGH setup time	^{t}OES	5		5		5		ns	
Output buffer turn-off delay from CAS or RAS	^{t}OFF	3	15	3	15	3	15	ns	20, 28, 31, 41

*60ns specifications are limited to a V_{CC} range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		33		ns	33
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	72		79		84		ns	33
Access time from RAS	^{t}RAC		60		70		80	ns	14
RAS to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Row-address hold time	^{t}RAH	10		10		10		ns	
Column-address to RAS lead time	^{t}RAL	22		27		30		ns	
RAS pulse width	^{t}RAS	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (EDO PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
RAS to CAS delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19, 26, 30
Read command setup time	^{t}RCS	0		0		0		ns	26, 29
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
RAS precharge time	^{t}RP	35		40		60		ns	
RAS to CAS precharge time	^{t}RPC	10		10		10		ns	
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
RAS hold time	^{t}RSH	10		15		15		ns	38
READ WRITE cycle time	^{t}RWC	140		157		187		ns	
RAS to WE delay time	^{t}RWD	85		95		105		ns	21
Write command to RAS lead time	^{t}RWL	10		12		12		ns	26
Transition time (rise or fall)	^{t}T	2	50	2	50	2	50	ns	9, 10
Write command hold time	^{t}WCH	10		10		10		ns	26, 38
Write command hold time (referenced to RAS)	^{t}WCR	40		40		60		ns	26
Write command setup time	^{t}WCS	0		0		0		ns	21, 26, 29
Output disable delay from WE	^{t}WHZ	3	15	3	15	3	15	ns	
Write command pulse width	^{t}WP	10		10		10		ns	26

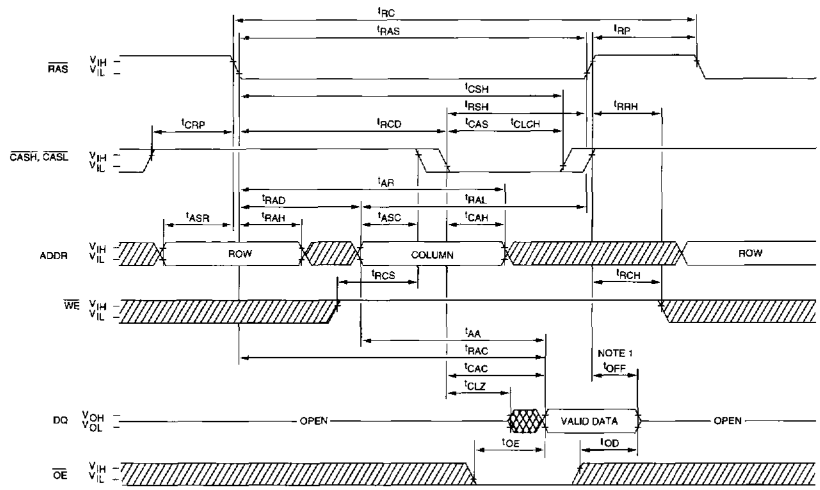
*60ns specifications are limited to a Vcc range of ±5%.

NOTES

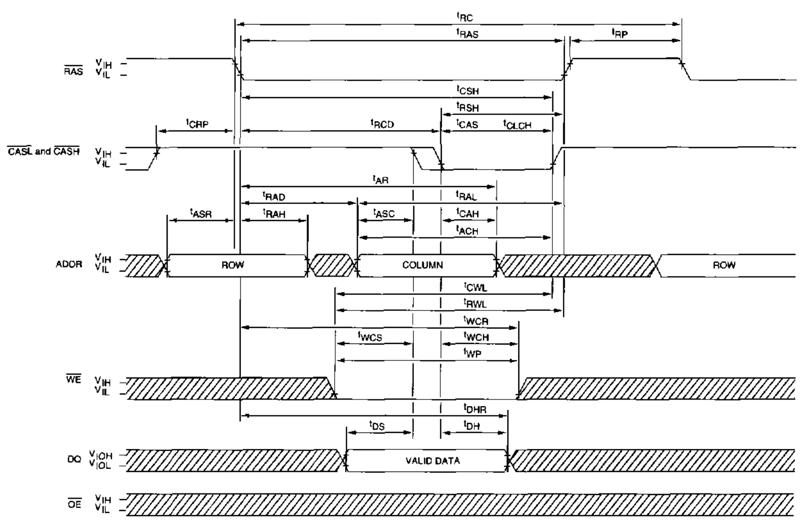
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
29. The first $\overline{CASx}$ edge to transition LOW.
30. The last $\overline{CASx}$ edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
32. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
33. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
34. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
35. First DQs controlled by the first $\overline{CASx}$ to go LOW.
36. Last DQs controlled by the last $\overline{CASx}$ to go HIGH.
37. Each $\overline{CASx}$ must meet minimum pulse width.
38. Last $\overline{CASx}$ to go LOW.
39. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
40. Column-address changed once each cycle.
41. The 3ns minimum is a parameter guaranteed by design.

EDO DRAM

READ CYCLE



EARLY WRITE CYCLE

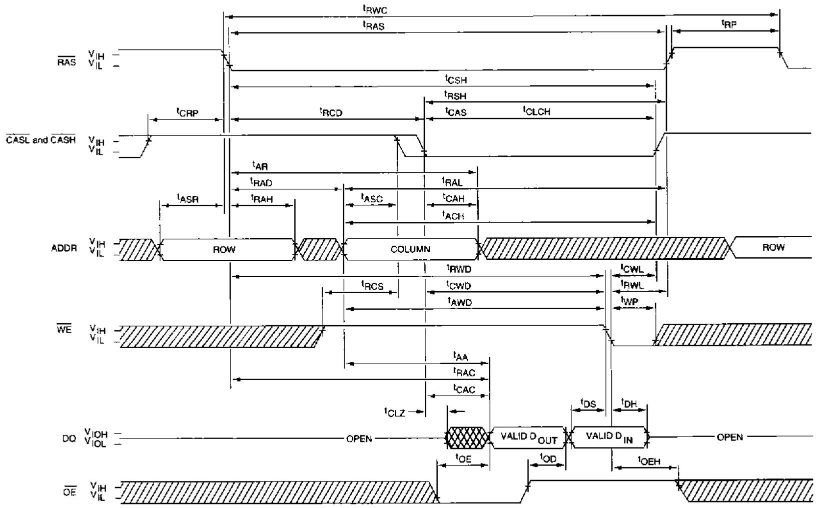


DON'T CARE

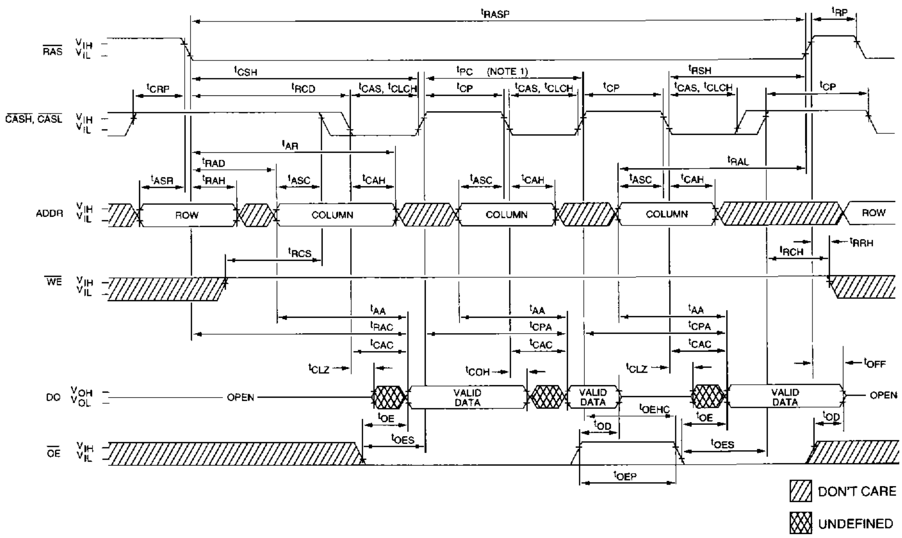
UNDEFINED

NOTE: 1. tOFF is referenced from the rising edge of RAS or CAS, whichever occurs last.

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

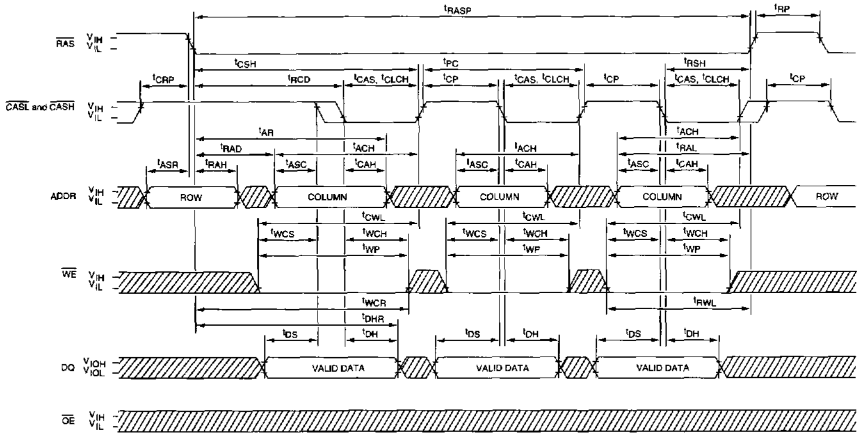


EDO-PAGE-MODE READ CYCLE

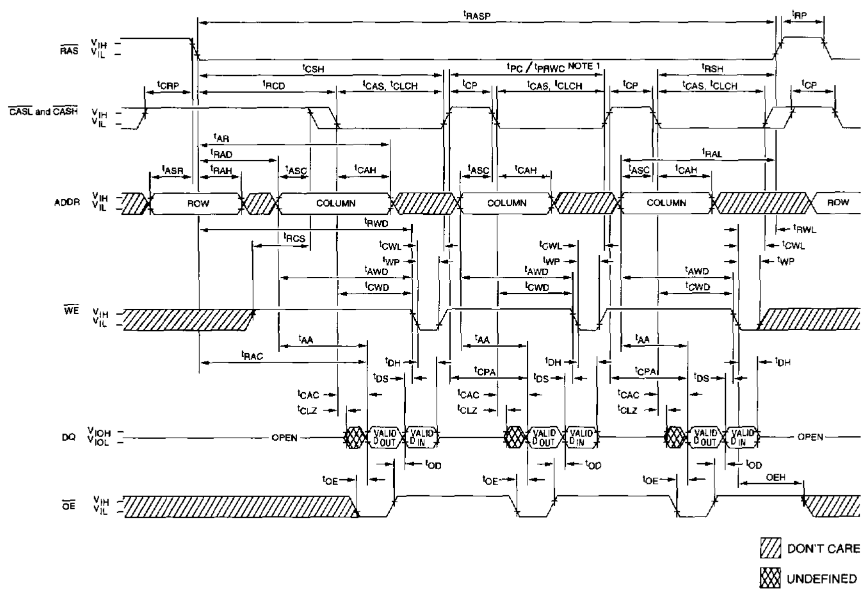


NOTE: 1. tPC can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specification.

EDO-PAGE-MODE EARLY-WRITE CYCLE

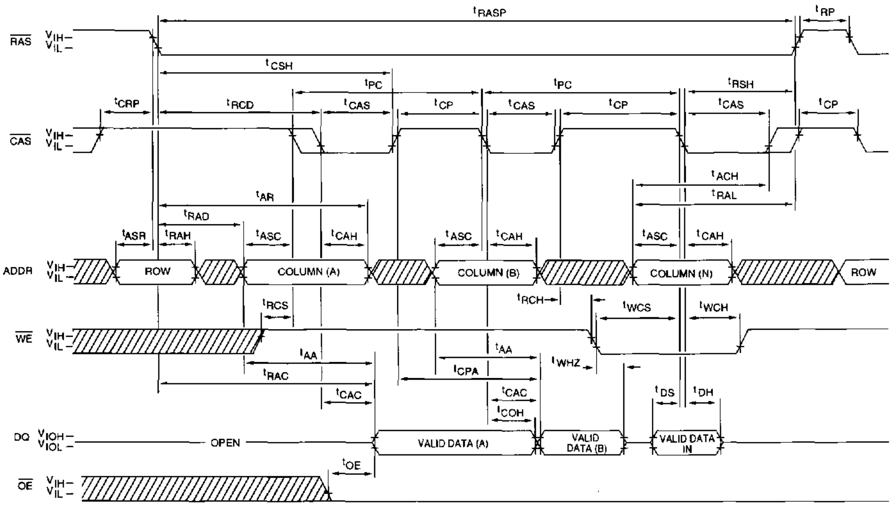


EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

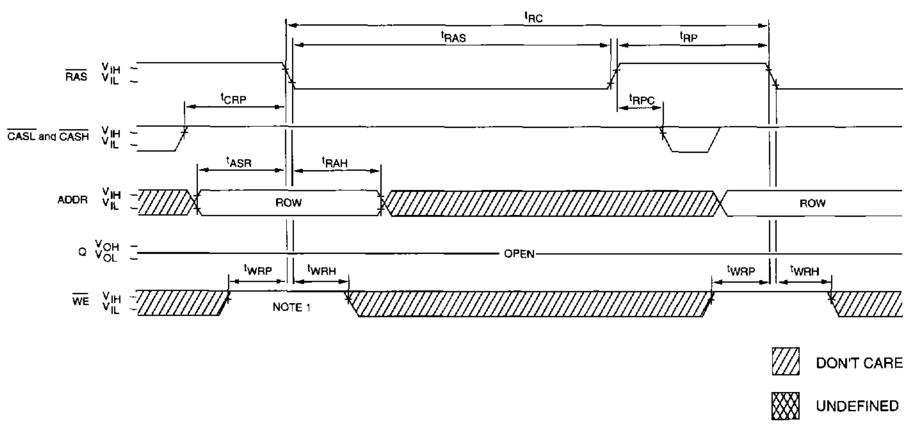


NOTE: 1. ᵗPC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the ᵗPC specification.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)

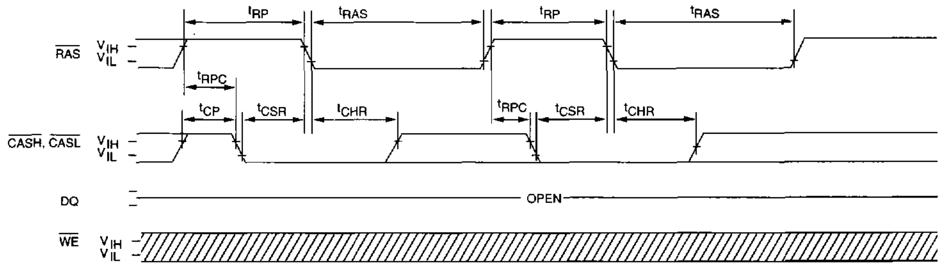


RAS-ONLY REFRESH CYCLE
(OE, WE = DON'T CARE)

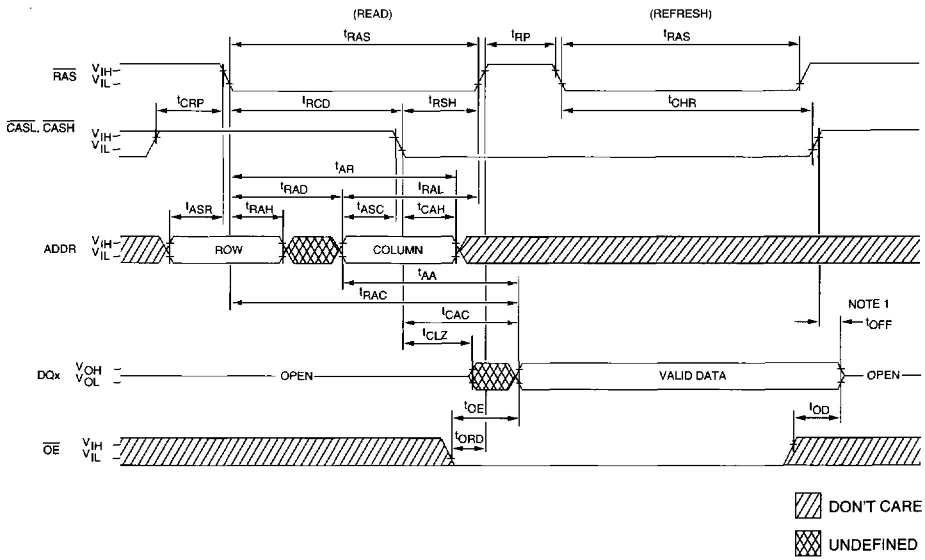


NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

CBR REFRESH CYCLE
(Addresses; $\overline{OE}$ = DON'T CARE)

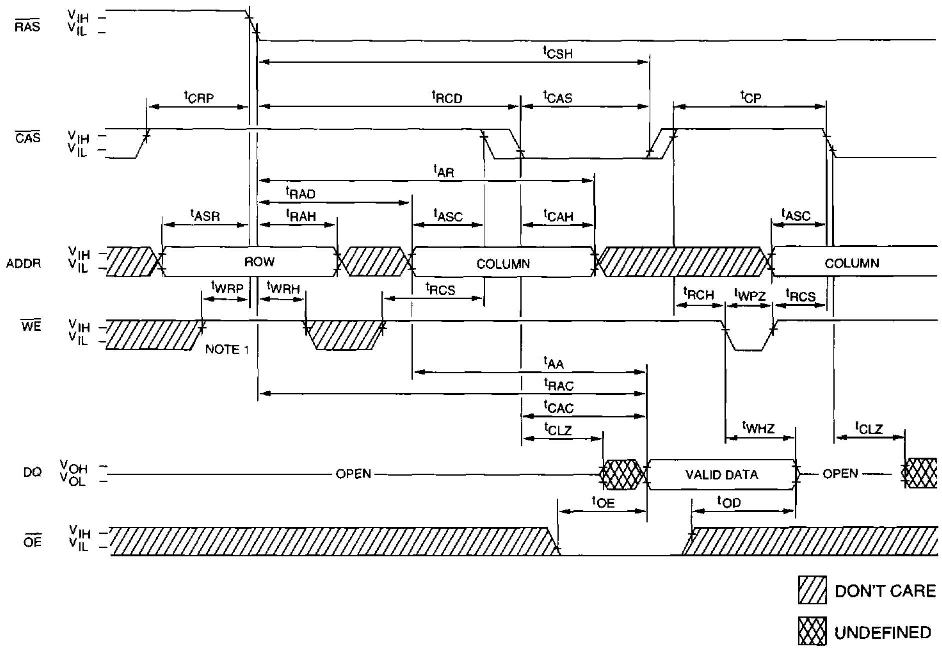


HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.