Microelectronic Integrated Systems

MLX90129

13.56MHZ SENSOR TAG IC

Features and Benefits

- □ Versatile A/D interface for resistive sensors
- □ ISO-15693 13.56MHz transponder
- □ Slave / Master SPI interface
- □ 4 k-bit EEPROM with access protection
- □ Standalone data-logging mode
- □ Ultra low power
- □ Battery or battery-less applications
- □ Low cost and compact design

Application Examples

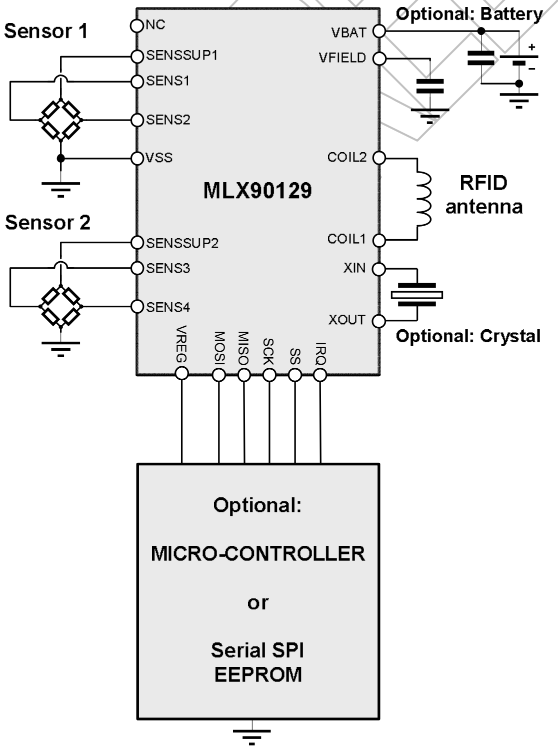
- □ Cold chain monitoring
- □ Asset management and monitoring (security and integrity)
- □ Building automation
- □ Industrial, medical and residential control and monitoring

Ordering Information [1]

Part No.	Temperature suffix	Package Code	Option code
MLX90129	K (-40°C to 125°C)	GO [TSSOP 20]	-
MLX90129	K (-40°C to 125°C)	LQ [QFN 20 (4mm x 4mm)]	-

[1] Example: MLX90129KGO

1 Functional Diagram



2 General Description

The MLX90129 combines a precise acquisition chain for external resistive sensors, with a wide range of interface possibilities.

It can be accessed and controlled through its ISO15693 RFID front-end or via its SPI port.

Without any other component than a 13,56MHz tuned antenna, it becomes a RFID thermometer.

For measuring others physical quantities, one or two resistive sensors can be connected to make batteryless sensing point. In this tag mode, the chip can supply a regulated voltage to the other components of the application.

Adding a battery will enable the use of the standalone data logging mode. The sensor output data is stored in the internal 3.5kbits user memory. One can extend the storage capacity by connecting an external E2PROM to the SPI port.

The SPI port can also connect the MLX90129 to a microcontroller which allows more specific applications, like adding actuating capability or RF transmission.

The MLX90129 has been optimized for low power, low voltage battery and battery-less applications.

3 Glossary of Terms

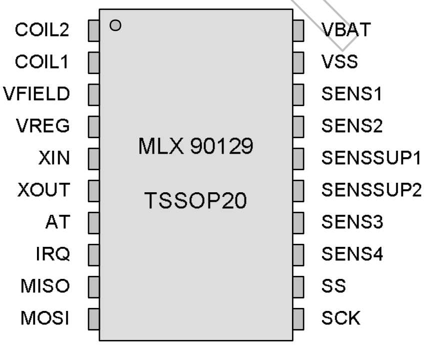
EEPROM	Electrically Erasable Programmable Read-Only Memory
DMA	Direct Memory Access
PGA	Programmable Gain Amplifier
LFO	Low Frequency Oscillator
XLFO	Crystal Low Frequency Oscillator
CTC	Contactless Tuning Capacitance

4 Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage, V_{BAT} (maximum rating)	14	V
Reverse Voltage Protection	-0.5	V
Maximum output voltage on pad VFIELD	13	V
Operating Temperature Range, T_A	-40 to +125	°C
Storage Temperature Range, T_S	150	°C
ESD Sensitivity (AEC Q100 002)	4	kV

Exceeding the absolute maximum ratings may cause permanent damage.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5 Pin definition



Pin	Symbol	I/O	Description
1	COIL2	B	Coil terminal 2 for RFID interface
2	COIL1	B	Coil terminal 1 for RFID interface
3	VFIELD	O	Unregulated supply voltage (from RF field)
4	VREG	O	Regulated supply voltage
5	XIN	I	Crystal oscillator input 1
6	XOUT	I	Crystal oscillator input 2
7	AT	I	Anti Theft (to connect to ground)
8	IRQ	O	Interrupt output
9	MISO	B	SPI Master In Slave Out
10	MOSI	B	SPI Master Out Slave In
11	SCK	B	SPI Serial Clock
12	SS	B	SPI Slave Select
13	SENS4	I	Sensor 2 input 2
14	SENS3	I	Sensor 2 input 1
15	SENSSUP2	O	Sensor 2 supply
16	SENSSUP1	O	Sensor 1 supply
17	SENS2	I	Sensor 1 input 2
18	SENS1	I	Sensor 1 input 1
19	VSS	I	Ground
20	VBAT	I	Battery supply

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6 General Electrical Specifications

DC Operating Parameters T_A = -40°C to 125°C, V_{VBAT}=4V (unless otherwise specified)

6.1 Power consumption

DC Operating Conditions (T = -40°C to 125°C, V_{VREG} = 2.2V to 3.0V)

Parameter	Conditions	MIN	TYP	MAX	Unit
Current consumption on battery in "Stand-by" mode		-	0.5	tbd	µA
Current consumption in "Sleep" mode	(Using the RC-oscillator)	-	1.5	tbd	µA
Current consumption in "Watchful" mode		-	100	tbd	µA
Current consumption in "Run" mode	EEPROM writing Sense & Convert	- 300	80 500	- 600	µA µA

6.2 RFID interface

DC Operating Conditions (T = -40°C to 125°C)

Parameter	Conditions	MIN	TYP	MAX	Unit
Programmable resonance capacitance	Once trimmed	73	75	77	pF
Quality factor Qc of the capacitor	Fcarrier = 13.56MHz	100			-
Capacitance trimming step		0.5	0.7	1.0	pF
Minimum coil AC voltage (for operation)		3			V_{peak}
Maximum clamping voltage				14	V_{peak}
Downlink & Uplink Data rate			26		kBit

6.3 SPI: electrical specification

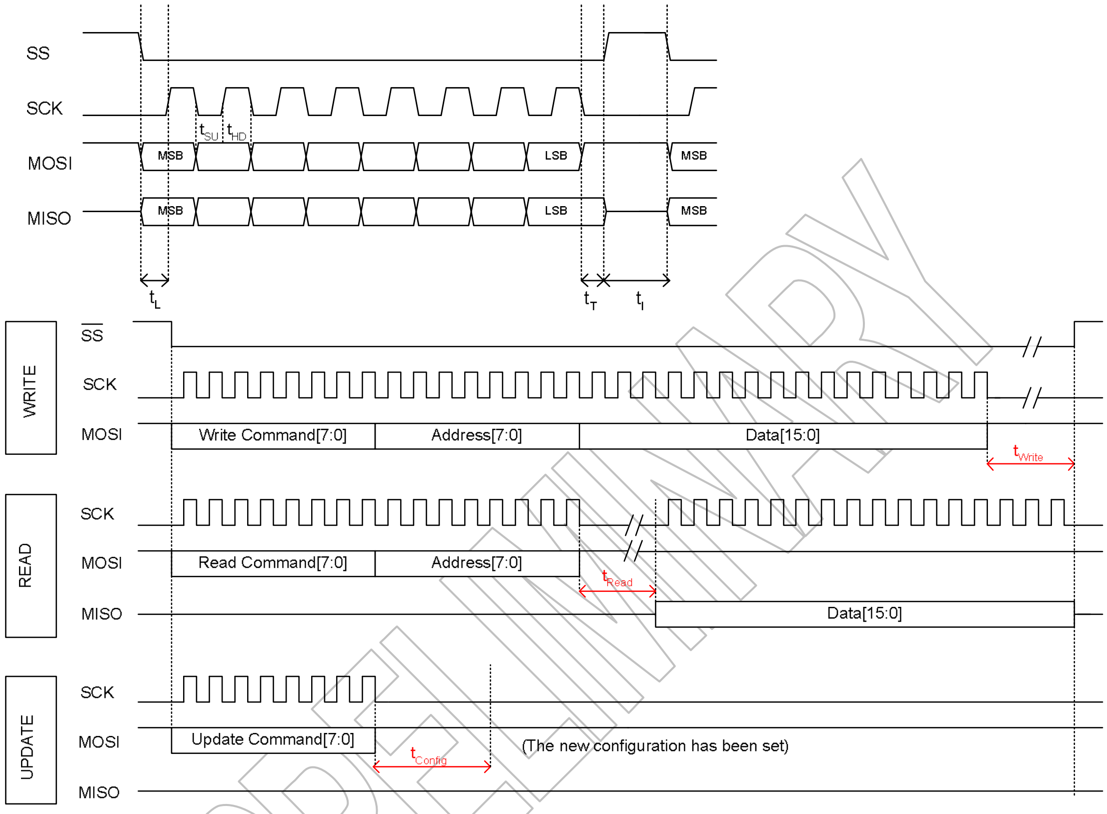
DC Operating Conditions (T = -40°C to 125°C)

Parameter	Description	Min	Typ	Max	unit
VDD	Power supply voltage (master side)	2.4	3.0	3.5	V
VIH	Input High Voltage	0.7*VDD	VDD	VDD + 0.5	V
VIL	Input Low Voltage	-0.3	0	0.3*VDD	V
VOH	Output High Voltage @ IOH = -2 mA	VDD-0.8		-	V
VOL	Output Low Voltage @ IOL = 2 mA	-		0.4	V
VHYS	Input Hysteresis	0.05*VDD		-	V

6.4 Non-volatile memories

Parameter	Description	Min	Typ	Max	unit
DataRet85	Data retention at 85°C	10			year
Cyclenb25	Number of program cycles at 25°C	100000			-
Cyclenb125	Number of program cycles at 125°C	10000			-

6.5 Slave SPI: timing specification



Timing specifications

Parameter	Description	Slave side		Units
		Min	Max	
tch	SCK high time	500	-	ns
tcl	SCK low time	500	-	ns
t_{Read} (**)	Delay to read a register word Delay to read an EEPROM word Delay to read an EE-Latch word Delay to get the ADC output code	2 32 2 430	- - - (*)	µs
t_{Write} (**)	Delay to write a register word Delay to write an EEPROM word Delay to read an EE-Latch word	- 8 4	- 16 8	ms
t_{Config}	Execution delay for commands *Update*	-	1	ms
t_{SU}	Setup time of data, after a falling edge of SCK	0	500	ns
t_{HD}	Hold time of data, after a rising edge of SCK	0	500	ns
t_L	Leading time before the first SCK edge (in clock pulses) _ when the MLX90129 is not in sleep mode _ when the MLX90129 is in sleep mode (***)	 3 1.5	 - -	 clk ms
t_T	Trailing time after the last SCK edge	0	-	ns
t_I	Idling time between transfers (SS=1 time)	0	-	ns

(*) – the conversion time depends on the programmed initialization time and on the ADC options. When the conversion is finished, the flag *Sensor Data Ready* is set.
(**) For the Read/Write Internal Devices commands, the delay depends on the nature of the so-called Internal Device: (Register, EE-Latch bank, ADC,…)
(***) – See the power management chapter to know when the MLX90129 may be in sleep mode

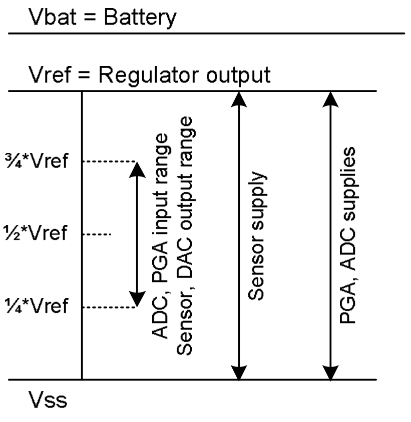
6.6 Master SPI timing specifications

Parameter	Description	Slave side			Units
		Min	Nom	Max	
tch	SCK high time		400		ns
tcl	SCK low time		400		ns
t_{Read}	Read EEPROM time		0.4		µs
t_{Write}	Erase or Write EEPROM time	1		28	ms
t_{SU}	Setup time of data, after a falling edge of SCK		400		ns
t_{HD}	Hold time of data, after a rising edge of SCK		400		ns
t_L	Leading time before the first SCK edge		200		µs
t_T	Trailing time after the last SCK edge		200		ns
t_I	Idling time between transfers (SS=1 time)		1600		ns

6.7 Sensor Signal Conditioner: electrical specifications

-40℃ < Temp < 125℃, unless otherwise specified. The sensor is supplied by a regulated voltage called $V_{ref.}$

Parameter	Symbol	Conditions / Comment	Min	Typ	Max	Unit
GENERAL CHARACTERISTICS						
Battery voltage	Vbat	Low-volt option not activated Low-volt option activated	tbd tbd	4.0 3.0	14.0 14.0	V
Temperature range	Temp_rg		-40		+125	℃
SENSOR ADJUSTMENT CAPABILITY						
Reference voltage V_{ref} (2)	Sens_VRef	Low-volt option = 0 Low-volt option = 1	3.0 2.0	3.1 2.1	3.2 2.2	V
Full Span (3)	Sens_FS	Full scale of the sensor output voltage (Sens_CM is at the specified value)	$\pm V_{ref}$ /1200	-	$\pm V_{ref}/16$	V
Zero offset (1)(3)	Sens_Off		0	-	± ½.V_{ref}	V
Common-mode voltage	Sens_CM		0.3*V_{ref}	½.V_{ref}	0.7*V_{ref}	V
External sensor resistance	Sens_Res		0.5	-	-	kΩ



Notes:

(1): The capability of adjustment of the input offset depends on the selected gain of the first Programmable Gain Amplifier (PGA1).
(2): The reference voltages of the ADC, of the DAC and the supply voltage of the sensors are ratio-metric.
(3): Full span is defined as the maximal sensor differential output voltage: $\Delta V(\text{sensor output})_{max}$.

PARAMETER	SYMBOL	CONDITIONS / COMMENT	MIN	TYP	MAX	UNITS
PROGRAMMABLE-GAIN AMPLIFIER PGA1						
Gain	PGA1_Gain	Code PGA1gain[3:0] =				V/V
		0000		8		
		0001		10		
		0010		12.6		
		0011		15.5		
		0100		19.6		
		0101		24.5		
		0110		30.8		
		0111		38.1		
		1000		47.6		
		1001		59.4		
		1010 to 1111		75.3		
PROGRAMMABLE-GAIN AMPLIFIER PGA2						
Gain	PGA2_Gain	Code PGA2gain[2:0] =				V/V
		000		1		
		001		2		
		010		3		
		011		4		
		100		5		
		101		6		
		110		7		
		111		8		
PGA1 + PGA2 + DAC						
Gain range	PGA_Gain		8		600	V/V
Sensor offset trimming range	PGA_Off_R	(= offset max of the sensor)	0		$V_{ref}/16$	V
Sensor offset trimming step	PGA_Off_S	8-bits DAC (7 bits + sign) Ratio-metric, to cancel the offset of the sensor		$V_{ref}/256$		V
Differential input range	PGA_Dir	Gain (PGA) = 1 (if higher, PGA_Dir should be divided by the gain)		$V_{ref}/16$		V
Differential output range	PGA_Dor			½.V_{ref}		V
Common-Mode input	PGA_Cmir		0.3*V_{ref}	½.V_{ref}	0.7*V_{ref}	V
DAC (differential outputs)						
Resolution	Dac_Res	7 bits + 1 bit sign		8		bit
Differential output range	Dac_Org			½.V_{ref}		V
INL	Dac_Inl		0		0.5	lsb
DNL	Dac_Dnl		0		0.5	lsb

PARAMETER	SYMBOL	CONDITIONS / COMMENT	MIN	TYP	MAX	UNITS
BRIDGE SUPPLIES & REFERENCES						
Reference serial resistance	Ref_Res	6 bits-programmable	0.4		64	kΩ
INTERNAL TEMPERATURE SENSOR						
Full scale	ITS_FS		-40		+125	℃
Output range	ITS_Or	ΔTemp = 170℃, ΔVout =	tbd	0.2	tbd	V
Offset	ITS_Off	T = 20℃,		20		mV
Sensitivity	ITS_Sens	ΔVout / ΔTemp =	tbd	1.2	tbd	mV/°
Non-linearity (without calibration)	ITS_LinErr	ΔTemp = 150℃ ($T_{(measured)}$ - $T_{(extrapolated)}$) =	-	±1	tbd	℃

ADC

The *MODE[1:0]* bits controls the tradeoff between the duration of the counting phase and the resolution. Mode 00 is the fastest but also the least accurate mode whereas the mode 11 is the most accurate but the slowest. The *LOW_POWER* bit allows the user to reduce the power consumption of the analog

ADC parameter	Mode 00	Mode 01	Mode 10	Mode 11	Unit
ENOB: effective number of bits	tbd	tbd	tbd	11	bit
INL: Integral linearity error	tbd	tbd	tbd	+/- 20	lsb
DNL: Differential linearity error	tbd	tbd	tbd	tbd	lsb
Offset error	tbd	tbd	tbd	3	lsb
Conversion time (*) in normal power mode Conversion time (*) in low power mode	tbd	tbd	tbd	tbd	µs

(*): To get the sampling rate of the system, the initialization time must be added to the conversion time. This time is programmable as it depends on the selected sensor (by default it is 150 µs).

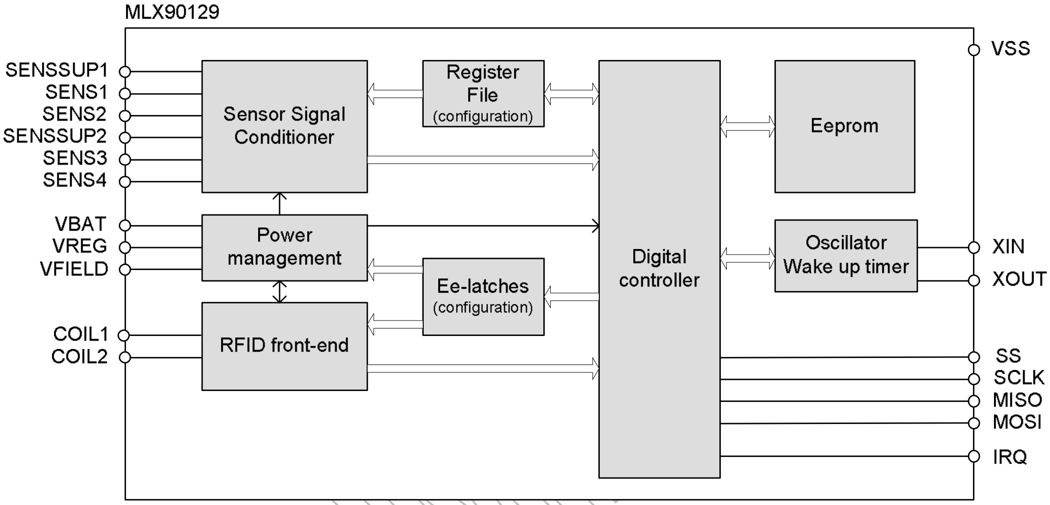
6.8 VREG regulator and battery monitoring: electrical specifications

PARAMETER	SYMBOL	CONDITIONS / COMMENT	MIN	TYP	MAX	UNITS
VREG REGULATOR						
Output voltage	Vreg_Vlow Vreg_Vhigh	Low-voltage option High-voltage option	2.0 2.8	2.2 3.0	2.4 3.2	V V
Output max. current	Vreg_Imax	200mV voltage loss on VREG 500mV voltage loss on VREG	tbd tbd	6.0 10.0	tbd tbd	mA mA
External capacitor	Vreg_Capa	Stable smoothed signal	0	-	10	µF

BATTERY LEVEL MONITOR CIRCUIT						
Threshold	Bmc_Thres		tbd	1.9	tbd	V

7 Detailed General Description

7.1 Block diagram



The ***sensor signal conditioner*** is used to amplify, filter and convert the output voltage of resistive sensors. They may be an external single-ended or differential resistive sensor, or the internal temperature sensor. The two external sensors are supplied by a stable reference voltage, provided by an integrated voltage regulator. The sensor output voltage is amplified thanks to a programmable-gain amplifier, and has its offset voltage compensated. Then, the conditioned sensor signal fits the input range of the A/D converter. The ADC converts the signal in a 16-bits code that can be stored or transmitted.

The ***power management*** unit deals with the different power modes of the chip: it monitors the battery level, scavenges the energy coming from a RFID 13,56MHz field and makes the power-on reset signal. A regulator is used to supply the digital parts, but can also be used to supply some other external devices.

The ***Oscillators block*** contains different kind of oscillators: a very low power, low frequency 1-kHz R-C oscillator used as a wake-up timer, a low-power 32-kHz quartz oscillator that can be used for an accurate time basis, and a high frequency 5-MHz R-C oscillator used for the digital controller.

The ***Register File*** contains all the configuration parameters of the chip. It may be loaded from the EEPROM after power-on, or as the result of a specific request from RFID or SPI.

The ***RFID front-end*** receives an external 13,56-MHz magnetic field, sensed on an external antenna coil. The antenna design is made easy thanks to an internal programmable high-Q capacitance (tuned during the test phase). From the antenna output voltage, it makes a stable clamped DC supply voltage, recovers the clock, and controls the modulation of the carrier and the demodulation of the incoming signal.

The ***EEPROM*** is a 4-kbits non-volatile memory, organized as 256 words of 16 bits divided in 39 reserved for configuration, 2 for default trimming value (*EE-Latches #03 and #09*) backup and 215 available for the application (around 3.4 kbits user memory). Its access is protected by several security levels. Some *EE-Latches* are also used when the stored data have to be immediately available for use.

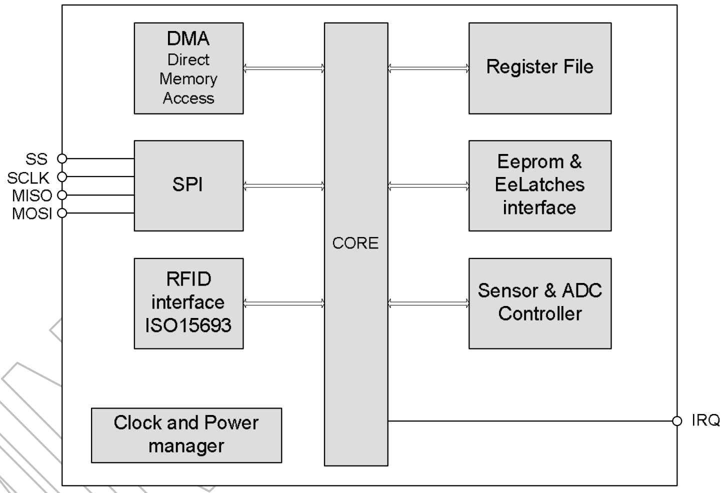
The ***Digital Controller*** manages the accesses of the different interfaces (SPI, RFID) with the different memories (EEPROM, register file) and the sensor. It comprises the RFID ISO-15693 and SPI protocols, controls the sensor signal conditioner and stores or sends the ADC output code. It can also run some standalone applications, thanks to its unit called *Direct Memory Access* (DMA).

7.2 Digital Controller and memory domains

7.2.1 Digital controller

The main features of the digital part of MLX90129, called *Digital Controller* are:

- Slave / Master SPI interface
- RFID interface
- DMA: Direct Memory Access
- Register File controller
- EEPROM controller
- Sensor interface controller
- Clock and Power management
- Core: transactions arbiter and interrupt manager



The digital controller manages the transactions between the communication interfaces, the memories and the sensor. It allows also a standalone mode with its DMA unit. All these blocks are explained in the next chapters.

The SPI and RFID communication ways can be used concurrently. The *Core transaction arbiter* handles the priorities and the interrupts. It updates some status bits that may be used by the external microcontroller or the RFID base-station to optimize the communication.

The *Digital Controller* of the MLX90129 allows the user to do the following tasks, via SPI or RFID:
_ Configure the sensor interface and the communication media.
_ Manage the power consumption, the interrupts, the security items,…
_ Run A/D conversions of the selected sensors.
_ Store (or read) data in the internal or in an external EEPROM.
_ Configure and start a standalone process (sleep – sense – interrupt or store – sleep - …)
_ Get the status of the current process.

All these tasks may be done by simply reading or writing the different memories: EEPROM, registers, ee-Latches, internal devices. Thus, several address domains are defined to access them in an easy way.

7.2.2 Address domains

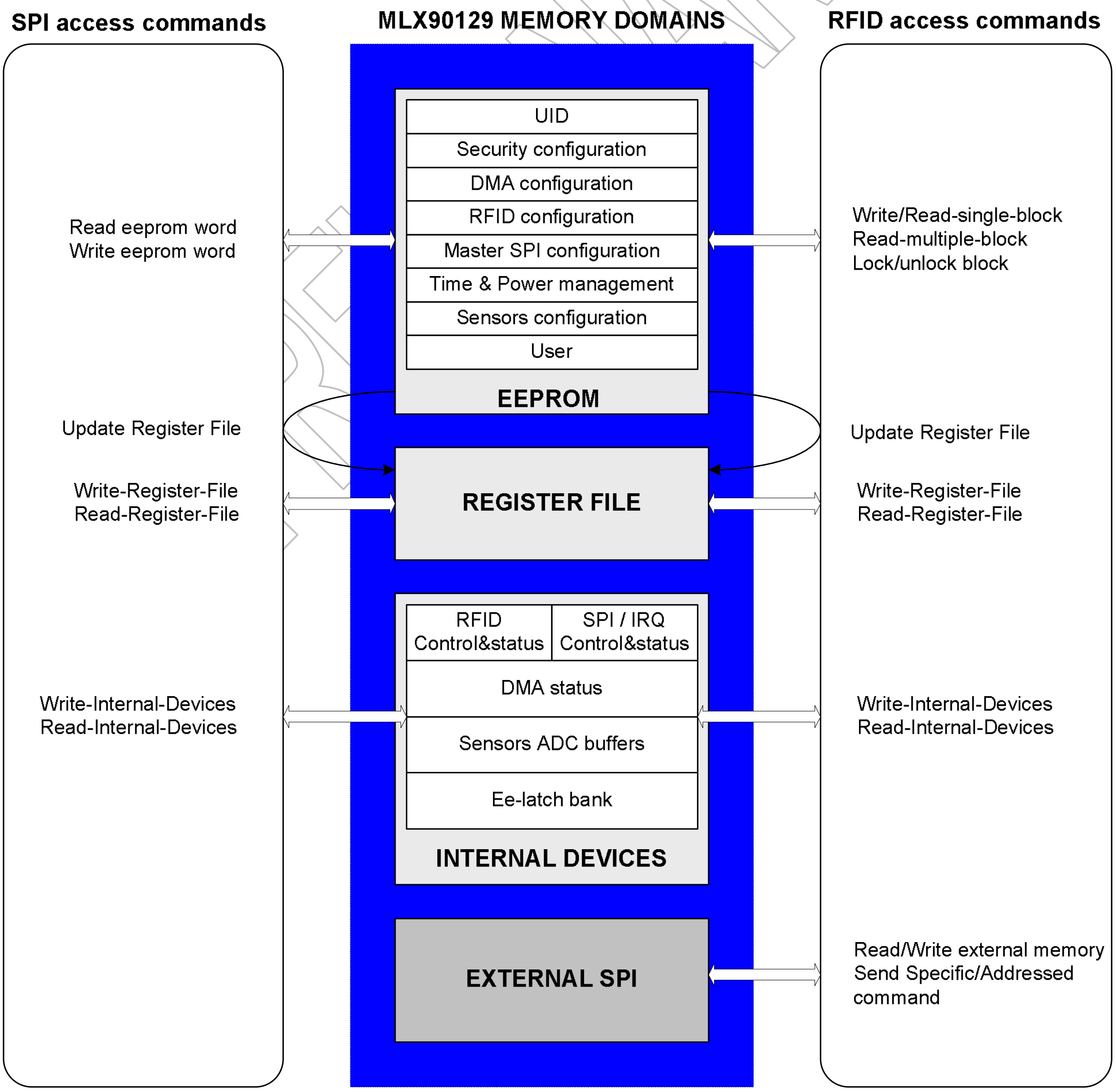
Four address domains have been defined to designate the memory and the non-memory devices that act during the requested transactions:

- ***Register File address domain***:
This memory domain is used to store the current configuration information of all internal MLX90129 devices (Sensor interface, Power management …). This memory is energy-dependent and must be updated each time the MLX90129 is turned-on.

- ***EEPROM address domain***:
This domain addresses the non-volatile EEPROM. It is used to store the user-defined data and the image of the *Register File* that can be automatically downloaded after a power-on. This memory block is energy independent and can store data even when the MLX90129 is no longer powered.

- ***External memory address domain***:
This domain addresses the external memory which can be connected to the MLX90129, using the SPI in master mode.

- ***Devices address domain***:
This domain allows accessing the registers linked to the so-called *internal devices* like the ADC buffer, the status words of the *Core Transaction Arbiter*, the EE-Latch bank... One of them may be accessed with the appropriate SPI / RFID commands including its address. The difference with the Register File is the fact that they are not copied from the EEPROM at the start-up, and they may be used during the requested transaction.



7.2.3 Internal Devices

The term *Internal Devices* designates the registers used to configure the main “non-memory” digital units: sensor interface, SPI / RFID interfaces, DMA … All these registers are part of the *Internal Device Address Domain*:

The registers linked to the SPI and RFID interfaces, called *SPI/RFID core control word* and *SPI/RFID core interrupt/status word* have the same definition, but are physically different and may contain some different data. The content of these registers are explained in the following chapters (SPI, RFID). Some of these bits may be used to avoid conflicts for the memories access, when communicating with SPI and RFID at the same time. For that, they can be accessed at any time via SPI or RFID.

The SPI / RFID local buffers store the result data of the last transaction. They are useful for example when the A/D conversion time is too long and does not fit the timing requirements of the RFID protocol.

The *EE-Latches* and the *Contactless-tuning capacitance* code contain some non-volatile data, immediately available (no delay, no supply), used for the RFID capacitance trimming or for the options of the power management.

The registers of the DMA unit called *Current destination address* are used to give a status of the process (the number of words that have been registered, …).

The content of the *ADC buffer* depends on the selection byte (Address) used within the *Read/Write Device* command: it may be the data from the internal temperature sensor, or from one of the two external sensors. After receiving a *Read Device* command (from RFID or SPI, with the appropriate address), the MLX90129 supplies the selected sensor and its interface, converts its output in a digital format, and stores it in the appropriate *ADC Buffer*. The data is also available in the SPI / RFID local buffer.

The CTC is the code used to program the RFID antenna capacitance, according to the specifications.

Map of the *Internal Device Address Domain*

Address	Bits	From SPI side	From RFID side
SPI / RFID			
0x00	15:0	SPI core control word	RFID core control word
0x01	15:0	SPI core interrupt / status word (read only)	RFID core interrupt / status word (read only)
0x02	15:0	SPI local buffer (read only)	RFID local buffer (read only)
Non-volatile memory			
0x03	15:0	EE-Latches word 0	EE-Latches word 0
0x04	15:0	EE-Latches word 1	EE-Latches word 1
Direct Memory Access (DMA)			
0x05	15:0	Current destination address (read only)	Current destination address (read only)
Sensor			
0x06	15:0	ADC buffer 0	ADC buffer 0
0x07	15:0	ADC buffer 1	ADC buffer 1
0x08	15:0	ADC buffer 2	ADC buffer 2
Contactless-tuning capacitance (CTC)			
0x09	15:0	CTC code	CTC code

Note:
The *internal devices* having the addresses 0x00, 0x01, 0x02, 0x05 are registers. Those having the addresses 0x03, 0x04, 0x09 are ee-Latches, and those whose addresses are 0x06, 0x07, and 0x08 refer to the ADC output buffers. The read / write delays are specified for all kind of *internal devices*, when accessing them via SPI.

7.3 Core Transaction Arbiter

Part of the *Digital Controller*, the *"Core transaction arbiter"* deals with several tasks:

- Grant or deny accesses of the communication interfaces to the different memories
- Manage the interrupts
- Update the status of the current operations

7.3.1 Communication security

The *Device Security Register* is stored in the EEPROM. It contains the access rights to the different memories by the RFID interface. It allows a partial or complete disabling of the RFID interface. In addition, it controls the functionality of the SPI by making it master or slave.

Device security map configuration register (EEPROM & Register, address **#05**, Read/Write)

Bits	**Name**	**Description** (when bit = 1)
15:14	-	Reserved (must be 00)
13	Rfid_Page0Read	Allow read access to Register file page 0 for RFID.
12	Rfid_Page0Write	Allow write access to Register file page 0 for RFID.*
11	Rfid_EEpViaDma	Allows RFID access to internal EEPROM via DMA.
10	Rfid_Adc_Access	Allow access to ADC buffer for RFID
9	Rfid_ Ext_Read	Allow a read access to the external memory by RFID
8	Rfid_ Ext_Write	Allow a read & write access to the external memory by RFID *
7	Rfid_EEl_Read	Allow a read access to EE-Latches by RFID
6	Rfid_EEl_Write	Allow a read & write access to EE-Latches by RFID *
5	Rfid_Reg_Read	Allow a read access to the *Register file* page 1by RFID
4	Rfid_Reg_Write	Allow a read & write access to the *Register* file page 1 by RFID *
3	Rfid_Lock_Dis	Disable the RFID Core-lock access function
2	Rfid_LockUn_En	Disable the RFID Lock / Unlock functions (for memory)
1	Rfid_Dis	Disable the RFID communication media
0	Spi_Master	SPI slave disable. Disables SPI-slave and enables activity of SPI-master.

- note: if the write-access is allowed, the read-access is also allowed, independently of the value of the *read access* bit

7.3.2 Management of communication conflicts

Memory access conflicts between SPI, RFID and DMA

The two communication channels, SPI and RFID, and the internal DMA (*Direct Memory Access*) are able to access the memories (EEPROM, registers…) or the sensor *ADC buffer*, at the same time. The potential access conflicts are managed by the *Core transaction arbiter.* A DMA transaction may be interrupted by a RFID or a SPI starting communication. The RFID (resp. SPI) transaction cannot be interrupted by a starting SPI (resp. RFID) communication, or a DMA operation. In each case, the current transaction is completed.
The priority order is the following:

1. SPI (highest priority)
2. RFID
3. DMA

Management of two subsequent transactions, from the same communication channel:

A transaction initiated via RFID or SPI should be completed before starting a new one. If a request is sent to the MLX90129 by a SPI master, or by a RFID base-station, and the current transaction is not completed, then it is dealt differently depending on its nature:
_ the reading of the *Core interrupt / status word* is allowed at any time and its content is sent in the response.
_ the reading of a memory (a register or an EEPROM word) is denied and an error-message response may be sent. For the SPI, it contains 0xFFFF. For the RFID, the content of the response is described in the standard protocol.
_ if the request is not understood, it is not processed, and a flag is set in the *Core interrupt / status word* . This flag is reset once it has been read.

The Core interrupt / status word (Internal device #01)

The *Core transaction arbiter* updates its *Core interrupt / status word* at each transaction. This status word is read-only and contains some information about the processing of the incoming request. It indicates:
_ whether the system is busy or not
_ whether the last request has been processed
_ whether the processing of the last request has failed
_ the source(s) of the interrupt, if the interrupt signal on pin IRQ is asserted '1'.
One *Core interrupt / status word* is associated to each communication way (SPI or RFID). Its content is explained in the chapters dedicated to RFID and to SPI.

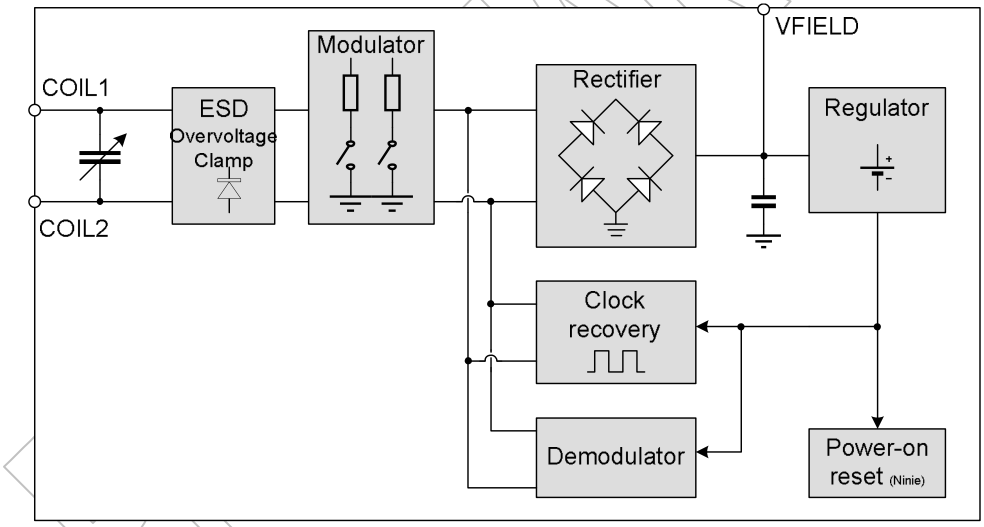
The Core Control Word (Internal device #00)

The *Core transaction arbiter* updates its *Core control word* at each transaction. This status word is read/write and contains the settings used to control the interrupt signal IRQ, and the potential interrupts from other communication channel. One *Core control word* is associated to each communication way (SPI or RFID). Its content is explained in the chapters dedicated to RFID and to SPI.

7.4 RFID communication

7.4.1 RFID analog front-end

The MLX90129 RFID interface complies with the ISO-15693 layer1 requirements. It is accessed by the RFID base-station (reader) in modulating the 13.56 MHz carrier frequency. The data are recovered from the signal amplitude modulation (ASK, Amplitude Shift Keying 10% or 100%). The Data transfer rate is 26 kBit/s using the 1/4 pulse-coding mode.
The outgoing data are generated by an antenna load variation, using the Manchester coding, and using one or two sub-carrier frequencies at 423 kHz and 484 kHz. The data transfer rate is 26 k-Bit/s in the fast data-rate mode. From the incoming field, the RFID interface recovers the clock and makes its own power supply. The rectified voltage may also be used to supply the whole device in battery-less applications.



7.4.2 ISO-15693 Features and Command set

For complete information about the communication protocol, please refer to the standard document:
ISO/IEC FCD 15693-2 and ISO/IEC FCD 15693-3: **Identification cards- contactless integrated circuit(s) cards - Vicinity cards -** It is available on the website: http://www.iso.org
Some of the features of the protocol are not supported. Furthermore, some “custom” commands have been defined (see Command set).

Summary of the main, supported features

Features	Supported	Not supported
Reader to Tag Modulation Index	10% and 100%	
Reader to Tag Coding	Pulse Position Modulation: 1 out of 4	PPM: 1 out of 256
Tag to Reader Modulation	Single and dual Sub-carrier	
Tag to Reader Sub-Carrier	423 kHz / 484 kHz	
Tag to Reader Coding	Manchester	
Tag to Reader Data-rate	High Data-rate 26 kBit	Low Data-rate 6 kBit

Summary of the main, supported protocol parts

- Data element

Data Element	Supported
UID (Unique Identifier)	Yes
AFI (Application Family Identifier)	No
DSFID (Data Storage Format Identifier)	No
CRC	Yes
Security status	No

- Protocol

Request Flag	Supported
Sub-Carriers	Yes
Data-rates	No
Inventory	Yes
Select	Yes
Address	Yes
Options	No
Nb slot	Yes
Response Flag	**Supported**
Error	Yes

- Anti-collision: Supported

Command frame

The content of the data included in the frame of a communication request, and the response from the MLX90129 to the base-station depends on the command opcode. The meaning of the flags, the equation of the CRC, the description of the Start-Of-Frame, the End-Of-Frame and the unique identifier number (UID), the meaning of the error codes… are included in the standard ISO-15693 layers 2 and 3.

Request format:

SOF	Flags	Command	(UID)	(Data)	CRC 16	EOF
	8 bits	8 bits	64 bits	x bits	16 bits	
	00XX 0X1X	XXXXXXXX	Optional			

Response format (if no error):

SOF	Flags	(Data)	CRC 16	EOF
	8 bits	x bits	16 bits	
	00			

Command set

The command set lists the mandatory commands defined in the standard ISO-15693 layer 3. It comprises also some custom commands used for some specific applications: access the sensor buffer, access an external device via SPI, handles the security options,…

ISO-15693 mandatory commands

Commands	code	Description
Inventory	01	Enable an anti-collision sequence
Stay quiet	02	Enable the '*Stay Quiet'* mode
Read single block	20	Read a single word from EEPROM
Write single block	21	Write a single word to EEPROM
Lock Block	22	Lock a page of EEPROM
Read multiple block	23	Read one or several contiguous blocks of the EEPROM
Select	25	Enter the "Selected" state (anti-collision)
Reset to ready	26	Return to the '*Ready*' mode

Custom commands

Commands	code	Description
Read register file	A0	Read one word from the *Register file*
Write register file	A1	Write one word to the *Register file*
Read internal device	A2	Read the content of an *internal device* identified by an address byte
Write internal device	A3	Write the register word of an *internal device*, identified by an address byte
Read external memory	A4	Read a word from an external memory (via SPI)
Write external memory	A5	Write a word into an external memory (via SPI)
Send specific command	A6	Send a command via SPI to an external device, whose code is appended to the frame (e.g. Write Enable for an external EEPROM).
Send addressed specific command	A7	Send a command via SPI to an external device, whose code and address are appended to the frame (e.g. *Lock Block* for an external EEPROM)
Write external memory status	A8	Send a command via SPI, to write an external memory status register (The op-code of this command is stored in a register)
Read external memory status	A9	Send a command via SPI, to read an external memory status register (The op-code of this command is stored in a register)
Lock device	B0	Lock an *internal device* (EEPROM, ADC, …), preventing its access.
Unlock device	B1	Unlock an *internal device*
Update Register File	C0	Fill the *Register File* with the image from the EEPROM, without re-boot
Unlock Block	F0	Unlock a locked page of EEPROM.

Frame content

Commands	Data in request (in order of apparition)	Data in response (when no error occurs)	Possible error codes
Inventory	Mask length (8 bits) Mask value (0 – 64 bits)	UID (64 bits)	0X, AX
Stay quiet	UID (64 bits)	No response	None
Read single block Read register file	Optional: UID (64 bits) Block address (8 bits)	Read block (16 bits)	0X, 10, AX
Write single block Write register file	Optional: UID (64 bits) Block address (8 bits) Data (16 bits)	No data	0X, 10, 12, 13, AX
Lock Block	Optional: UID (64 bits) Block address (8 bits)	No data	0X, 10, 11, AX
Read multiple block	Optional: UID (64 bits) First block address (8 bits) Number of blocks (8 bits)	Read blocks (N*16 bits)	0X, 10, AX
Reset to ready	UID (64 bits)	No data	0X, AX
Select	UID (64 bits)	No data	0X, AX
Read internal device	Optional: UID (64 bits) Address (8 bits)	Data (16 bits)	0X, AX
Write internal device	Optional: UID (64 bits) Address (8 bits) Data (16 bits)	No data	0X, AX
Read external memory	Optional: UID (64 bits) Read command op-code (8 bits) Block address (8 bits)	Data (16 bits)	0X, AX
Write external memory	Optional: UID (64 bits) Write command op-code (8 bits) Block address (16 bits) Data (16 bits)	No data	0X, AX
Send specific command	Optional: UID (64 bits) Command op-code (8 bits)	No data	0X, AX
Send addressed specific command	Optional: UID (64 bits) Command op-code (8 bits) Address (16 bits)	No data	0X, AX
Write external memory status	Optional: UID (64 bits) Command op-code (8 bits) Data (8 bits)	No data	0X, AX
Read external memory status	Optional: UID (64 bits) Command op-code (8 bits)	Data (8 bits)	0X, AX
Lock device	Optional: UID (64 bits) Address (8 bits)	No data	0X, AX
Unlock device	Optional: UID (64 bits) Security password (16 bits) Address (8 bits)	Response data (16 bits)	03, 0X, AX
Update Register File	Optional: UID (64 bits)	No data	03, A0, A1
Unlock Block	Optional: UID (64 bits) Security password (16 bits) Address (8 bits)	Always an error code	01

Response error code

If the flag *Error_flag* of the response is set by the MLX90129, the error code is transmitted to provide some information about the error that occurred. Most of them are described in the standard ISO15693. The last ones are some custom codes.

Error code	Meaning	FWT	Command
01	The command is not supported, i.e. the request code is not recognized	Short	All
02	The command is not recognized, for example: a format error occurred	Short	All
03	The option is not supported	Short	All
0F	Unknown error	Short	All
10	The specified block is not available (does not exist)	Short	Read/Write/Lock
11	The specified block is already locked and thus cannot be locked again	Short	Lock
12	The specified block is locked and its content cannot be changed	Short	Write
A0	The selected *Internal Device* is locked	Short	Write int. device
A1	The selected *Internal Device* is busy (*)	Short	Read/Write internal device
A2	The access to the selected *Internal Device* is denied	Short	Read/Write internal device

(*) "Device is busy" error code occurring during a write operation means that the MLX90129 is still performing the last write operation. Then, the base-station has to wait for some time and send the command again. For read operation, it means that the selected *Internal device* (sensor ADC, …) cannot read the data and respond immediately.

7.4.3 Internal Devices dedicated to RFID communication

Using the RFID (and SPI) commands called *Read-internal-device* and *Write-internal-device,* it is possible to access some registers of the *Device Address Domain*. These registers contain some status information, some settings and options, the ADC buffer of the selected sensor, the ee-Latches, etc… This so-called *Internal Device* is selected thanks to the address byte included in the command. The addresses and the access rights of the *Internal Devices* are listed in the chapter: *Core transaction arbiter*.

The following words are parts of the *Device address domain*:

- The *RFID core control word* is read/write. It contains a bit used to lock the non-RFID transactions.
- The *RFID interrupt & status word* is read-only, using the RFID command *Read internal device*, and the address 0x00. It contains the status of the security units, of the pending accesses to the memories, and of the system current activity.

RFID core control word (*Devices address domain*, address **#00**, read/write)

Bits	Name	Description (when = 1)
15:1	-	Unused (must be 0)
0	**Core_Lock**	When set to '1', it locks any transactions including the SPI interface or the DMA. This allows having an access from the RFID interface at any time. If the base station sets this bit, but the last transaction has not been accomplished yet, this latter is not interrupted. But it is still possible to access the *Device Address Domain*, via SPI.

RFID interrupt & status word (*Devices address domain*, address **#01**, read-only)

Bits	Name	Description, if bit=1
15	(reserved)	
14	**Irq_LowBattery**	Low battery voltage detected
13	**Irq_SensorFault**	Sensor fault detected (bridge is broken or short-cut)
12	**Irq_ExternalEvent**	An external event has been detected (rising edge on pin NC). (The event detector must be activated and enabled)
11	(reserved)	
10:8	(unused)	
7	**Irq_Sensor_Threshold**	The output data from the sensor has crossed the defined threshold level or window
6	**Irq_Timer_WakeUp**	The count-down of the wake-up is over
5	**Irq_DMA_ready**	The DMA transaction has been completed
4	**Irq_EEPROM_Full**	The internal or external non-volatile memory if full
3	(unused)	
2	**Transaction_Error_Flag**	One of the previously executed commands has failed (delay not fulfilled, denied access, data not processed …). This bit is automatically cleared after power-on or after read of the *RFID interrupt & status word*.
1	**Last_Transaction_Status**	This bit indicates whether the last request has been processed ('0') or not ('1'). In this latter case, the MLX90129 ignores any new request.
0	**Core_Main_Status**	The system is busy with an internal operation and the request from RFID cannot be processed.

7.5 Serial Peripheral Interface (SPI)

7.5.1 SPI : modes of operation

The SPI implemented in the MLX90129 works in Slave or Master mode.

- When the MLX90129 SPI is configured in the Slave mode, the SPI master (being a microcontroller, a Zigbee End Device, …) controls the *serial clock* signal SCK, the *Slave Select* signal SS and transmits the data to the slave via the *Master-Out-Slave-In* signal MOSI. As a slave, the MLX90129 answers with the *Master-In-Slave-Out* signal MISO, synchronized on SCK.
- When configured in the Master mode, the MLX90129 SPI can select an external slave, typically an external serial EEPROM, and use it for data logging. The command op-codes and delays between request and response are programmed in the SPI configuration register. The master SPI controls the *Slave Select*, the *Serial Clock* signal, sends the data on MOSI and read data on MISO. It is possible to control the SPI as master thanks to custom RFID commands.

SPI is compliant with the following control options:

- Master mode and Slave mode
- CPOL=0: The clock is active-high: in the idle mode, SCK is low.
- CPHA=0: Sampling of data occurs on rising edges of SCK. Toggling of data occurs on falling edges.
- MSB first (on MISO and MOSI)
- Baud-rate: 1MHz

Detailed signal description:

- **MOSI :** this pin is used to transmit data out of the SPI module when it is configured as a Master and receive data when it is configured as a Slave.
- **MISO :** this pin is used to transmit data out of the SPI module when it is configured as a Slave and receive data when it is configured as a Master.
- **SS :** when the MLX90129 is configured as a SPI master, it controls the SS pin to select an external peripheral with which a data transfer will take place. When configured as a Slave, it is used as an input to receive the *Slave Select* signal.
- **SCK :** this pin is used to output or receive the clock.
- **IRQ** : this pin is used to interrupt the SPI master (microcontroller) process.

When the MLX90129 is not selected by the SPI master or when the received command code is not supported, the pin MISO is in tri-state. When the MLX90129 uses the SPI in the master mode (to access an external memory), it complies with the same rules for any external SPI masters.

7.5.2 Slave SPI command set

SPI command set

Command	Code	Operation
EEP_RD	0000 1111	Read the addressed EEPROM word
EEP_WR	0000 1110	Write the addressed EEPROM word
REG_RD	0000 1101	Read the addressed register in the *Register File*
REG_WR	0000 1001	Write the addressed register in the *Register File*
DEV_RD	0001 0000	Read a word from the selected *internal device* (Control, status, ADC,…)
DEV_WR	0001 1000	Write a word into the selected *internal device* (Control, ee-Latches)
REG_UPDT	0001 1100	Fills the *Register File* with its image stored in the EEPROM (without reboot)

7.5.3 Internal devices dedicated to SPI communication

The SPI and the RFID interfaces share the access to the memory. In order to prevent any access conflicts, and to manage the communications via SPI and RFID, two registers have been defined in the *Device Address Domain*: the *SPI Core control word* and the *SPI interrupt/status word.* They are always immediately accessible for read or write operations, even if the system is busy.

The SPI I/O signals are accompanied of an output interrupt signal IRQ. This signal may be used to wake up or to warn the SPI master (micro-controller) about some access conflicts or some general problems (low battery level, sensor fault, external event …). It is set once one of the selected events occur. It is reset once the SPI master has read the *SPI Core interrupt / status word*, or has set the bit *Disable IRQ setting* of the *SPI Core control word.*

SPI Core control word (*Device address domain*, address **#00**, read/write)

Bits	Name	Description (if bit=1)
15:7	-	Reserved (must be 0)
6:4		*RFID interrupts control*:
6	**Irq_Rfid_Field_En**	*Enable RFID Interrupt 2* (Access to Register file).
5	**Irq_Rfid_EEp_Access_En**	*Enable RFID Interrupt 1* (Access to EEPROM).
4	**Irq_Rfid_ Reg_Access_En**	*Enable RFID Interrupt 0* (RFID field is detected).
3	**Irq_Last_Trans_En**	*End of transaction* Enable interrupt indicating the completion of the last requested transaction. To de-assert this interrupt, the user will request another transaction, read the SPI local data buffer (in device address domain), disable this interrupt or block IRQ assertion.
2	**Irq_Dis**	*Disabled IRQ setting.* Disable the setting of the IRQ signal.
1	**Core_Sts_Irq_En**	*Core status interrupt enabled.* Enable the interrupt on IRQ telling that the system is free.
0	**Core_Lock**	*Core lock.* Lock any transactions between the different internal devices and the non-SPI interfaces. This allows having an access from SPI to any registers at any time. The last pending transaction is always completed.

SPI interrupt & status word (*Devices address domain*, address **#01**, read only)

Bits	Name	Description (if bit=1)
15	(reserved)	
14	**Irq_LowBattery**	Low battery voltage detected
13	**Irq_SensorFault**	Sensor failure detected (broken or short-cut)
12	**Irq_ExternalEvent**	An external event has been detected (rising edge on pin NC)
11	(reserved)	
10	**Irq_Rfid_Reg_Access**	The RFID interface is accessing the Register File
9	**Irq_Rfid_EEp_Access**	The RFID interface is accessing the EEPROM
8	**Irq_Rfid_Field**	The magnetic field is high enough to start a RFID communication
7	**Irq_Sensor_Threshold**	The output data from the sensor has crossed the defined threshold level or window
6	**Irq_Timer_WakeUp**	The count-down of the wake-up is over
5	**Irq_Dma_Ready**	The DMA transaction has been completed (in the non-loop mode)
4	**Irq_Memory_Full**	The internal or external non-volatile memory is full
3	**Irq_Write_Failure**	The non-volatile block has been badly or weakly written: the data is wrong or its long-term retention is not guaranteed
2	**Transaction_Error**	One of the previously executed commands has failed (read delay, denied access, data not processed,…). This bit is automatically cleared after reboot or after read of the *SPI interrupt & status word*.
1	**Last_Transaction_Status**	This bit indicates whether the last request from SPI has been processed ('0') or not ('1'). In this latter case, the MLX90129 ignores any new request from SPI.
0	**Core_Main_Status**	The system is busy with an internal operation and the request from SPI cannot be processed immediately.

In the application cases where a microcontroller, a RFID base-station or the DMA may access the memories or the internal devices at the same time, it could be useful to check the state of the bit *Core main status*. If the system is busy for a too long time, it is possible to stop the on-going process with the following sequence:

1. Set the bit *Core lock* in the *SPI Core control word*.
2. Set the bit *Core interrupt enable* (to get an interrupt after the completion of the last on-going transaction).
3. Wait for an interrupt on IRQ.
4. Reset the bit *Core interrupt enable*.
5. Do all necessary actions.
6. Reset the bit *Core lock* in the *SPI Core control word*.

In application where the SPI is used for several subsequent commands, it could be useful to check the *Last transaction status* to be sure that the system is ready before a new transaction.

7.5.4 Interrupts

The following table summaries the information about the interrupts. For each bit of the *SPI interrupt & status word*, the condition to assert high or low the status flag, and to assert high the interrupt request on IRQ, are described. All interrupts can be disabled in asserting high the bit *Irq_Dis* of the *SPI Core control word*.

Bit	Interrupt name	Status flag assertion HIGH : conditions	Status flag assertion LOW : conditions	IRQ enable conditions
0	Core_Main_ Status	The Core is not busy with transactions between different internal devices	The Core is busy with a transaction between different internal devices.	Core_Sts_Irq_En =1
1	Last_ Transaction_ Status	The last requested transaction with the Core has been completed. E.g. ADC is ready	A request for a new transaction is pending	Irq_Last_Trans_ En =1
2	Transaction_ Error	When one of previously requested commands was not executed	The user reads the *SPI interrupt & status word*	(Never)
3	Irq_Write_ Failure	When one of the previously requested write-operations to a non-volatile memory has failed	The user reads the *SPI interrupt & status word*	Always
4	Irq_Memory_ Full	Conditions to be fulfilled: - the DMA is busy - *loop enable* and *IRQ enable* bits are set in *DMA control* - the allocated memory is full	The user halts the DMA processing or disables the *IRQ enable* bit in *DMA control word*	Always
5	Irq_Dma_ Ready	The DMA unit has completed the last requested transaction	The user reads the *SPI interrupt & status word*	Dma_IrqDataReady_En =1 in the *DMA configuration register*
6	Irq_Timer_ WakeUp	The timer has completed its counting phase	The timer is requested to start a new counting phase (during the *automatic logging mode*)	WUT_Irq_En =1 in the *Power management configuration word.*
7	Irq_Sensor_ Threshold	The last ADC output code crosses the defined threshold level or window	The chip is requested to read a new value of the sensor	Sensor_Irq_En =1 in the *Sensor control word*
8	Irq_Rfid_ Field	A RFID field has been detected, and is strong enough to start a RFID communication	The RFID field has been removed, or is too low for a RFID communication	Irq_Rfid_Field =1 in the *SPI Core control word*
9	Irq_Rfid_EEp _Access	A RFID reader is accessing the EEPROM	The user reads the *SPI interrupt & status word*	Irq_Rfid_EEp_Access=1 in the *SPI Core control word*
10	Irq_Rfid_ Reg_ Access	A RFID reader is accessing the register file	The user reads the *SPI interrupt & status word*	Irq_Rfid_ Reg_ Access =1 in the *SPI Core control word*
12	Irq_External Event	An event occurs and the event detector is enabled, using the appropriate ee-Latch	The event detector is disabled in the appropriate ee-Latch	Always
13	Irq_Sensor Fault	A failure has been detected on the currently selected external sensor	A new sensor (without failure) is selected or the failure disappears	Sensor_Irq_En=1 in *Sensor control word*
14	Irq_ LowBattery	The battery voltage level is too low (close to the power-on reset level)	After charging or replacement of the battery	LowBattery_Irq_ En=1

7.5.5 Master SPI configuration

A bit of the *Device security map* is used to set the SPI as master. Then, the MLX90129 controls the clock SCK, the slave-select SS (output), and the communication I/O MOSI (output) and MOSI (input).
The SPI configuration words are used to setup the parameters of the SPI-master interface, in order to access an external memory (a serial SPI EEPROM). In master mode, the SPI may be used by the internal DMA unit (Direct Memory Access) to store the output data of the sensor. The stored data may be read back by a RFID base-station.

Address provided to 90129	Adress of eeprom "even byte"	Adress of eeprom "odd byte"
#00	#00	#01
#01	#02	#03
#02	#04	#05
#n/2	#n	#n+1

Storing a 16-bit word {MS-Byte; LS-Byte} in the external EEPROM:
The RFID reader sends a command to the MLX90129, containing an address #n/2 (in red). Then MLX90129 will send a sequence of commands to the external EEPROM. This sequence is composed of:
_ Optionally a Write Enable command
_ The address #n/2 of the first byte to write (LSByte)
_ The LS-Byte
_ The MS-Byte
Thus, the LS-Byte will be written in the EEPROM address #n, and the MS-Byte in the EEPROM address #(n+1).
The Master-SPI configuration register must be filled to register #0D to handle the specific protocol of the external EEPROM.

Master SPI configuration words (EEPROM & Register, **#0D**, **#0E**, R/W)

Bits	Name	Description
		*External memory control word (**#0D**)*
15:8	**SPI_WriteEn_Code**	***Write enabled command code***. Command op-code of the “write enable” operation, used toward an external EEPROM.
7	**SPI_BurstMode_En**	***Burst mode enable***: enable the write burst mode used in some SPI serial EEPROM. (*)
6:4	**SPI_WriteDelay**	***Write delay***. Delay which is inserted between a write command and another subsequent command. Precision is 4 ms. Minimal write delay calculation equation, when value of this field is non-zero: t_{WC} = 4 x WriteDelay - 1 (ms).
3:2	**SPI_WriteEn_Ctrl**	***Write enable operation control.*** Defines when the *Write Enable* command must be applied: 00 - never 01 - before first write only 10 - before every write operation 11 - reserved
1:0	**SPI_AddressMode**	***Addressing mode***. Defines the address length to be passed via SPI for a proper EEPROM addressing. 00 - 8-bit address is used 01 - 16-bit address is used 10 - 24-bit address is used (8 MSB are filled with zeroes) 11 - reserved
		*External memory command codes word (**#0E**)*
15:8	**SPI_WriteCode**	***Write command code***. Command op-code used by MLX90129 to write in an external memory block
7:0	**SPI_ReadCode**	***Read command code***. Command op-code used by MLX90129 to read from an external memory block

(*) Note:
The setting of the bit *Burst mode enable* switches all subsequent transactions with an external memory into burst mode. It means, that only the first memory access transaction requires to send a command and an address. After completion of this first transaction, the master SPI of the MLX90129 does not set the SS signal to ‘1’. When a new block has to be read / written, the SPI master skips the command and address phases and immediately sends or receives data to or from the external memory (it allows a page access).

7.6 Direct Memory Access (DMA)

7.6.1 Main features

The DMA (Direct Memory Access) unit controls the standalone applications, without any external microcontroller. It handles the start-up operations, and sends the data from a programmed source towards a programmed destination, using flexible protocol and interrupt conditions. Typically, it may get the data from the sensor interface and store it in an EEPROM. It works on defined time periods controlled by a wake-up timer.

Its main features are the following:

- The configuration registers are filled from the EEPROM at the start-up (when enabled)
- The duty-cycle (ratio between active and sleep mode) is controlled by a wake-up timer (WUT) that wakes the system up after a programmed delay
- Programmed behaviour (source, destination, interrupt options, master-SPI options, …)
- Programmable command-set to address any kind of external SPI memory
- Programmable timings used in the SPI protocol of the external memory (between the request and the response)
- Calculation of the address of the destination (incrementing the programmable Address #0).

7.6.2 DMA operations

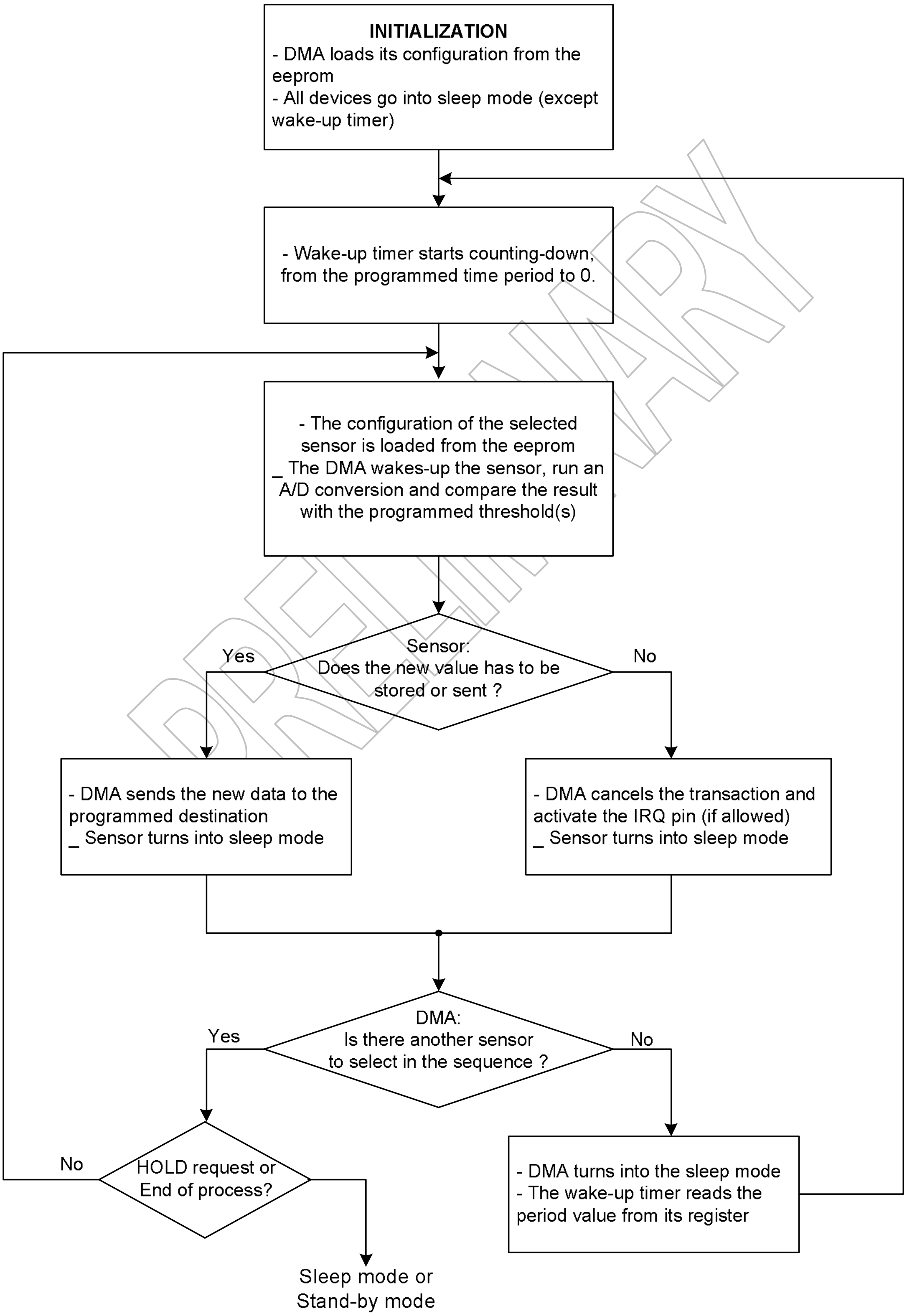
Loading of the register file from the EEPROM data.

_ At the power-up of the battery, the DMA automatically loads the *Register File* with its image from the EEPROM. A bit stored in the EE-Latch bank, called *Disable Automatic Loading*, can be set to disable this automatic loading.
_ The power-on reset from the RFID field does not lead to the loading of the entire *Register File*: only the *UID* is loaded in order to enable a RFID anti-collision procedure.
_ At any time, the RFID or the SPI interface can send an *Update* command to update the content of the *Register File* with the values stored in the EEPROM.
_ The configuration may be chosen is such a way that DMA operations starts automatically at power-up.

Data logging in the internal or external EEPROM

_ After power-up, the DMA loads the *Register File* with the data stored in the EEPROM (it also loads its own configuration).
_ The wake-up timer (WUT) starts counting to a programmed value. During this counting, the MLX90129 works in a *sleep mode*, consuming a very low power. To save power, the duty cycle should be as low as possible.
_ At the end of the counting, the WUT wakes the DMA up.
_ The DMA loads the configuration registers of the selected sensor, and starts a sensor acquisition.
_ The result data is then stored in the EEPROM, at an address calculated from a programmed value.
_ Depending on the options, the DMA may configure and start an acquisition of another sensor, or may let the system enter the *sleep mode*. If another sensor is selected, then the DMA loads the new sensor configuration before starting the acquisition.

At any moment, this process may be interrupted by an external microcontroller, to read the data collection. For that, it asserts low the bit *Processing Control* of the *DMA configuration register.* Then, the process may be hold or reset. In order to store only the latest data from ADC, the bit *Loop enable* must be set. In this case, the old data is rewritten by the DMA unit with the new one when the memory border has been reached. When the memory is completely filled, a *Full Memory* interrupt appears on the pad IRQ. It is also possible to send an interrupt request (IRQ) to the external microcontroller after each Wake-up timer period. Then, the microcontroller may decide to read the sensor output data and process it.


INITIALIZATION
- DMA loads its configuration from the eeprom
- All devices go into sleep mode (except wake-up timer)
- Wake-up timer starts counting-down, from the programmed time period to 0.
- The configuration of the selected sensor is loaded from the eeprom
_ The DMA wakes-up the sensor, run an A/D conversion and compare the result with the programmed threshold(s)
Yes
Sensor:
Does the new value has to be stored or sent ?
No
- DMA sends the new data to the programmed destination
_ Sensor turns into sleep mode
- DMA cancels the transaction and activate the IRQ pin (if allowed)
_ Sensor turns into sleep mode
Yes
DMA:
Is there another sensor to select in the sequence ?
No
No
HOLD request or End of process?
- DMA turns into the sleep mode
- The wake-up timer reads the period value from its register
Sleep mode or Stand-by mode

Interrupt of DMA process

The microcontroller or the RFID base-station can read the *DMA status register* and access the *DMA configuration register* to start and control the DMA processing. At any time, they can hold the DMA process and check the current status of the copied data (telling how many words have been copied). Then, they can change the DMA configuration to a new one or continue the processing. While the DMA is processing data or is on hold, any change of the parameters in the DMA configuration words does not cause the expected changes in the behaviour.

End of DMA process

At the end of the sequence, the MLX90129 may enter its sleep mode or its stand-by mode. During the *Sleep mode*, the system may be interrupted by a RFID field, or by a SPI "SS=0" event.

7.6.3

7.6.4 Setup of the Automatic Logging Mode

Setup

In order to enable the *automatic logging mode*, the following sequence must be run:
_ Setup the *DMA configuration word*
_ Setup the *DMA source start address*, *DMA destination start address* and the *DMA length*.
_ If an external EEPROM is used, setup the *SPI-master configuration word* and the *SPI-master command word*.
_ If only one sensor is used, setup the sensor interface configuration directly in the register file.
If several sensors are used, setup the sensor interface configurations also in the EEPROM.
_ Setup the Sensor control word and the Sensor thresholds words (if required)
_ Setup the Wake-up Timer configuration word
_ Setup the logging period in the wake-up timer
_ To enable the DMA operation, the bit *Processing Control* of the *DMA configuration register* must be reset.
_ Set the bit *Automatic Logging enable* in the wake-up timer configuration to '1'.

All these actions can be performed automatically after the system boot: the required configuration can be set in Register File image in the EEPROM. Then, after power-on, the system reads this configuration and performs the programmed actions.

Logging several sensors and time-stamp

When more than one sensor is selected as a source of automatic logging, the DMA stores subsequently all the sensor output data in the selected memory. The stored data has a prefix to identify them:

Bit	15:14	13:0
Definition	Prefix	ADC output code

The prefix code is defined in the following table:

Prefix code	Related sensor or parameter
00	Sensor 0
01	Sensor 1
10	Sensor 2
11	Iteration index (Time stamp)

It is not mandatory to store all the data from a sensor at each iteration, but only the data fitting the conditions defined in the bits *Data logging control* of the register word called *Sensor[x] Controller configuration space*.

7.6.5 _DMA registers map

DMA status register (Device Address Domain, **#05**, read only)

Bits	Name	Description
15:0	**DMA_Current_Destination _Address**	Address of the block of memory in the destination address domain (which is still not filled with data from the source device).

DMA configuration word (EEPROM & Register, address #09 to #0C, read/write)

Bits	Name	Description (when bit = '1')
*DMA Control word (**#09**)*		
15:12 15 14 13 12	 **DMA_Time_Incl** **DMA_Sensor2_Incl** **DMA_Sensor1_Incl** **DMA_Sensor0_Incl**	*Sensing sequence* include the iteration index (time stamp) in the memory include the measurement and the storing of sensor 2 include the measurement and the storing of sensor 1 include the measurement and the storing of sensor 0
10:11		Reserved (must be 00)
9	**DMA_LastWordMask**	Disable the copying of the LSB (byte) of the current word in the external memory
8	**DMA_FirstWordMask**	Disable the copying of the MSB (byte) of the current word in the external memory
7:6	**DMA_DestinationCode**	*Destination of the data transfer* 00 : register file 01 : internal EEPROM 10 : SPI as master (external EEPROM) 11 : (reserved)
5:4	**DMA_SourceCode**	*Source of the data transfer* 00 : (reserved) 01 : internal EEPROM 10 : (reserved) 11 : Sensor interface
3	**DMA_LoopEn**	Enable an eternal loop of data logging. In this case, after having copied *Length* words, the DMA unit does not stop its operation but sets its address to the initial one and goes on copying data.
2	**DMA_IrqDataReady_En**	*IRQ Data-transfer enabled.* The IRQ signal is set when the data transfer has been completed.
1	**DMA_Hold**	*Hold.* The DMA holds its operation till it this bit goes low. The current ongoing DMA transaction is always completed.
0	**DMA_Processing_Control**	*Processing control.* '0': Enables the Timer to start and sequence the DMA operations. '1': Run directly the DMA operations, without timing.
*DMA: Source start address (**#0A**)*		
15:0	**DMA_Source_Address**	Address of the first word to be copied from the source device.
*DMA: Destination start address (**#0B**)*		
15:0	**DMA_Destination_Address**	Address of the first word to be filled into the destination device.
*DMA: Length (**#0C**)*		
15:0	**DMA_Data_Length**	Length of the block to be copied (in words).

7.6.6 Wake-up timer / Power management

The Wake-up timer is used for two purposes:

- to wake-up the microcontroller after a defined delay via the IRQ pin
- to enable and sequence the periodical logging of data from the sensor
- to enter the stand-by mode after a programmed delay

The following table contains the control options of this timer:

Wake-up timer (WUT) / Power management configuration words
(EEPROM & register, addresses #0F to #10)

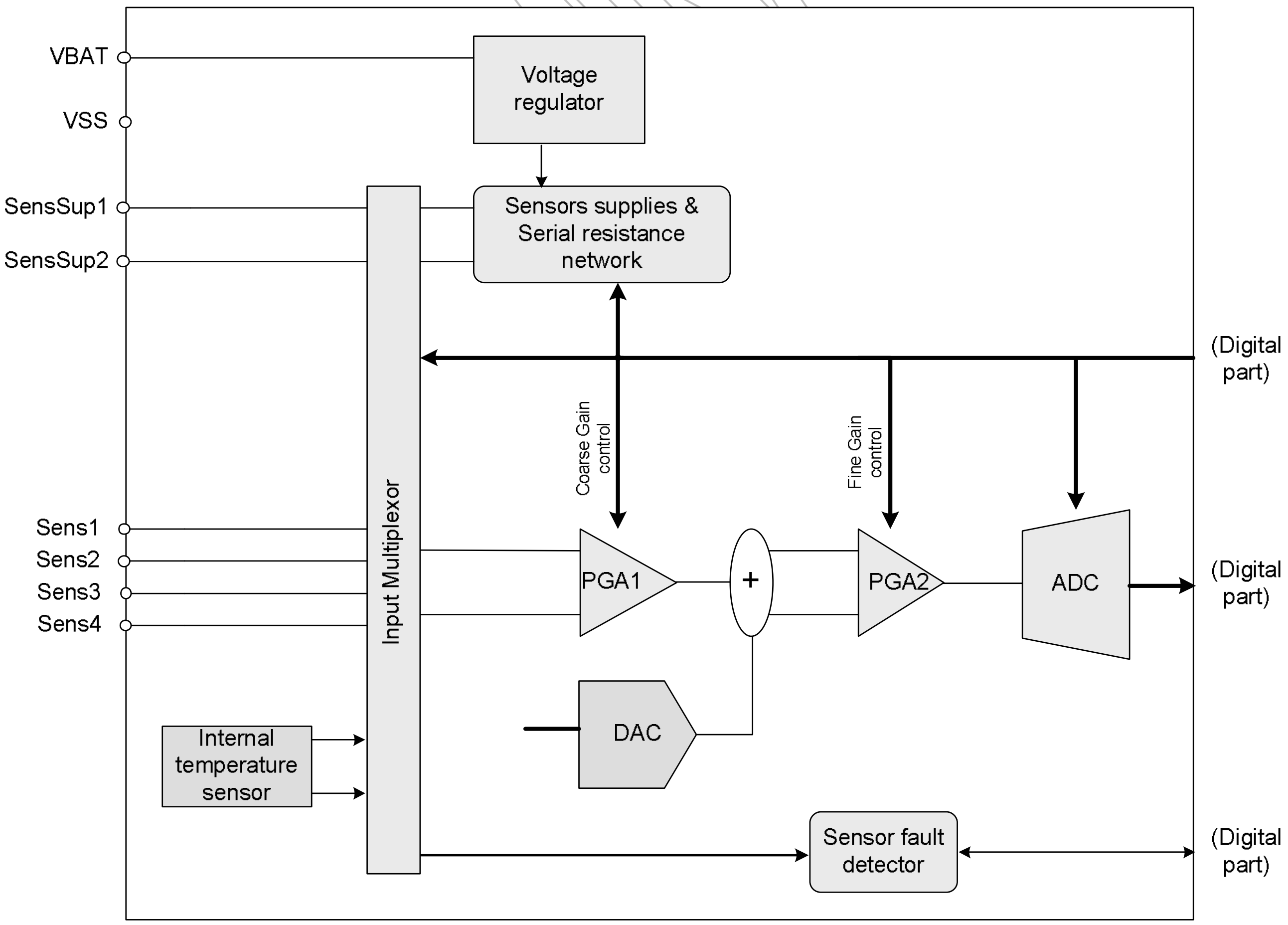
Bits	Name	Description (when =1)
		*Control word (**#10**).*
15:6	-	Reserved (must be 0)
5:4	**WUT_Precision**	***Precision***. Defines the time unit for the specified timer wake-up period (called *Count-down period*). The accuracy is ±0.5 ms. 00: time in ms 01: time in s 10: time in min 11: time in hours
3	**WUT_AutoStandby_En**	***Automatic stand-by enabled.*** Allow the MLX90129 to automatically enter the stand-by mode after the end of the wake-up timer count-down, or after completion of the automatic logging (if it is enabled).
2	**WUT_AutoLog_En**	***Automatic logging mode enabled.*** If this bit is set to '1', the wake-up timer loads its value from the Register file and starts a count-down. As soon as it reaches 00h, it allows to run one or several sensor acquisitions and to store the data in the programmed destination. Then, it loads its count-down period again and starts counting. This process may be halted by resetting this bit to '0'.
1	**LowBattery_Irq_En**	***Low-battery interrupt enabled.*** Enable interrupts from Low-battery detector.
0	**WUT_Irq_En**	***Timer IRQ enabled***. The timer starts its operation and generates IRQ signal after passing specified period.
15:0	**WUT_CountDownPeriod**	***Count-down period (#0F)***

7.7 Sensor Signal Conditioner

7.7.1 Block diagram

The sensor signal conditioner amplifies and filters the sensor output signal, before converting it to a digital format.
These are its main features:

- Two programmable gain amplifiers (PGA1 and PGA2)
- Programmable offset level (DAC)
- 16-bit A/D converter
- Internal temperature sensor
- Two selectable external differential or single-ended sensors
- Voltage regulator, to supply internal and external devices
- Sensor fault detector
- Programmable serial resistor connected to the external sensors



7.7.2 Blocks description

Input multiplexor
This block allows selecting the sensor signal which will be connected to the first amplifier of the signal conditioner. It is possible to select the external sensor(s) connected to SENS1, SENS2, SENS3 and SENS4, or the internal temperature sensor.

Programmable amplifier 1 (PGA1)
This block is the first programmable amplifier of the analog chain. It has a wide range of gain and is fully differential. It is compliant with a wide range of input common-mode voltage.
PGA1_Out2 – PGA1_Out1 = Gain1 * (PGA1_InP – PGA1_Inn)

D/A converter (DAC)
This block is used to compensate the offset of the sensor and of PGA1, amplified by PGA1. It is also used to choose the value of the physical sensed value, for which the ADC will give its middle code.

Programmable amplifier 2 (PGA2)
This block amplifies (with a programmable gain) the output voltages of PGA1 and of the DAC, following the equation:
PGA2_Out2 – PGA2_Out1 = Gain2 * [(PGA1_Out2 – PGA1_Out1) – DAC_Out]

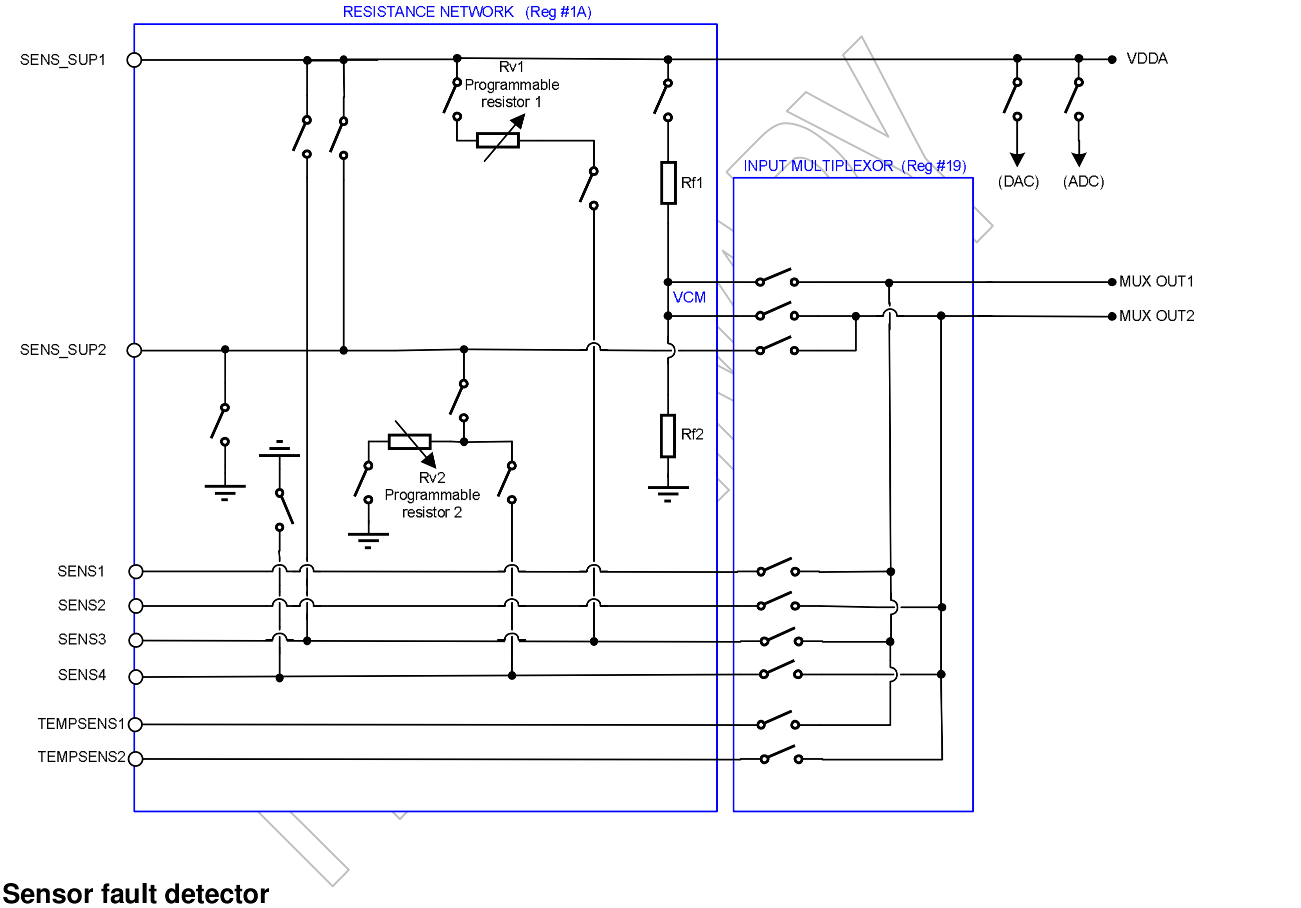
A/D converter (ADC)
This block converts into a digital format the output voltage of PGA2.

Voltage regulator
This block provides the signal conditioner chain and the external sensors with a programmable, stable voltage for a wide range of sourced currents.

Internal temperature sensor
This block gives a temperature-dependent voltage. As all other sensors, it must be calibrated to give accurate data.

Sensor supplies & Resistor network

Many combinations of resistors connections with the external sensors are possible. All the switches figured on the following schematic are independently programmable via register #1A. The supply VDDA is the stabilized output of the voltage regulator. The configuration register #19 is used to connect an external sensor or internal resistance to the inputs of the analog chain (called MUX OUT1 and MUX OUT2).

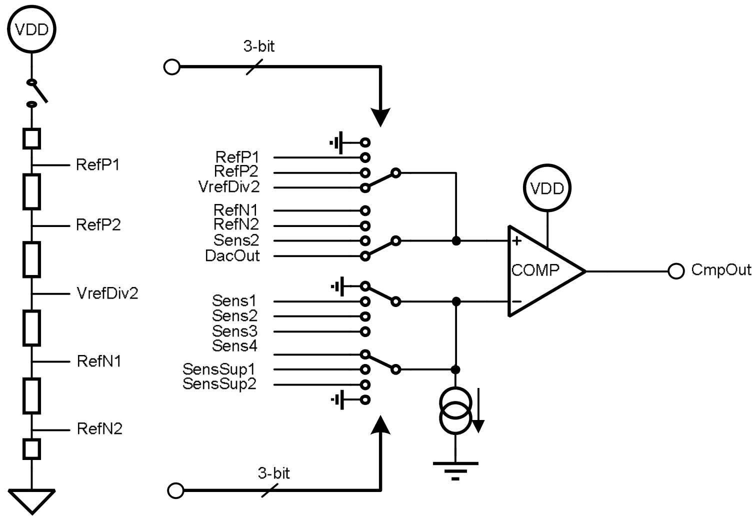


Sensor fault detector

A detector may be used to detect a failure in the external sensor. The sensor supply and outputs may be broken or short-cut.

All the potential failures can be tested by selecting the sensor terminal and comparing it with the appropriate voltage reference. This can be done by programming the configuration register #14 of the *Analog Configuration Space*. The comparison result is stored in the *RFID/SPI Core interrupt/status word*.

If it is enabled, the detection of a failure causes an interrupt on IRQ. The nature of the failure may be deduced from the configuration bits that were used when it has been detected.



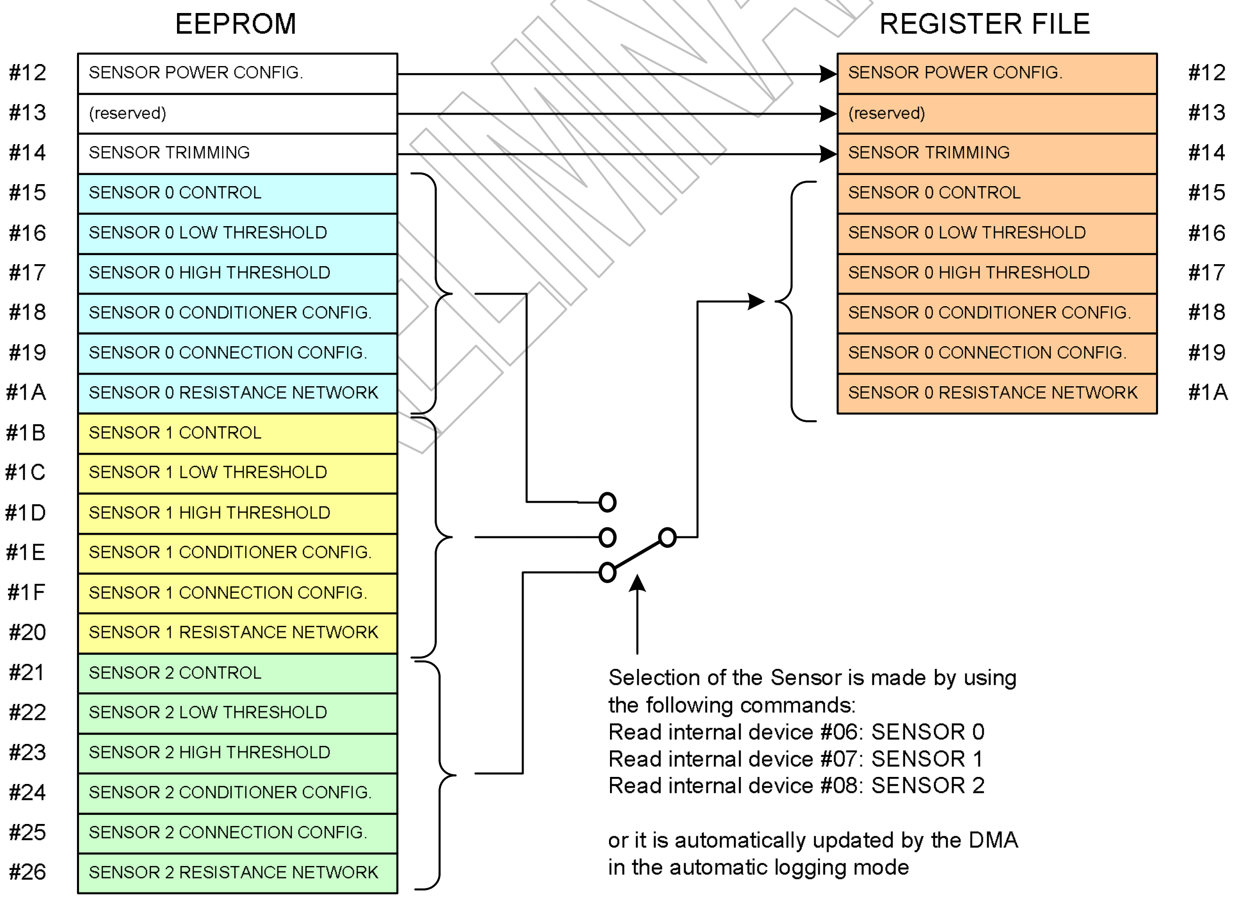
7.7.3 Sensor Digital Controller

Functions

- Initialization of the sensor interface, and running of the A/D conversions
- Buffer the ADC output code (in one of the 3 ADC buffers) when conversion has been completed
- Digital data processing: mean calculation, comparison with thresholds values
- Take the decision to store the data, and/or configure the conditions to generate an interrupt on IRQ.

Initialization

Before any A/D conversion, the configuration of the sensors must be stored in the register file at addresses from #12 to #1A. Each sensor has its configuration stored in EEPROM. Depending on the selected sensor, the appropriate data will be copied from EEPROM to the register file.


EEPROM
REGISTER FILE
#12 SENSOR POWER CONFIG.
#13 (reserved)
#14 SENSOR TRIMMING
#15 SENSOR 0 CONTROL
#16 SENSOR 0 LOW THRESHOLD
#17 SENSOR 0 HIGH THRESHOLD
#18 SENSOR 0 CONDITIONER CONFIG.
#19 SENSOR 0 CONNECTION CONFIG.
#1A SENSOR 0 RESISTANCE NETWORK
#1B SENSOR 1 CONTROL
#1C SENSOR 1 LOW THRESHOLD
#1D SENSOR 1 HIGH THRESHOLD
#1E SENSOR 1 CONDITIONER CONFIG.
#1F SENSOR 1 CONNECTION CONFIG.
#20 SENSOR 1 RESISTANCE NETWORK
#21 SENSOR 2 CONTROL
#22 SENSOR 2 LOW THRESHOLD
#23 SENSOR 2 HIGH THRESHOLD
#24 SENSOR 2 CONDITIONER CONFIG.
#25 SENSOR 2 CONNECTION CONFIG.
#26 SENSOR 2 RESISTANCE NETWORK
SENSOR POWER CONFIG. #12
(reserved) #13
SENSOR TRIMMING #14
SENSOR 0 CONTROL #15
SENSOR 0 LOW THRESHOLD #16
SENSOR 0 HIGH THRESHOLD #17
SENSOR 0 CONDITIONER CONFIG. #18
SENSOR 0 CONNECTION CONFIG. #19
SENSOR 0 RESISTANCE NETWORK #1A

Selection of the Sensor is made by using the following commands:
Read internal device #06: SENSOR 0
Read internal device #07: SENSOR 1
Read internal device #08: SENSOR 2

or it is automatically updated by the DMA in the automatic logging mode

The configuration of the selected sensor is automatically loaded from EEPROM when:

- Using commands Read Internal Device #07, Read Internal Device #08, for the first time.
- Using a command Read Internal Device #?? different from the previous one.

The configuration of the selected sensor is **not** automatically loaded from EEPROM when:

- Using command Read Internal Device #06, for the first time.
- Using the same command Read Internal Device as the previous one.

ADC & Sensor interface configuration

Sensor control word in the *Sensor Controller Configuration Space* (EEPROM, addresses **#15**, #1B, #21)

Bits	Name	Description (when =1)
15:14	**ADC_Mode**	***ADC mode*** 00: higher speed, but lower accuracy 01, 10: intermediate modes 11: lower speed, but higher accuracy
13:12	**Sensor_InitTime**	***Sensor initialization time*** 00: 150µs (= default initialization time for the internal sensor) 01: 1ms 10: 16ms 11: 128ms
11	**Sensor_Irq_En**	***Fault interrupt enabled***. Enable the interrupt from *sensor fault detector*
		Interrupt conditions control
10	**Sensor_Irq_Above**	- generate an interrupt when the last sample is above the programmed high threshold
9	**Sensor_Irq_Betwn**	- generate an interrupt when the last sample is between the programmed high and low thresholds
8	**Sensor_Irq_Below**	- generate an interrupt when the last calculated sample is below the programmed low threshold
7	**ADC_LowPower**	***Low power mode***. Enable the low power mode of the ADC.
		Data logging control
6	**ADC_DataLogAbove**	- store the calculated samples above the high threshold
5	**ADC_DataLogBetwn**	- store the calculated samples between the high and low thresholds
4	**ADC_DataLogBelow**	- store the calculated samples below the low threshold
3:2		Reserved (00)
1:0	**ADC_Proc_Ctrl**	***Samples processing control*** Defines the rules for the calculation of the value which will be stored in the *ADC buffer* 00 - single sample 01 - average of 2 samples 10 - average of 8 samples 11 - average of 32 samples

Sensor low threshold in the *Sensor Controller Configuration Space* (EEPROM, addresses **#16**, #1C, #22)

Bits	Name	Description (when =1)
15:0	**Sensor_ThresLow**	Sensor [x] low threshold word

Sensor high threshold in the *Sensor Controller Configuration Space* (EEPROM, addresses **#17**, #1D, #23)

Bits	Name	Description (when =1)
15:0	**Sensor_ThresHigh**	Sensor [x] high threshold word

ADC buffer (Internal Device Domain, **#06 to #08**, R/W)

Bits	Name	Description
15:0	**ADC buffer**	Output data of the ADC, after A/D conversion of the selected sensor

7.7.4 Sensor operation

In order to read the output data of a sensor, the SPI master or the RFID base-station has to access one of the 3 words *ADC buffer* in the *Device address domain*. Accessing this buffer makes sensor configuration, the A/D conversion and the data processing to start. To make sure that all operations are done, it is enough to:

- wait for a specified period of time and read the *internal device* #02 (local buffer).
- periodically monitor the *SPI/RFID Core status word* and check the bit: *Sensor interrupt: Data ready*.

Using RFID, it is usually needed to read *internal device* #02 to access the ADC data.

7.7.5 Map of the Analog Side Configuration Space

Some registers words may be filled depending on the sensor selection. The table below presents the configuration words stored in the *Analog Side Configuration Space* of the EEPROM. Although the power management of the sensor block is automatically managed by the digital side, it may be useful to disable some unused cells to safe power.

EEPROM #12: Sensor power configuration word

#	Bits	Name	Content	Value
			Sensor power configuration word	
12	0	**Sensor_Pga1_En**	PGA1 enable bit	0: not powered (disabled) 1: powered (enabled)
	1	**Sensor_Pga2_En**	PGA2 enable bit	
	2	**Sensor_Dac_En**	DAC enable bit	
	3	**Sensor_Adc_En**	ADC enable bit	
	4	**Sensor_Reg_En**	Voltage Regulator enable bit	
	5	**Sensor_DacBuf_En**	DAC buffer enable bit	
	6	**Sensor_Bias_En**	Bias block enable bit	
	7	**Sensor_Temp_En**	Temperature sensor enable bit	
	8	**Sensor_Sfd_En**	Sensor fault detector enable bit	
	9	**Sensor_Ats_Pwr_En**	Event detector power-on bit	
	10	(not used, must be 0)		
	11	**Sensor_Ats_En**	Event detector enable bit	
	12	**Sensor_BatMon_En**	Battery monitor enable bit	
	13	**ExtSupplyMode**	0: the regulator always supplies the external device 1: the regulator supplies it only in its watchful state (to save power)	
	14	(not used, must be 0)		
	15	(not used, must be 0)		

EEPROM #13

#	Bits	Name	Content	Value
13	15:0	Reserved	Must be 0x00	0000h

EEPROM #14: Serial resistor trimming and sensor-fault configuration word

This EEPROM-word is used to trim the value of the programmable serial resistance connected to the sensor. It is also used to program the connection between the external sensor and the sensor fault detector.

#	Bits	Name	Content	Value
Sensor trimming and fault-detector configuration word (Common for all sensors)				

14	5:0	**Sensor_Res_Trim**	Trimming of the sensor serial resistor	Bit[0]=1 → add 0.5kΩ to the serial resistance
				Bit[1]=1 → add 2kΩ
				Bit[2]=1 → add 4kΩ
				Bit[3]=1 → add 8kΩ
				Bit[4]=1 → add 16kΩ
				Bit[5]=1 → add 32kΩ

	9:6	Melexis calibration: do not change this value		
	15:10	**Sensor_Fault_Cfg**	Sensor fault detector: selection bits	Comparator input "+" is connected to: Bit[15:13]=000: VSS Bit[15:13]=001: 0.95*VDD Bit[15:13]=010: 0.75*VDD Bit[15:13]=011: 0.5*VDD Bit[15:13]=100: 0.25*VDD Bit[15:13]=101: 0.05*VDD Bit[15:13]=110: SENS2 Bit[15:13]=]=111: DAC output Comparator input "-" is connected to: Bit[12:10]=000: VSS Bit[12:10]=001: SENS1 Bit[12:10]=010: SENS2 Bit[12:10]=011: SENS3 Bit[12:10]=100: SENS4 Bit[12:10]=101: SENSSUP1 Bit[12:10]=110: SENSSUP2 Bit[12:10]=111: VSS

EEPROM #18, #1E, and #24 : Sensor Conditioner configuration word

The MLX90129 can handle 2 different external sensors and 1 internal sensor. Each of these sensor output signals can be conditioned in a different way, using different values of gains and DC levels (offset).

#	Bits	Name	Content	Value
Sensor 0: Signal Conditioner configuration word				
18	7:0	**Sensor0_DacCode**	Offset (or level shifter): DAC code, for Sensor1	00000000: 0 01111111: Vref/2 10000000: 0 11111111: -Vref/2
	11:8	**Sensor0_Pga1Gain**	Gain of PGA1	0000: Gain=8 1111: Gain=74
	14:12	**Sensor0_Pga2Gain**	Gain of PGA2	000: Gain=1 111: Gain=8
	15	**Sensor0_Chopper_En**	Chopper enable	1: enabled
Sensor 1: Signal Conditioner configuration word				
1E	15:0	Same as above	Same as above	
Sensor 2: Signal Conditioner configuration word				
24	15:0	Same as above	Same as above	

EEPROM #19, #1F, and #25 : Sensor Connections configuration word

The first amplifier (PGA1) of the conditioning chain may be connected to the internal / external sensors in some different ways. Each sensor has its own connections, programmed in the following EEPROM words:

#	Bits	Name	Content	Value
Sensor 0: Connections configuration word				

19	9:0	**Sensor0_MuxCfg**	Input multiplexer selection bits (connecting the multiplexor inputs to the first amplifier PGA1)	(no decoding)
				Bit[0] = 0 → Mux out1= SENS1 (default)
				Bit[1] = 1 → Mux out1= SENS3
				Bit[2] (not used = 0)
				Bit[3] = 1 → Mux out1= VCM (=VDD/2)
				Bit[4] = 1 → Mux out1=Temp. sensor output1
				Bit[5] = 0 → Mux out2= SENS2 (default)
				Bit[6] = 1 → Mux out2= SENS4
				Bit[7] = 1 → Mux out2= SENSSUP2
				Bit[8] = 1 → Mux out2= VCM
				Bit[9] = 1 → Mux out2=Temp. sensor output2

	15:10	Reserved, **Must be 00000**		
Sensor 1: Connections configuration word				
1F	9:0	**Sensor1_MuxCfg**	Same as above	
Sensor 2: Connections configuration word				
25	9:0	**Sensor2_MuxCfg**	Same as above	

EEPROM #1A, #20, and #26 : Sensor Serial resistances configuration word

Each of the 3 sensors called Sensor0, Sensor1, and Sensor2 can be connected to some serial resistances in order to reduce their current consumption, or to set their common-mode level.

#	Bits	Name	Content	Value
Sensor 0 serial resistance configuration word				
1A	15	**Sensor0_Temp_En**	Temperature sensor enable	Bit[15]=1 -> enables the temperature sensor

	14:0	**Sensor0_Res_Cfg**	Resistance network configuration	Bit[0] (not used=0)
				Bit[1]=1 → SENSSUP2 = VDDA
				Bit[2]=1 → SENS3 = VDDA
				Bit[3] (not used=0)
				Bit[4]=1 → SENSSUP2 = VSS
				Bit[5]=1 → SENS4 = VSS
				Bit[6]=1 → VCM = VDD/2 (enabled)
				Bit[7]=1 → connects prog. res.1 to VDD
				Bit[8]=1 → connects prog. res.2 to VSS
				Bit[9] (not used=0)
				Bit[10]=1 → connects prog. res.1 to SENSSUP2
				Bit[11]=1 → connects prog. res.1 to SENS3
				Bit[12] (not used=0)
				Bit[13]=1 → connects prog. res.2 to SENSSUP2
				Bit[14]=1 → connects prog. res.2 to SENS4

Sensor 1 serial resistance configuration word				
20	15	Same as above	Same as above	
Sensor 2 serial resistance configuration word				
26	15	Same as above	Same as above	

7.8 Non-volatile memories: EEPROM & EE-latches

The MLX90129 embeds a 4kbits EEPROM memory and some EE-Latches bits. This non-volatile memory contains the configuration parameters and some identification numbers. The configuration part of the EEPROM consists of 45 words of 16 bits. The 210 other words are available for the specific needs of the application or may be used for data-logging or for the configuration of the external devices. The read and write access rights are defined for each page and depends on the device wanting to access it: a microcontroller, a RFID base-station or the internal DMA unit of the MLX90129. The user can also lock and unlock some pages by sending the appropriate RFID commands.

7.8.1 Access security

The access to the EEPROM words is protected depending on their content. Four security levels have been defined and can be chosen for any EEPROM page. If any external device tries to access via SPI a memory location without permission, it obtains value 0xFFFF as result. Via RFID, the error response is defined by the standard ISO15693.

- Definition of the different security levels

Security level	Code	Write access	Read access	Typical application
L0	00	SPI, DMA	SPI, DMA	Test
L1	01	SPI, DMA	SPI, RFID, DMA	UID
L2	10	SPI, RFID, DMA	SPI, RFID, DMA	Register file initial configuration, data logging Customer ID, Unlocked User Data
L3	11	Reserved	Reserved	

- EEPROM security access levels

The user data are separated in 8 pages, whose access levels (L0 to L3) are defined thanks to 2 bits, stored in the '*Security Map* Register' of the EEPROM.

EEPROM security map

Page	Address (hex)	Access level	Words	Description
0	0x00 - 0x08	L0	9	Page 0: Melexis ID and device security
1	0x09 - 0x26	programmable	30	Page 1: Register file initial image
2	0x27 - 0x3F	programmable	25	Page 2: User defined data, Customer ID
3	0x40 - 0x5F	programmable	32	Page 3: User defined data
4	0x60 - 0x7F	programmable	32	Page 4: User defined data
5	0x80 - 0x9F	programmable	32	Page 5: User defined data
6	0xA0 - 0xBF	programmable	32	Page 6: User defined data
7	0xC0 - 0xFF	programmable	64	Page 7: User defined data

EEPROM security map register (EEPROM, address #04)

Bits (security level)	Description
[15:14]	Access level for EEPROM Page 7
[13:12]	Access level for EEPROM Page 6
[11:10]	Access level for EEPROM Page 5
[9 : 8]	Access level for EEPROM Page 4
[7 : 6]	Access level for EEPROM Page 3
[5 : 4]	Access level for EEPROM Page 2
[3 : 2]	Access level for EEPROM Page 1
[1 : 0]	Reserved (must be 0x00)

7.8.2 Non-volatile memories content

EEPROM

Register file initial image in EEPROM:

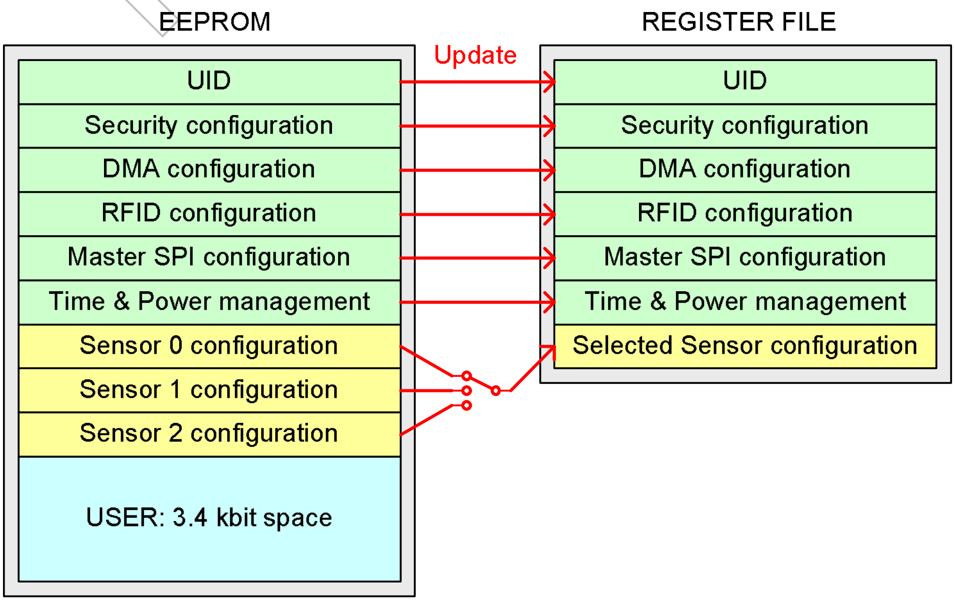
Address	Description
	UID (Unique Identifier)
00	UID: bits 15:0
01	UID: bits 31:16
02	UID: bits 47:32
03	UID: bits 63:48
	Security configuration space
04	EEPROM security map
05	Device security map
06	Password RFID
07	(not used)
08	(not used)
	DMA configuration space
09	DMA: Control word
0A	DMA: Source address word
0B	DMA: Destination address word
0C	DMA: Length
	SPI (External memory) configuration space
0D	External memory: Control word
0E	External memory: Command codes word
	Timer (power control) configuration space
0F	Timer: Period
10	Timer: control word
	Address space always accessible from RFID interface
11	RFID user register: its purpose is user-defined (E.g. it may be used for some fast handshakes between the microcontroller and the RFID base-station).
	Sensors common configuration space
12	Sensor power configuration word
13	(reserved)
14	Sensor trimming and fault-detector configuration word
	Selected sensor configuration space (EEPROM & register file) **
15	Sensor control word
16	Sensor low threshold word
17	Sensor high threshold word
18	Sensor signal conditioner configuration word
19	Sensor connections configuration word
1A	Sensor resistance configuration word

Address	Description
	Extended sensors configuration space (in EEPROM only)
15	*Sensor 0*: Sensor control word
16	*Sensor 0*: Sensor low threshold word
17	*Sensor 0*: Sensor high threshold word
18	*Sensor 0*: Sensor signal conditioner configuration word
19	*Sensor 0*: Sensor connections configuration word
1A	*Sensor 0*: Sensor resistance configuration word
1B	*Sensor 1*: Sensor control word
1C	*Sensor 1*: Sensor low threshold word
1D	*Sensor 1*: Sensor high threshold word
1E	*Sensor 1*: Sensor signal conditioner configuration word
1F	*Sensor 1*: Sensor connections configuration word
20	*Sensor 1*: Sensor resistance configuration word
21	*Sensor 2*: Sensor control word
22	*Sensor 2*: Sensor low threshold word
23	*Sensor 2*: Sensor high threshold word
24	*Sensor 2*: Sensor signal conditioner configuration word
25	*Sensor 2*: Sensor connections configuration word
26	*Sensor 2*: Sensor resistance configuration word
27	Internal device backup word 1
28	Internal device backup word 2

(**) In the register file, this configuration space is updated from the appropriate part of the *Extended sensor configuration space* at each access to one of the three sensors. This configuration space and all others with higher addresses are not updated during a *Register File Update* operation.

7.8.3 Image of the Register File

The EEPROM contains the initial image of the *Register File*. This image is copied after the power-on, or upon a SPI / RFID *Update* request. The sensor configuration in the *Register File* depends on the currently selected sensor.



7.8.4 EE latches

Another kind of non-volatile memory is used to store the trimming / configuration bits that should be immediately available: the EE-Latch bank. They are mainly used for the trimming of the oscillators and the capacitance of the antenna, for security and power management. It is important to read its value before re-programming it, in order to not erase some trimming bits.

EE-Latch map: (*Internal Devices Domain*, Address #03 and #04)

#	Bits	Name	**Description** (when the bit is asserted high)
03h	**4:0**	**LFO_Freq_Trim** (Trimming bits)	(used by Melexis)
	6:5	**Bias_Cur_Trim** (Trimming bits)	(used by Melexis)
	7	**DisableAutoLoading**	Disables the automatic loading of the Register File with its image from the EEPROM after a power-on reset from the battery
	10:8	**HFO_Freq_Trim** (Trimming bits)	(used by Melexis)
	13:11	**VReg_Trim** (Trimming bits)	(used by Melexis)
	14	**RCb_Quartz**	Selects the low-frequency RC-oscillator LFO (=0) or the quartz-oscillator XLFO (=1)
	15	**Disconnect_Vfield_Vbat**	Disconnects the pads VFIELD and VBAT, when not using the energy from the field to supply the whole device.
04h	**1:0**	Not used	(Must be 0)
	2	**VReg_Dis**	Disables the VReg regulator and shorts-cut its output to Vbat
	3	**VReg_LV**	Low-voltage option for the VREG regulator and the sensor regulator
	7:4	Reserved	(Must be 0)
	14:8	**RFID_EEPROM_Lock_Map****	Map of pages in EEPROM, to be locked for RFID write, using the "*Lock*" command
	15	**RFID_Device_Lock****	Locks the RFID device
09h	**4:0**	**CTC_Trimming**	Trimming of the integrated capacitance, part of the RFID antenna
	15:5	Not used	(Must be 0)

(**) - following fields are not accessible for write from RFID interface via device write command.

7.8.5 EE-Latches backup in EEPROM

The content of EE-Latches (Internal devices #03, #04 and #09) are copied in the EEPROM for backup:

EEPROM #27 and #28

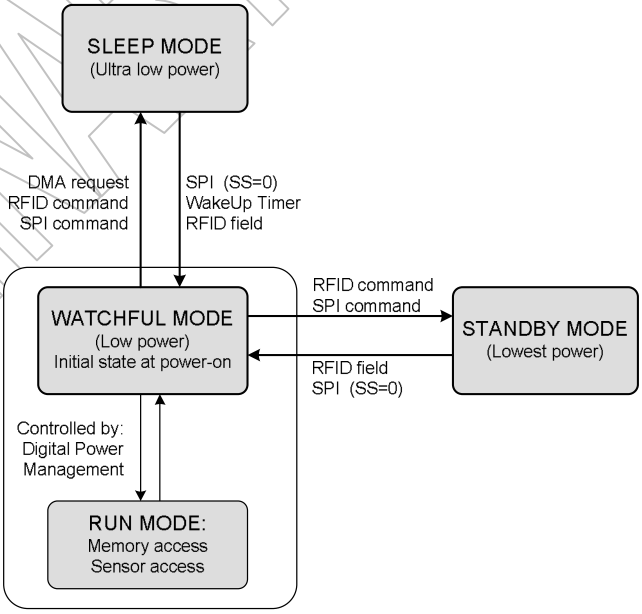
#	Bits	Description
		Internal device backup word 1
27	**15:0**	Copy of internal device #03 bits [15:0]
		Internal device backup word 2
28	**1:0**	Copy of internal device #09 bits [1:0]
	3:2	Copy of internal device #03 bits [3:2]
	7:4	Copy of internal device #09 bits [4:2]
	15:8	Copy of internal device #03 bits [15:8]

7.9 Power management

The power management unit controls the following features of the MLX90129:

- Start-up modes (with or without battery)
- Power modes (stand-by, sleep, watchful or run mode)
- Energy scavenging for battery-less applications
- Oscillators management (digital clock, wake-up timer)

7.9.1 Power modes



Power-off mode
No battery, no field. The MLX90129 can quit this mode when a battery is connected or when a RF field is applied.

Watchful mode
This mode is the initial state, after power-on. In this state, the digital part is activated; the MLX90129 can receive commands from the RFID or SPI.

Run mode
Depending on the command from SPI or RFID, or on request from DMA, the MLX90129 enters the Run mode, where all the blocks implied in the transaction are powered. This state is not low-power, but time-limited.

Stand-by mode
In the stand-by mode, the supply voltage is applied, but the MLX90129 consumes a minimum current. Typically, this mode is used after the module has been assembled and tested. Then, it can be stored for a long time without wasting the battery energy.
The Digital Controller can not exit this mode by itself. It can only exit it by an external interrupt: emission of a RFID field or asserting low the Slave Select input of the SPI.
The MLX90129 may re-enter this mode upon request from SPI or RFID (in writing the Wake-up Timer configuration word). It is possible to enter this mode after a programmed count-down from the Wake-up timer, or after a logging sequence.
After switching from the stand-by or sleep modes, the external micro-controller (or the RFID base-station) must wait for a defined initialization time before sending any new commands.

Sleep mode
In the *Sleep mode*, only the wake-up timer works and sends an IRQ pulse (Interrupt Request) to the microcontroller after a programmable time period. The MLX90129 may leave this mode upon interrupt that may come from the RFID (field detected), from the SPI (SS=0) or on request from the DMA to run an acquisition after a defined time period. In this mode, it is possible to power-down the external device supplied by VREG.

7.9.2 Oscillators management

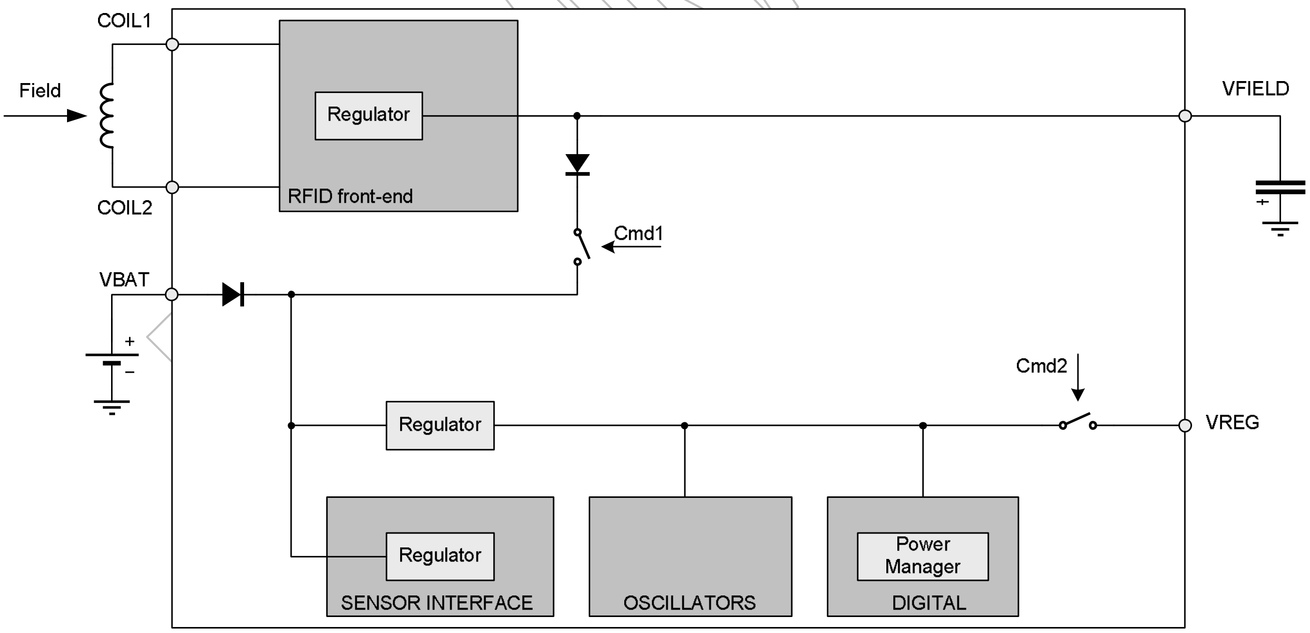
The MLX90129 contains 3 oscillators:

- A low-power low-frequency RC-oscillator (that may be used as a wake-up timer)
- A low-power low-frequency quartz oscillator (that may also be used as an accurate wake-up timer)
- A 5MHz RC-oscillator for the digital clock

The two RC-oscillators have their frequency adjustable, by programming the ee-Latch bank. The use of the quartz oscillator is optional. If it is chosen instead of the RC-oscillator, then a 32.768kHz crystal should be connected between the pads XIN and XOUT.

7.9.3 Energy scavenging

The MLX90129 embeds power supply management capabilities which allow a strong flexibility to design motes or data logger devices with strong power consumption constraints. It is possible to store the energy from the incoming magnetic field into an external capacitor, on pad VFIELD or to run from a coin cell battery.



The power management mode is defined by the switches Cmd1 and Cmd2 and is configurable through the EEPROM and EE-Latch.

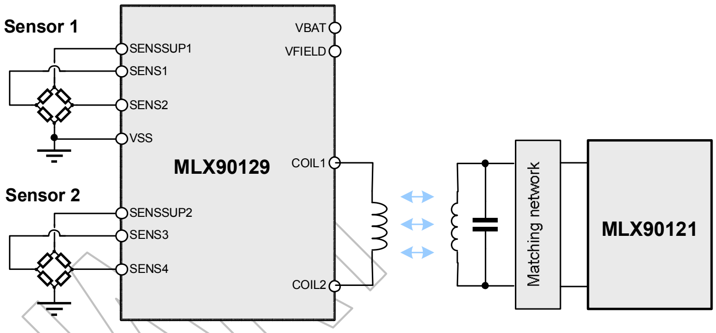
- For the battery-less applications, VFIELD pad can be used to supply the MLX90129 if the switch between VFIELD and VBAT (Cmd1) is closed.
- For battery applications, the switch between VFIELD and VBAT should (Cmd1) be open
- For both kind of application, it is possible to supply the external device via VREG, either at any time, or only in watchful state (Cmd2)

The commands of these switches are defined as:
Cmd1: *Disconnect_Vfield_Vbat* = EElatch #03, bit 15.
Cmd2: *ExtSupply_En* = EEPROM #12, bit 13
They must be set to close the switches.

8 Application Information

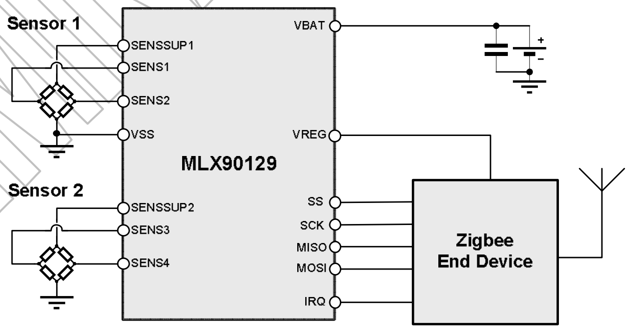
1. RFID sensor tag

The MLX90129 may be used as a 13.56 MHz sensor transponder. The L-C antenna is easy to implement and to tune thanks to the integrated programmable capacitance. A battery may be used for a higher communication distance, or when using some low impedance sensors.



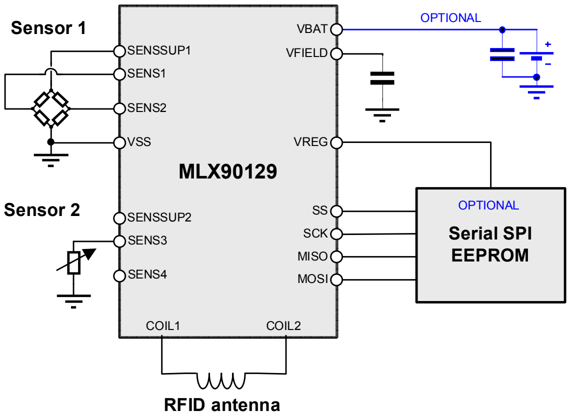
2. Zigbee RF sensor tag

The MLX90129 may be coupled with a Zigbee End Device. This device may communicate via SPI and control the configuration registers thanks to its customer application layer. It may be supplied and waken-up by the MLX90129 IRQ, depending on the programmed behaviour. The MLX90129 may also be used to initiate a Zigbee communication.



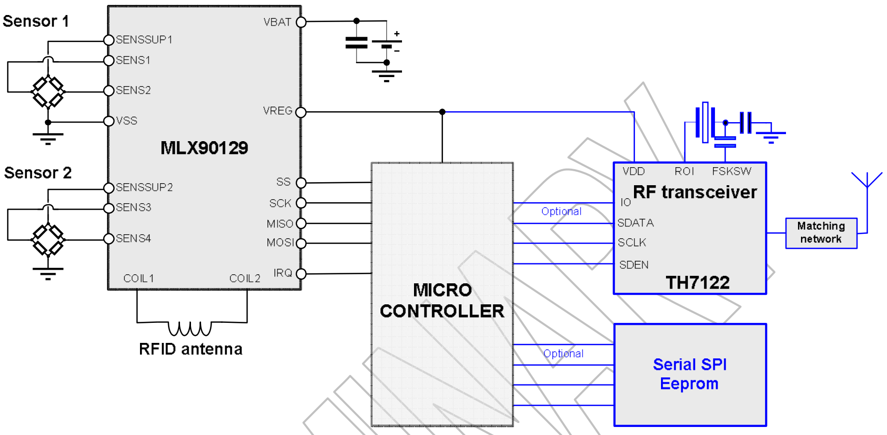
3. Data logger

The MLX90129 may be used in a standalone way as a data logger. The data may be stored in the internal EEPROM or in an external serial SPI EEPROM. Using the *automatic logging mode*, the MLX91029 wakes-up each programmed time period, converts the sensor data and stores it in the selected memory. This process may be hold or stopped by an external SPI master (microcontroller,…) or a RFID base-station. The data stored in EEPROM may be read via RFID.



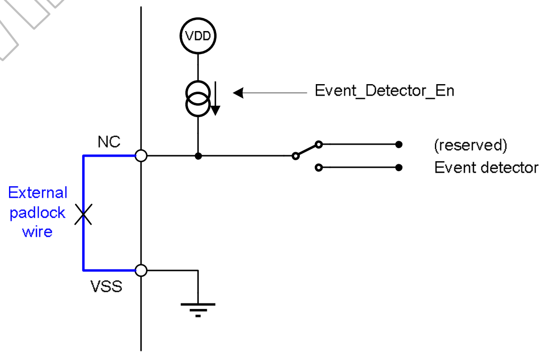
4. Micro-controller based applications

Numerous flexible applications using a microcontroller can be imagined. The microcontroller may manage the MLX90129 to sense, store or send the data via RFID. It may also control a RF transceiver as the TH7122 and an external non-volatile memory (serial SPI EEPROM).



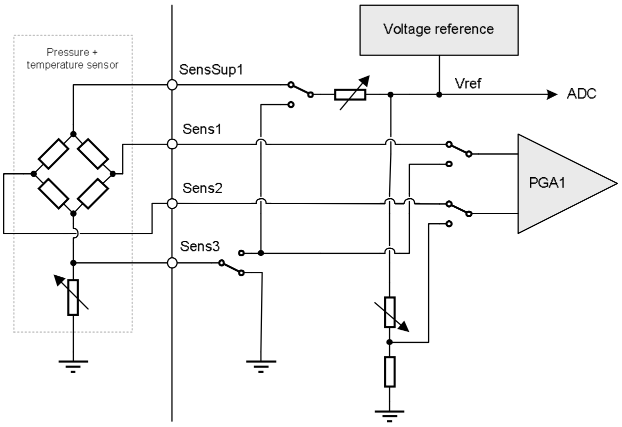
5. Padlock application

When the event detection system is enabled, a padlock may be made with a wire connected between the pins NC and VSS. If this wire is broken, this event is memorized, and an interrupt can (optionally) be sent to the external micro-controller. Instead of the wire, a light sensor (solar cell) may be connected. When powered, it sets an IRQ to the controller.



6. Serial resistor connected to the external sensor(s)

Numerous connections are possible between the external sensor and the internal resistors. The following figure shows an example of these possibilities.



9 Reliability Information

Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

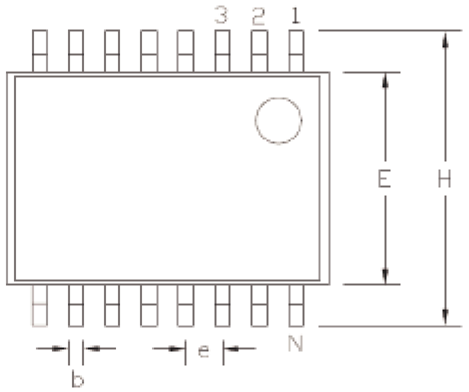
Melexis is contributing to global environmental conservation by PROMoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx.

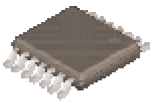
10 ESD Precautions

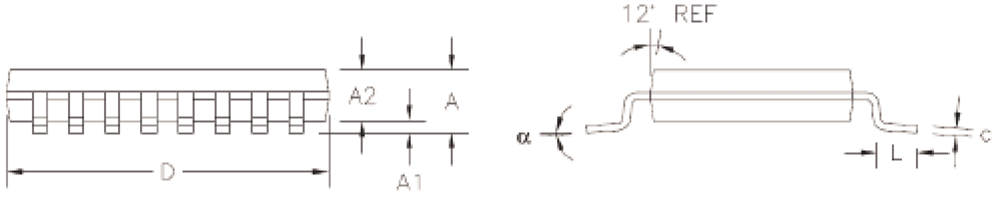
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

11 Package Information

TSSOP20:



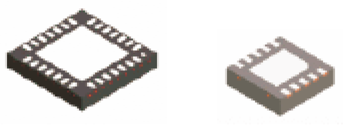


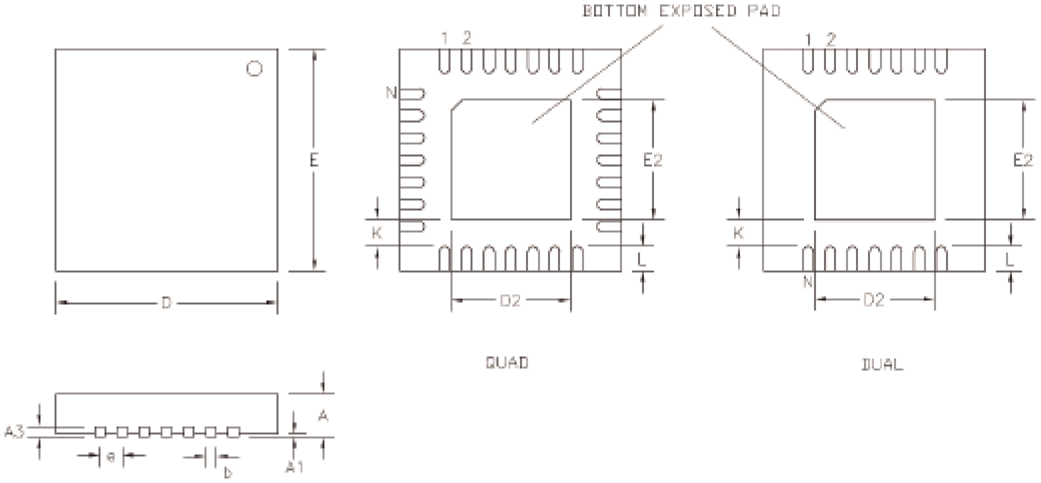


This table in mm

N		A	A1	A2	D	E	H	L	b	c	e	α
8	min	–	0.05	0.85	2.90	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	3.10	4.50	BSC	0.75	0.30	0.20	BSC	8°
14	min	–	0.05	0.85	4.90	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	5.10	4.50	BSC	0.75	0.30	0.20	BSC	8°
16	min	–	0.05	0.85	4.90	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	5.10	4.50	BSC	0.75	0.30	0.20	BSC	8°
20	min	–	0.05	0.85	6.40	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	6.60	4.50	BSC	0.75	0.30	0.20	BSC	8°
24	min	–	0.05	0.85	7.70	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	7.90	4.50	BSC	0.75	0.30	0.20	BSC	8°
28	min	–	0.05	0.85	9.60	4.30	6.40	0.50	0.19	0.09	0.65	0°
	max	1.10	0.15	0.95	9.80	4.50	BSC	0.75	0.30	0.20	BSC	8°

QFN4x4: 20 Leads.





This table in mm

Type	D x E	N	e		A	A1	A3	D2	E2	L	K	b
Dual	3 x 3	10	0.50	min	0.80	0.00	0.20	2.23	1.49	0.30	0.20	0.18
				max	1.00	0.05	REF	2.48	1.74	0.50	–	0.30
	5 x 5	8	0.80	min	0.80	0.00	0.20	3.65	3.05	0.45	0.20	0.25
				max	1.00	0.05	REF	3.90	3.30	0.65	–	035
Quad	4 x 4	16	0.65	min	0.80	0.00	0.20	1.95	1.95	0.50	0.20	0.25
				max	1.00	0.05	REF	2.20	2.20	0.70	–	0.35
	4 x 4	20	0.50	min	0.80	0.00	0.20	2.50	2.50	0.35	0.20	0.18
				max	1.00	0.05	REF	2.70	2.70	0.45	–	0.30
	5 x 5	20	0.65	min	0.80	0.00	0.20	3.00	3.00	0.45	0.20	0.25
				max	1.00	0.05	REF	3.25	3.25	0.65	–	0.35
		32	0.50	min	0.80	0.00	0.20	3.35	3.35	0.30	0.20	0.18
				max	1.00	0.05	REF	3.70	3.70	0.50	–	0.30
	6 x 6	28	0.65 (Opt.A)	max	1.00	0.05	0.20	3.25	3.25	0.50	0.20	0.30
				max	1.00	0.05	REF	3.80	3.80	0.65	–	0.35
		28	0.65 (Opt.B)	min	0.80	0.00	0.20	4.50	4.50	0.35	0.20	0.25
				max	1.00	0.05	REF	4.70	4.70	0.45	–	0.35
		40	0.50	min	0.80	0.00	0.20	4.30	4.30	0.45	0.20	0.18
				max	1.00	0.05	REF	4.50	4.50	0.55	–	0.30
	7 x 7	28	0.80	min	1.40	0.00	0.20	4.95	4.95	0.50	0.20	0.25
				max	1.60	0.05	REF	5.20	5.20	0.70	–	0.35
		32	0.65	min	0.80	0.00	0.20	5.00	5.00	0.45	0.20	0.25
				max	1.00	0.05	REF	5.20	5.20	0.55	–	0.35
		48	0.50	min	0.80	0.00	0.20	5.00	5.00	0.45	0.20	0.18
				max	1.00	0.05	REF	5.20	5.20	0.55	–	0.30

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Europe, Africa:	Americas:	Asia:
Phone: +32 1367 0495	Phone: +1 603 223 2362	Phone: +32 1367 0495
E-mail: sales_europe@melexis.com	E-mail: sales_usa@melexis.com	E-mail: sales_asia@melexis.com