3-Pin Microprocessor Reset Monitors

The MAX809 and MAX810 are cost–effective system supervisor circuits designed to monitor $V_{\rm CC}$ in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 20 µsec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a minimum of 140 msec after V_{CC} rises above the reset threshold. The MAX810 has an active–high RESET output while the MAX809 has an active–low \overline{RESET} output. The output of the MAX809 is guaranteed valid down to $V_{CC}=1.0$ V. Both devices are available in a SOT–23 package.

The MAX809/810 are optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 17 μ A (V_{CC} = 3.3 V) makes these devices suitable for battery powered applications.

Features

- Precision V_{CC} Monitor for 3.0 V, 3.3 V, and 5.0 V Supplies
- 140 msec Guaranteed Minimum RESET, RESET Output Duration
- RESET Output Guaranteed to $V_{CC} = 1.0 \text{ V (MAX809)}$
- Low 17 μA Supply Current
- V_{CC} Transient Immunity
- Small SOT-23 Package
- No External Components
- Wide Operating Temperature: -40°C to 85°C

Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical µP Power Supply Monitoring

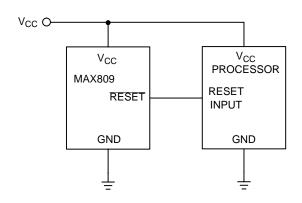


Figure 1. Typical Application Diagram



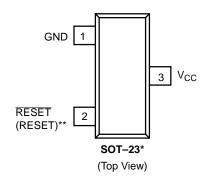
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SOT-23 (TO-236) CASE 318

PIN CONFIGURATION



NOTE: *SOT-23 is equivalent to JEDEC (TO-236)

- ** RESET is for MAX809
- ** RESET is for MAX810

ORDERING INFORMATION

Device	Package	Shipping
MAX809xTR	SOT-23	3000 Tape/Reel
MAX810xTR	SOT-23	3000 Tape/Reel

NOTE: The "x" denotes a suffix for V_{CC} threshold – see table on page 6.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage (V _{CC} to GND)		6.0	V
RESET, RESET		-0.3 to (V _{CC} + 0.3)	V
Input Current, V _{CC}		20	mA
Output Current, RESET, RESET		20	mA
dV/dt (V _{CC})		100	V/μsec
Power Dissipation ($T_A \le 70^{\circ}C$) SOT-23 (derate 4.0 mW/°C above +70°C)	P _D	230	mW
Operating Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T _{sol}	+260	°C

^{*}Maximum Ratings are those values beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS (V_{CC} = Full Range, T_A = -40° C to $+85^{\circ}$ C unless otherwise noted. Typical values are at T_A = $+25^{\circ}$ C, V_{CC} = 5.0 V for L/M/J, 3.3 V for T/S, 3.0 V for R) (Note 1.)

Characteristic	Symbol	Min	Тур	Max	Unit
V_{CC} Range $T_A = 0$ °C to +70°C $T_A = -40$ °C to +85°C		1.0 1.2	- -	5.5 5.5	V
Supply Current MAX8xxL/M/J: V _{CC} < 5.5 V MAX8xxR/S/T: V _{CC} < 3.6 V	Icc	- -	24 17	60 50	μΑ
Reset Threshold (Note 1.) $MAX8xxL: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX8xxM: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX809J: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX80XT: T_A = 25^{\circ}C$ $MAX8xXT: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX8xXS: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX8xXS: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $MAX8xXR: T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	V _{TH}	4.56 4.50 4.31 4.25 3.93 3.89 3.04 3.00 2.89 2.85 2.59 2.55	4.63 - 4.38 - 4.00 - 3.08 - 2.93 - 2.63	4.70 4.75 4.45 4.50 4.06 4.10 3.11 3.15 2.96 3.00 2.66 2.70	V
Reset Threshold Temperature Coefficient		_	30	-	ppm/°C
V_{CC} to Reset Delay $V_{CC} = V_{TH}$ to $(V_{TH} - 100 \text{ mV})$		_	20	-	μsec
Reset Active Timeout Period		140	240	560	msec
	V _{OL}	- - -	- - -	0.3 0.4 0.3	V
RESET Output Voltage High (MAX809) MAX809R/S/T: $V_{CC} > V_{TH}$ max, $I_{SOURCE} = 500$ μA MAX809L/M/J: $V_{CC} > V_{TH}$ max, $I_{SOURCE} = 800$ μA	V _{OH}	0.8 V _{CC} V _{CC} – 1.5	- -	- -	V
RESET Output Voltage Low (MAX810) MAX810R/S/T: $V_{CC} = V_{TH}$ max, $I_{SINK} = 1.2$ mA MAX810L/M/J: $V_{CC} = V_{TH}$ max, $I_{SINK} = 3.2$ mA	V _{OL}	- -	- -	0.3 0.4	V
RESET Output Voltage High (MAX810) 1.8 < V _{CC} < V _{TH} min, I _{SOURCE} = 150 μA	V _{OH}	0.8 V _{CC}	-	_	V

^{1.} Production testing done at $T_A = 25^{\circ}C$, over temperature limits guaranteed by design.

PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground
2	RESET (MAX809)	$\overline{\text{RESET}} \text{ output remains low while V}_{\text{CC}} \text{ is below the reset voltage threshold, and for 240 msec (typ.)}$ after V_{CC} rises above reset threshold
2	RESET (MAX810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for 240 msec (typ.) after V_{CC} rises above reset threshold
3	V _{CC}	Supply Voltage (typ.)

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The MAX809/810 provides accurate $V_{\rm CC}$ monitoring and reset timing during power–up, power–down, and brownout/sag conditions, and rejects negative–going transients (glitches) on the power supply line. Figure 2 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies **under** the curve will **not** generate a reset signal. Combinations above the curve are detected as a brownout or power–down. Typically, transient that goes 100 mV below the reset threshold and lasts 20 μ s or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the $V_{\rm CC}$ pin of the MAX809/810.

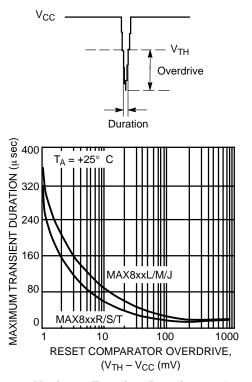


Figure 2. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

RESET Signal Integrity During Power-Down

The MAX809 \overline{RESET} output is valid to $V_{CC}=1.0~V$. Below this voltage the output becomes an "open circuit" and does not sink current. This means CMOS logic inputs to the μP will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where \overline{RESET} must be maintained valid to $V_{CC}=0~V$, a pull–down resistor must be connected

from \overline{RESET} to ground to discharge stray capacitances and hold the output low (Figure 3). This resistor value, though not critical, should be chosen such that it does not appreciably load \overline{RESET} under normal operation (100 k Ω will be suitable for most applications). Similarly, a pull–up resistor to V_{CC} is required for the MAX810 to ensure a valid high \overline{RESET} for V_{CC} below 1.0 V.

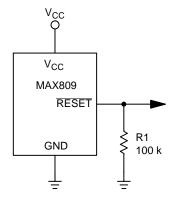


Figure 3. Ensuring RESET Valid to $V_{CC} = 0 V$

Processors With Bidirectional I/O Pins

Some μ P's (such as Motorola 68HC11) have bi–directional reset pins. Depending on the current drive capability of the processor pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a 4.7 k Ω resistor in series with the output of the MAX809/810 (Figure 4). If there are other components in the system which require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the μ P, the buffer should be connected as shown with the solid line.

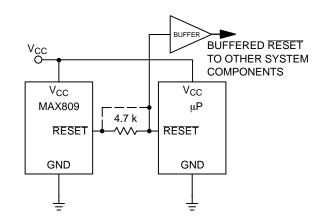


Figure 4. Interfacing to Bidirectional Reset I/O

TYPICAL CHARACTERISTICS

30

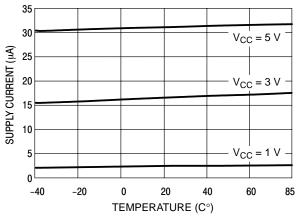


Figure 5. Supply Current vs. Temperature (No Load, MAX8xxR/S/T)

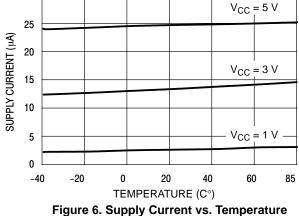


Figure 6. Supply Current vs. Temperature (No Load, MAX8xxL/M/J/)

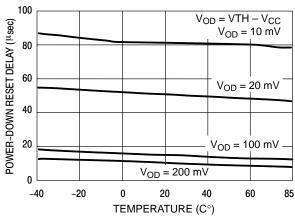


Figure 7. Power–Down Reset Delay vs.
Temperature and Overdrive (MAX8xxR/S/T)

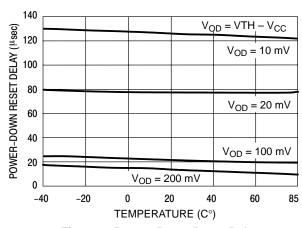


Figure 8. Power–Down Reset Delay vs. Temperature and Overdrive (MAX8xxL/M/J)

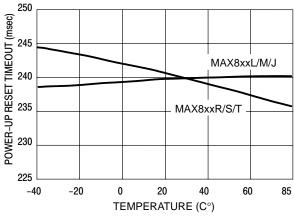


Figure 9. Power–Up Reset Timeout vs.
Temperature

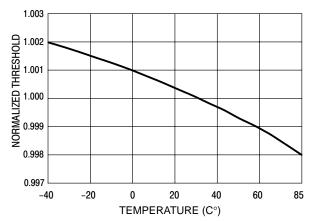
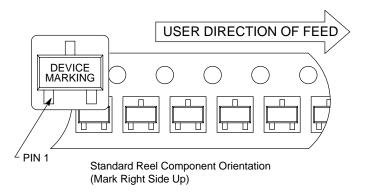


Figure 10. Normalized Reset Threshold vs.
Temperature

TAPING FORM

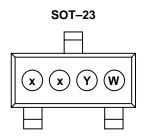
Component Taping Orientation for 3L SOT-23 (JEDEC-236) Devices



Tape & Reel Specifications Table

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOT-23	8 mm	4 mm	3000	7 inches

MARKING DIAGRAM



xx = Specific Device Code

Y = Year

W = Work Week

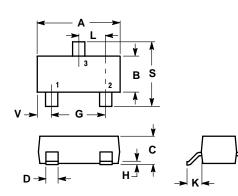
MARKING

ON Semiconductor Part #	Reset V _{CC} Threshold (V) or Address	Marking
MAX809L	4.63	J1YW
MAX809M	4.38	J2YW
MAX809T	3.08	J3YW
MAX809S	2.93	J4YW
MAX809R	2.63	J5YW
MAX809J*	4.00	J6YW
MAX810L	4.63	K1YW
MAX810M	4.38	K2YW
MAX810T	3.08	K3YW
MAX810S	2.93	K4YW
MAX810R	2.63	K5YW

^{*} J version is available for MAX809 only

PACKAGE DIMENSIONS

SOT-23 PLASTIC PACKAGE (TO-236) CASE 318-08 **ISSUE AF**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.1102	0.1197	2.80	3.04
В	0.0472	0.0551	1.20	1.40
С	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
Н	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
٧	0.0177	0.0236	0.45	0.60

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