

Features

- **Maximum Acquisition Time**
 - 10V Step to 0.1% 4 μ s
 - 10V Step to 0.01% 6 μ s
- **Maximum Drift Current 10nA**
(Maximum Over Temperature)
- **TTL Compatible Control Input**
- **Power Supply Rejection \geq 80dB**
- **Total Gamma Dose 1 x 10⁵ RAD(SI)**
- **No Latch-Up**

Applications

- **Data Acquisition Systems**
- **D to A Deglitcher**
- **Auto Zero Systems**
- **Peak Detector**
- **Gated Op Amp**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-2420RH-Q	-55°C to +125°C	14 Lead CerDIP

Description

The HS-2420RH is a radiation hardened monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

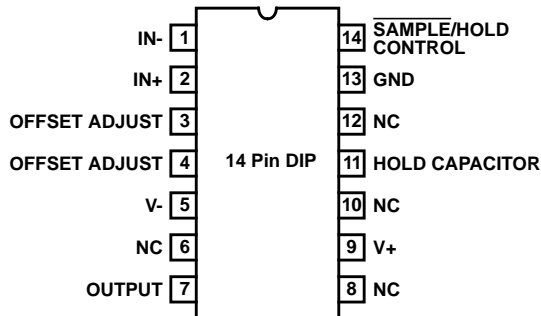
With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operation amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

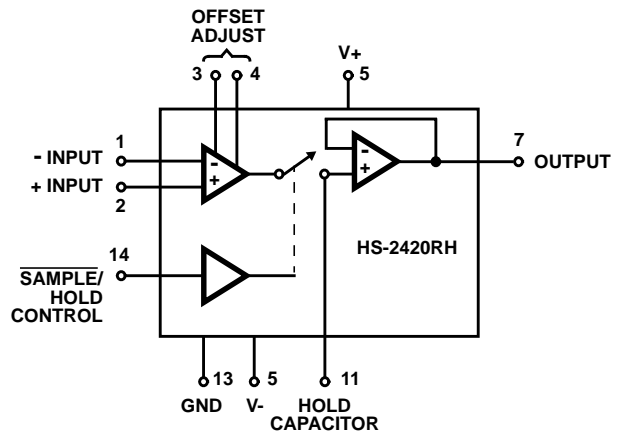
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

Pinout

14 LEAD CERAMIC DUAL-IN-LINE
FRIT SEAL PACKAGE (CerDIP)
MIL-STD-1835, GDIP1-T14
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Specifications HS-2420RH

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	+40V
Differential Input Voltage	±24V
Digital Input Voltage (S/H Pin)	+8V, -15V
Output Current	Short Circuit Protected
Storage Temperature Range	-65°C < T _A < +150°C
Lead Temperature (Soldering 10s)	+275°C
Junction Temperature	+175°C

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	74°C/W	18°C/W
Maximum Power Dissipation at +125°C		
CerDIP Package	0.68W	
If Device Power Exceeds Package Dissipation Capability, Derate Linearly at the Following Rate		
CerDIP Package	13.5mW/°C	
ESD Classification	≤2000V	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Operating Temperature Range	-55°C < T _A < +125°C	Logic Level Low (VIL)	0.0V to 0.8V
Operating Supply Voltage (± VSUPPLY)	±15V	Logic Level High (VIH)	2.0V to 5.0V
Analog Input Voltage (VS)	±10V		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V, V- = -15V, VIL = 0.8V (Sample); VIH = 2.0V (Hold); CH = 1000pF, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	VIO		1	+25°C	-4	4	mV
			2, 3	-55°C, +125°C	-6	6	mV
Input Bias Current	IB+		1	+25°C	-200	200	nA
			2, 3	-55°C, +125°C	-400	400	nA
	IB-		1	+25°C	-200	200	nA
			2, 3	-55°C, +125°C	-400	400	nA
Input Offset Current	IIO		1	+25°C	-50	50	nA
			2, 3	-55°C, +125°C	-100	100	nA
Open Loop Voltage Gain	+AVS	RL = 2kΩ, CL = 50pF, VOUT = +10V	1	+25°C	25	-	kV/V
			2, 3	-55°C, +125°C	25	-	kV/V
	-AVS		1	+25°C	25	-	kV/V
			2, 3	-55°C, +125°C	25	-	kV/V
Common Mode Rejection Ratio	-CMRR	V+ = 25V, V- = -5V, VOUT = +10V, VS/H = 10.8V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
	+CMRR		1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
Output Current	+IO	VOUT = +10V	1	+25°C	+15.0	-	mA
	-IO	VOUT = -10V	1	+25°C	-15.0	-	mA
Output Voltage Swing	+VOP	RL = 2kΩ, CL = 50pF	1	+25°C	+10.0	-	V
			2, 3	-55°C, +125°C	-10.0	-	V
	-VOP		1	+25°C	-	-10.0	V
			2, 3	-55°C, +125°C	-	-10.0	V
Power Supply Current	+ICC		1	+25°C	-	5.5	mA
	-ICC		1	+25°C	-3.5	-	mA
Power Supply Rejection Ratio	+PSRR	V+ = 10V and 20V, V- = -15V and -15V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
	-PSRR		1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB

Specifications HS-2420RH

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_{IL} = 0.8V$ (Sample); $V_{IH} = 2.0V$ (Hold); $CH = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Digital Input Current	IIN1	VIN1 = 0V	1	+25°C	-	800	μA
			2, 3	-55°C, +125°C	-	800	μA
	IIN2	VIN2 = 5.0V	1	+25°C	-	20	μA
			2, 3	-55°C, +125°C	-	20	μA
Digital Input Voltage	VIL		1	+25°C	-	0.8	V
			2, 3	-55°C, +125°C	-	0.8	V
	VIH		1	+25°C	2.0	-	V
			2, 3	-55°C, +125°C	2.0	-	V
Drift Current	ID	VIN = 0V, RL = 2kΩ, CL = 50pF, S/H = 4.0V	2	+125°C	-10	10	nA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_{IL} = 0.8V$ (Sample), $V_{IH} = 2.0V$ (Hold), $CH = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Step Error	VERROR	VS/H = 0V and 4V, tRISE (VS/H) ≈ 30ns (Note 1)	9	+25°C	-20	20	mV
Transient Response Rise Time and Fall Time	TR(TR)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 200mVP-P	9	+25°C	-	100	ns
	TR(TF)		9	+25°C	-	100	ns
Transient Response Overshoot	TR(+OS)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 200mVP-P	9	+25°C	-	40	%
	TR(-OS)		9	+25°C	-	40	%
Transient Response Slew Rate	TR(+SR)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 10VP-P	9	+25°C	3.5	-	V/μs
	TR(-SR)		9	+25°C	3.5	-	V/μs

NOTE:

1. VERROR = VOUT (VS/H = 0V) - VOUT (VS/H = 4V)

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_{IL} = 0.8V$ (Sample), $V_{IH} = 2.0V$ (Hold), $CH = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Mode Feedthrough Attenuation	VATTEN	RL = 2kΩ, CL = 50pF, AV = +1, VIN = 20VP-P, fIN = 50kHz	1	+25°C, -55°C, +125°C	70	-	dB
Gain Bandwidth Product	GBWP	RL = 2kΩ, CL = 50pF, AV = +1, VIN = 100mVP-P	1	+25°C	2.5	-	MHz
Acquisition Time (0.1%)	+tACQ (0.1%)	RL = 2kΩ, CL = 50pF, AV = +1, VOUT = 0V and +10V	1	+25°C	-	4	μs
	-tACQ (0.1%)	RL = 2kΩ, CL = 50pF, AV = +1, VOUT = 0V and -10V	1	+25°C	-	4	μs
Acquisition Time (0.01%)	+tACQ (0.01%)	RL = 2kΩ, CL = 50pF, AV = +1, VOUT = 0V and +10V	1	+25°C	-	6	μs
	-tACQ (0.01%)	RL = 2kΩ, CL = 50pF, AV = +1, VOUT = 0V and -10V	1	+25°C	-	6	μs

NOTE: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Specifications HS-2420RH

TABLE 4. DC ELECTRICAL PERFORMANCE CHARACTERISTICS POST 100KRAD

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_{IL} = 0.8V$ (Sample); $V_{IH} = 2.0V$ (Hold); $CH = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V _{IO}		1	+25°C	-6	6	mV
Input Bias Current	IB+		1	+25°C	-400	400	nA
	IB-		1	+25°C	-400	400	nA
Input Offset Current	I _{IO}		1	+25°C	-100	100	nA
Open Loop Voltage Gain	+AVS	R _L = 2kΩ, C _L = 50pF, V _{OUT} = +10V	1	+25°C	25	-	kV/V
			2, 3	-55°C, +125°C	25	-	kV/V
	-AVS	R _L = 2kΩ, C _L = 50pF, V _{OUT} = -10V	1	+25°C	25	-	kV/V
			2, 3	-55°C, +125°C	25	-	kV/V
Common Mode Rejection Ratio	-CMRR	V ₊ = 25V, V ₋ = -5V, V _{OUT} = +10V, V _{S/H} = 10.8V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
	+CMRR	V ₊ = 5V, V ₋ = -25V, V _{OUT} = -10V, V _{S/H} = 9.2V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
Output Current	+I _O	V _{OUT} = +10V	1	+25°C	+12.0	-	mA
	-I _O	V _{OUT} = -10V	1	+25°C	-12.0	-	mA
Output Voltage Swing	+V _{OP}	R _L = 2kΩ, C _L = 50pF	1	+25°C	+10.0	-	V
			2, 3	-55°C, +125°C	+10.0	-	V
	-V _{OP}	R _L = 2kΩ, C _L = 50pF	1	+25°C	-	-10.0	V
			2, 3	-55°C, +125°C	-	-10.0	V
Power Supply Current	+I _{CC}		1	+25°C	-	5.5	mA
	-I _{CC}		1	+25°C	-3.5	-	mA
Power Supply Rejection Ratio	+PSRR	V ₊ = 10V and 20V, V ₋ = -15V and -15V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
	-PSRR	V ₊ = 15V and 15V, V ₋ = -10V and -20V	1	+25°C	80	-	dB
			2, 3	-55°C, +125°C	80	-	dB
Digital Input Current	I _{IN1}	V _{IN1} = 0V	1	+25°C	-	800	μA
			2, 3	-55°C, +125°C	-	800	μA
	I _{IN2}	V _{IN2} = 5.0V	1	+25°C	-	20	μA
			2, 3	-55°C, +125°C	-	20	μA
Digital Input Voltage	V _{IL}		1	+25°C	-	0.8	V
			2, 3	-55°C, +125°C	-	0.8	V
	V _{IH}		1	+25°C	2.0	-	V
			2, 3	-55°C, +125°C	2.0	-	V
Drift Current	I _D	V _{IN} = 0V, R _L = 2kΩ, C _L = 50pF, S/H = 4.0V	2	+125°C	-10	10	nA

Specifications HS-2420RH

TABLE 4A. AC ELECTRICAL PERFORMANCE CHARACTERISTICS POST 100KRAD

Device Tested at V+ = +15V, V- = -15V, VIL = 0.8V (Sample), VIH = 2.0V (Hold), CH = 1000pF, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Step Error	VERROR	VS/H = 0V and 4V, tRISE (VS/H) ≈ 30ns (Note 1)	9	+25°C	-20	20	mV
Transient Response Rise Time and Fall Time	TR(TR)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 200mVP-P	9	+25°C	-	100	ns
	TR(TF)		9	+25°C	-	100	ns
Transient Response Overshoot	TR(+OS)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 200mVP-P	9	+25°C	-	40	%
	TR(-OS)		9	+25°C	-	40	%
Transient Response Slew Rate	TR(+SR)	CL = 50pF, RL = 2kΩ, AV = +1, VOUT = 10VP-P	9	+25°C	2.0	-	V/μs
	TR(-SR)		9	+25°C	2.0	-	V/μs

NOTE:

1. VERROR = VOUT (VS/H = 0V) - VOUT (VS/H = 4V)

TABLE 5. BURN-IN DELTA PARAMETERS (TA = +25°C)

PARAMETERS	DELTA LIMITS
VIO	±2.0mV
IBIAS	±75nA
IIO	±75nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	
		TESTED FOR -Q	RECORDED FOR -Q
Initial Test	100% 5004	1, 9	1
Interim Test	100% 5004	1, 9, Δ	1, Δ
PDA	100% 5004	1, Δ	
Final Test	100% 5004	2, 3, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3	1, 2, 3
Subgroup B6	Sample 5005	1	
Group D	Sample 5005	1	
Group E, Subgroup 2	Sample 5005	1	

NOTE: Alternate Group A testing may be exercised in accordance with Method 5005 of MIL-STD-883.

Test Circuits

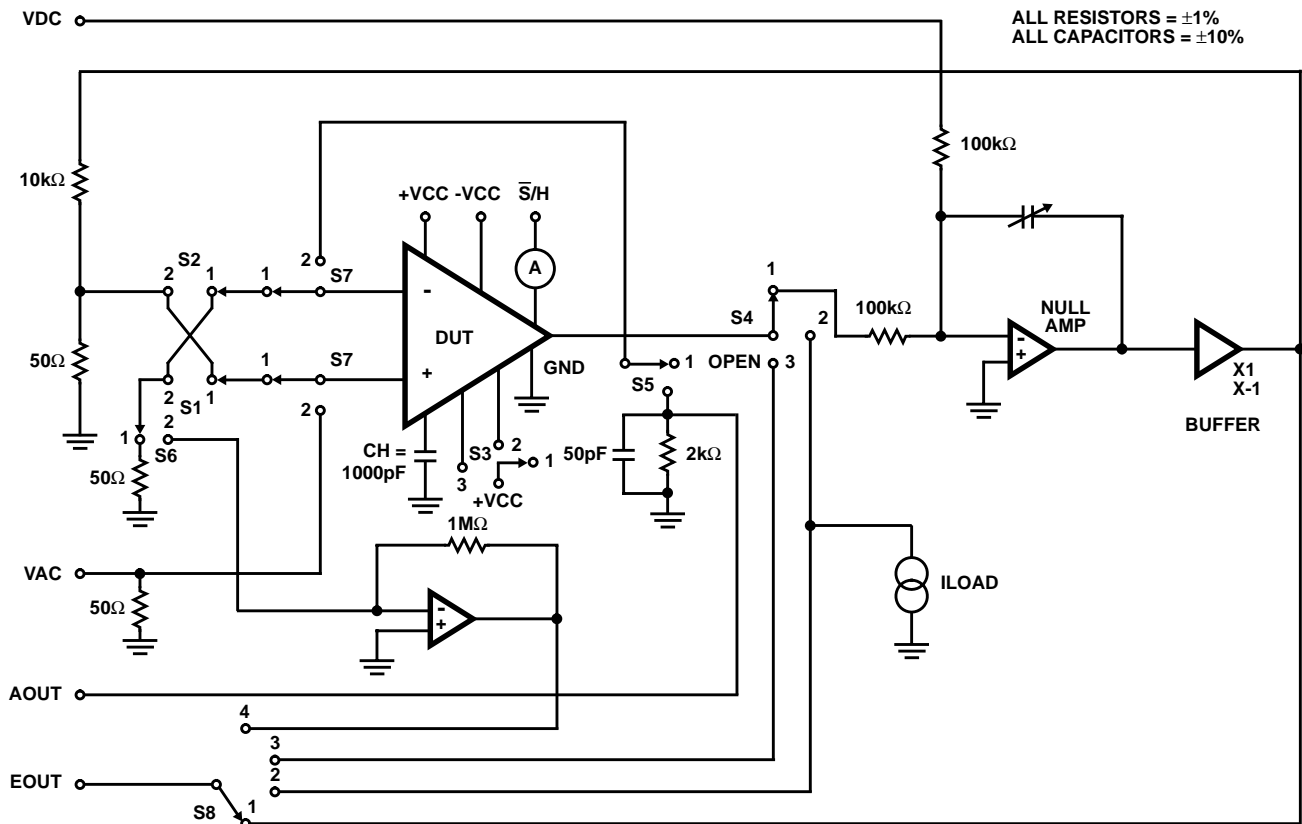
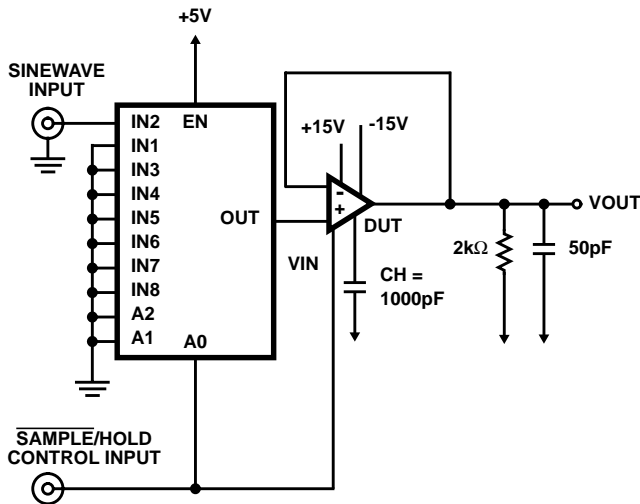


FIGURE 1. TEST FIXTURE SCHEMATIC (SWITCH POSITIONS S1 - S8 DETERMINE CONFIGURATION)

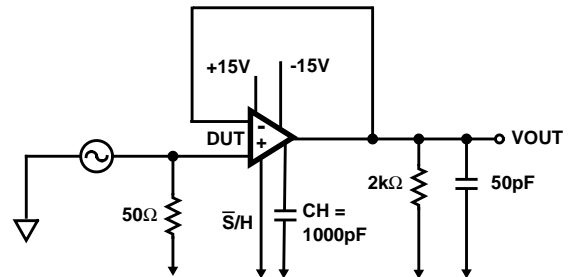


NOTE: Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{FeedthroughAttenuation} = 20 \log \left(\frac{\text{VOUT HOLD}}{\text{VIN HOLD}} \right)$$

Where VOUT HOLD = Peak-Peak Value of Output Sinewave during the Hold Mode.

FIGURE 2. HOLD MODE FEEDTHROUGH ATTENUATION

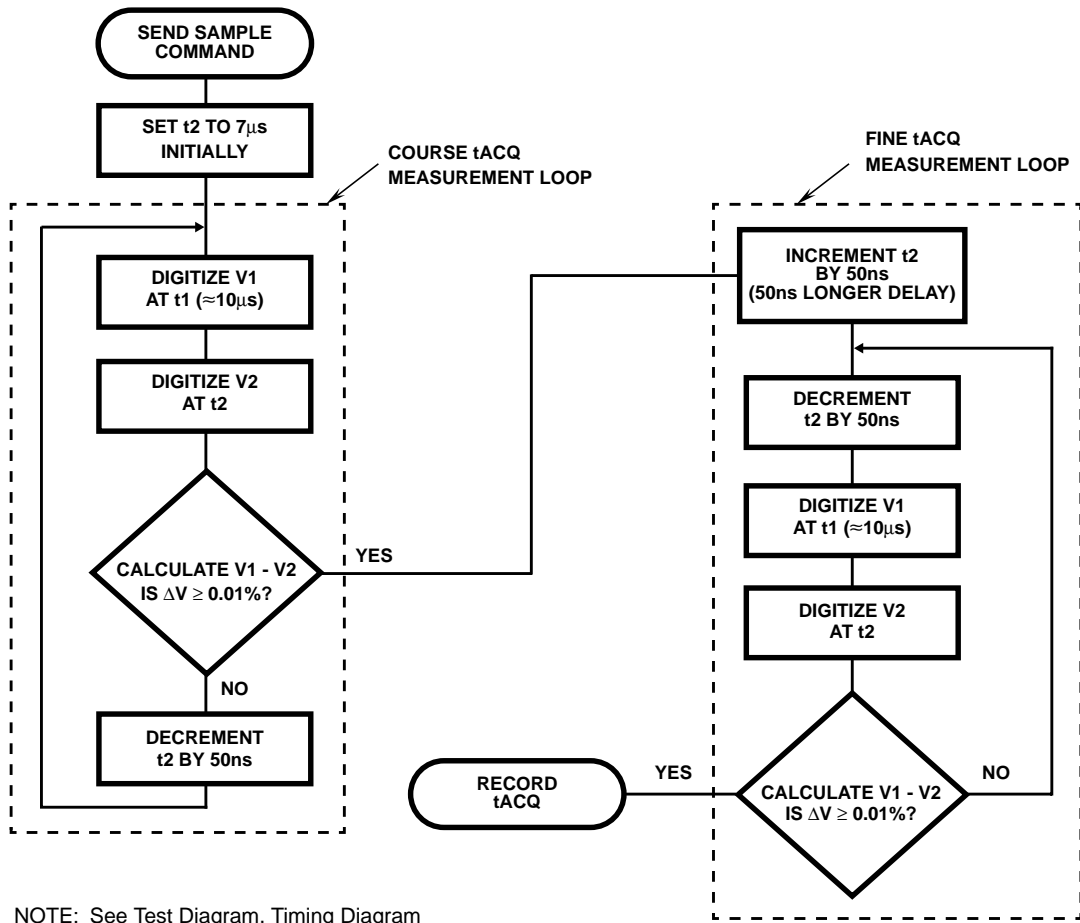


GBWP is the Frequency of VINPUT at which:

$$20 \log \left(\frac{\text{VOUT}}{\text{VINPUT}} \right) = -3\text{dB}$$

FIGURE 3. GAIN BANDWIDTH PRODUCT

Test Circuits (Continued)



NOTE: See Test Diagram, Timing Diagram

FIGURE 4. ACQUISITION TIME (tACQ TO 0.01% IS SHOWN, tACQ TO 0.1% IS DONE IN THE SAME MANNER)

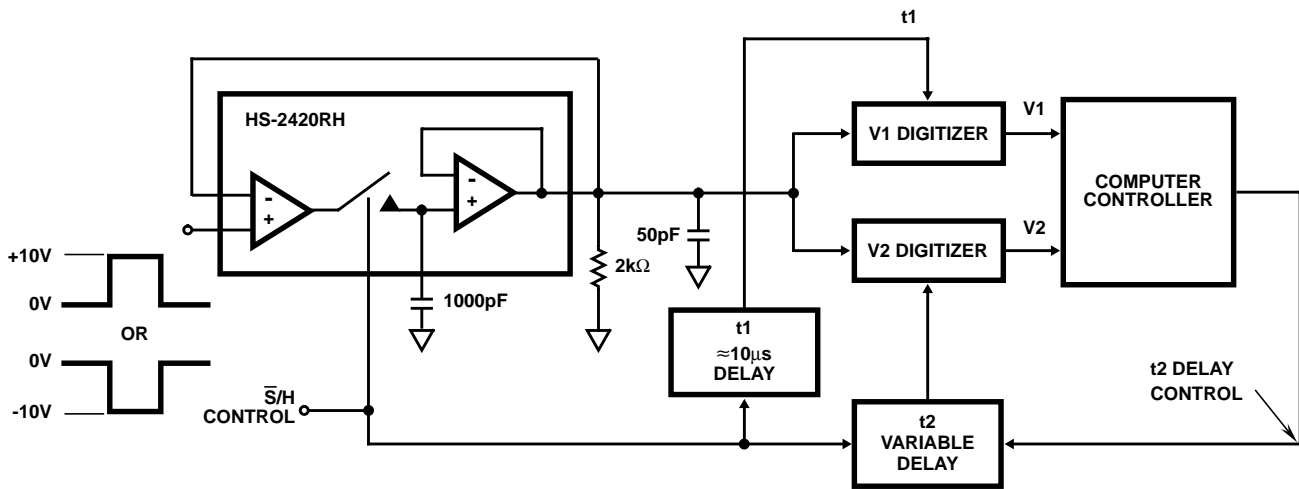


FIGURE 5

Timing Waveforms

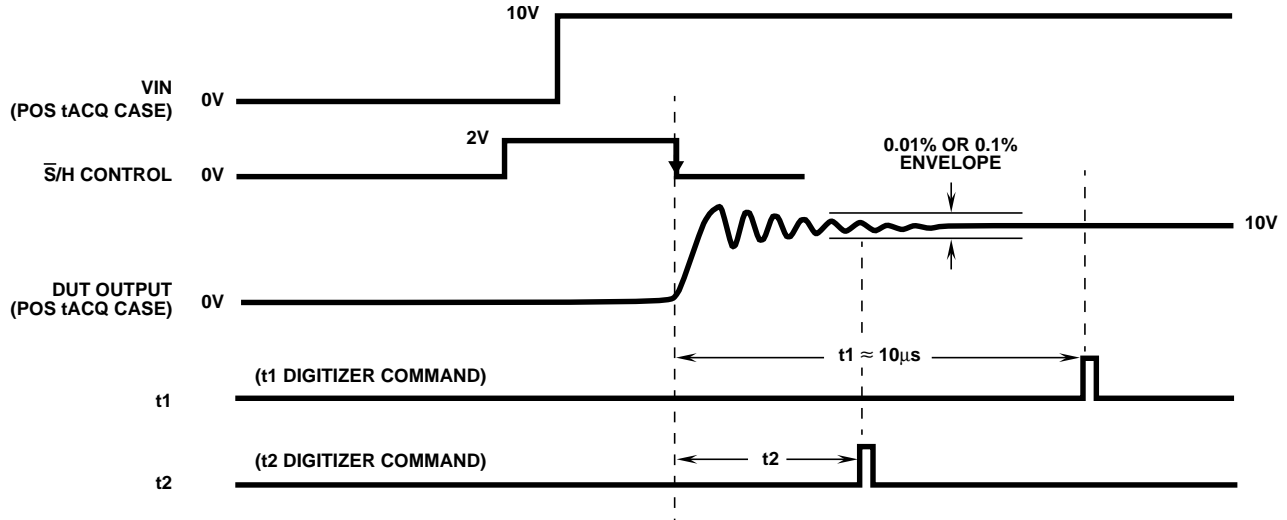


FIGURE 6. TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE tACQ CASE)

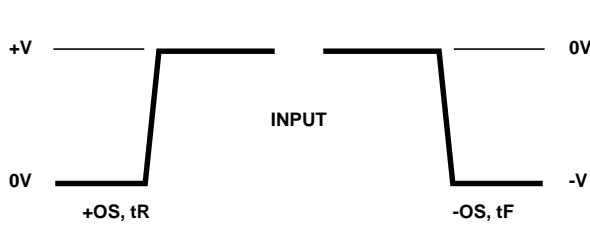


FIGURE 7A

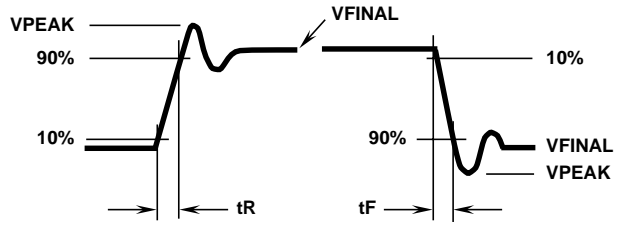


FIGURE 7B

FIGURE 7. OVERSHOOT, RISE AND FALL TIME WAVEFORMS

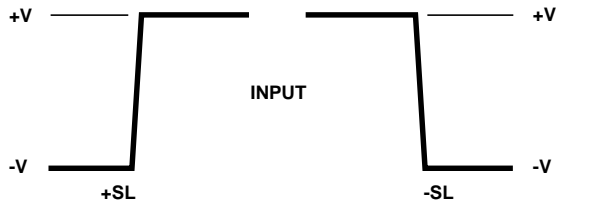


FIGURE 8A

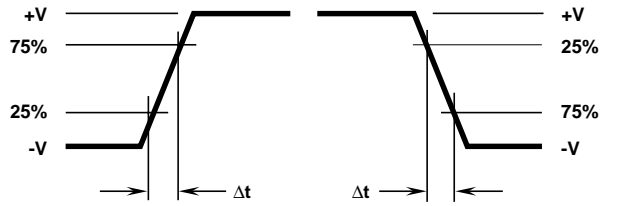


FIGURE 8B

FIGURE 8. SLEW RATE WAVEFORMS

Typical Performance Curves

VSUPPLY = ±15VDC, TA = +25°C, CH = 1000pF, Unless Otherwise Specified

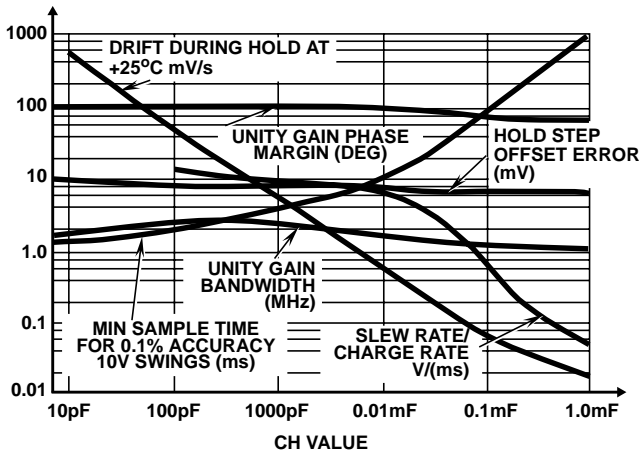


FIGURE 9. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR

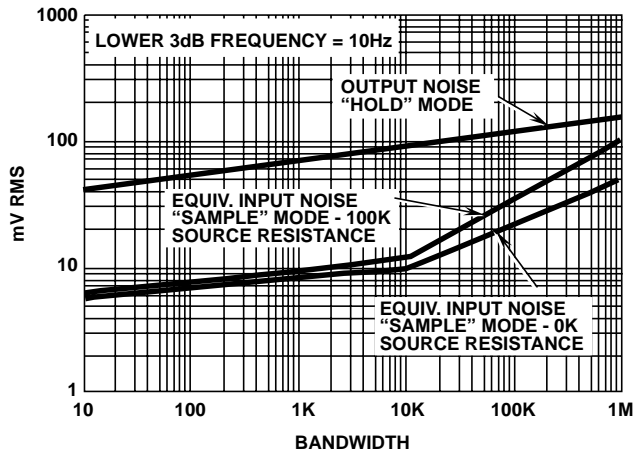


FIGURE 10. BROADBAND NOISE CHARACTERISTICS

HS-2420RH

Typical Performance Curves VSUPPLY = ±15VDC, TA = +25°C, CH = 1000pF, Unless Otherwise Specified (Continued)

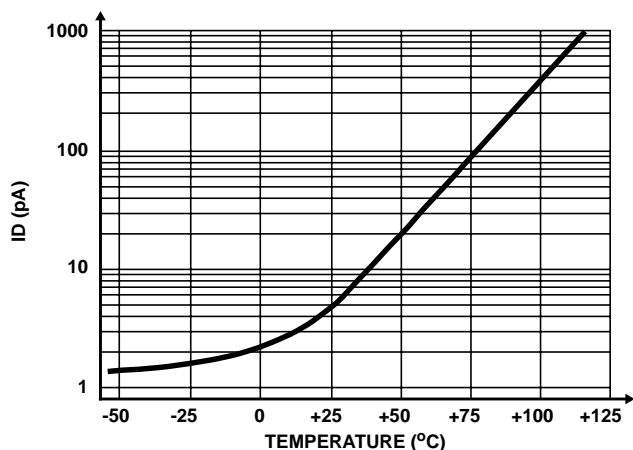


FIGURE 11. DRIFT CURRENT vs TEMPERATURE

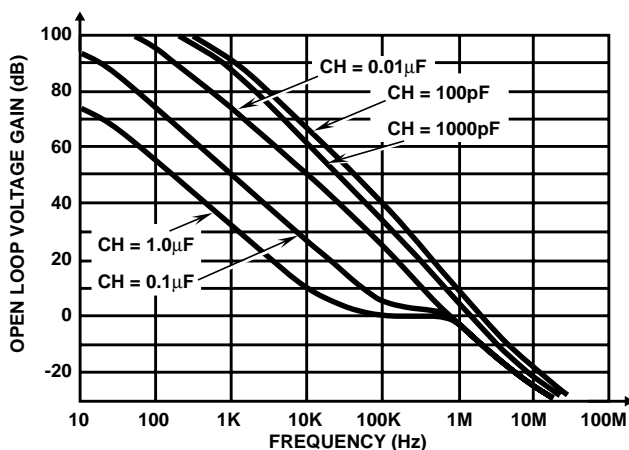


FIGURE 12. OPEN LOOP FREQUENCY RESPONSE

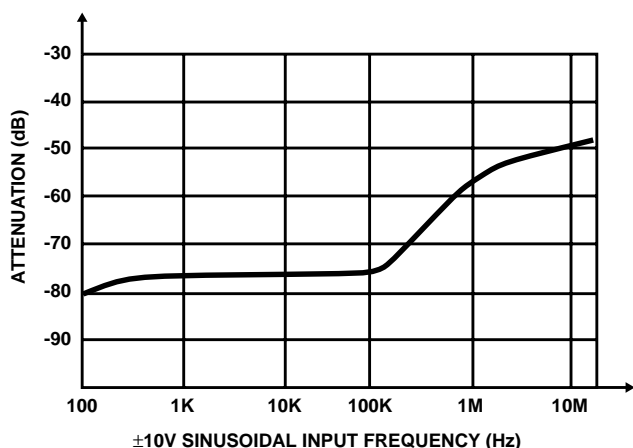


FIGURE 13. HOLD MODE FEEDTHROUGH ATTENUATION
CH = 1000pF

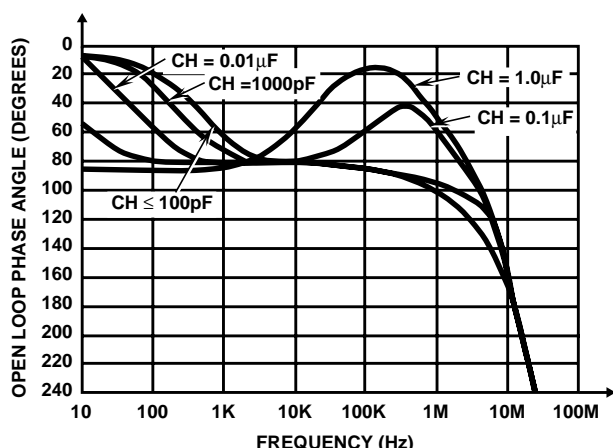
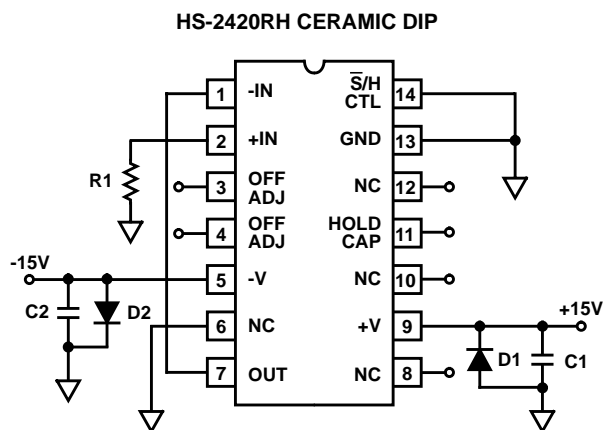


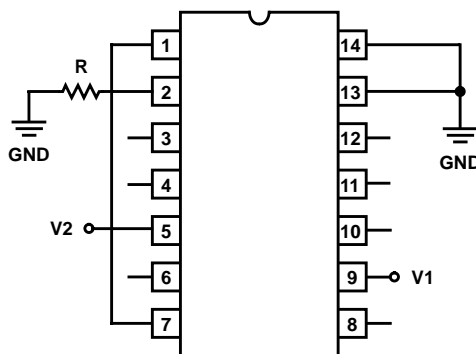
FIGURE 14. OPEN LOOP PHASE RESPONSE

Burn-In Circuit



NOTES:
R1 = 100kΩ ±5% (per socket)
C1 = C2 = 0.1µF (one per row) or 0.01µF (one per socket)
D1 = D2 = 1N4002 or equivalent (per board)

Irradiation Circuit



NOTES:
V1 = +15V
V2 = -15V
R = 100kΩ

HS-2420RH

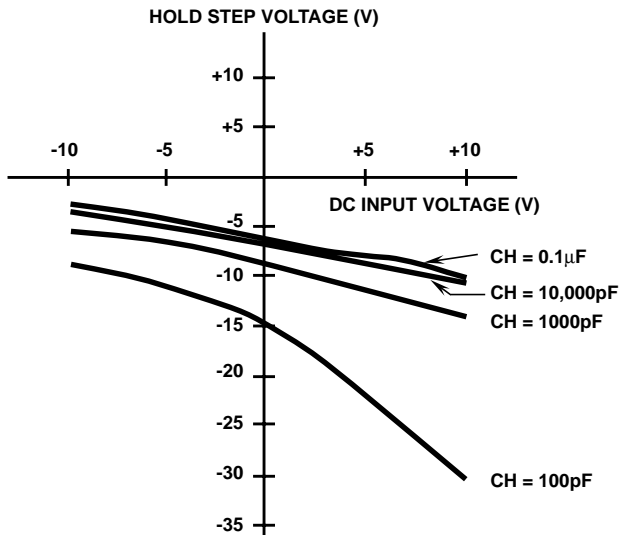


FIGURE 14. HOLD STEP vs INPUT VOLTAGE

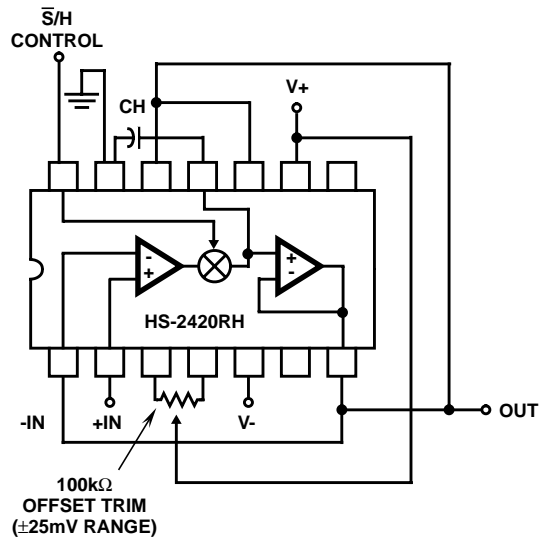


FIGURE 15. BASIC SAMPLE-AND-HOLD (TOP VIEW)

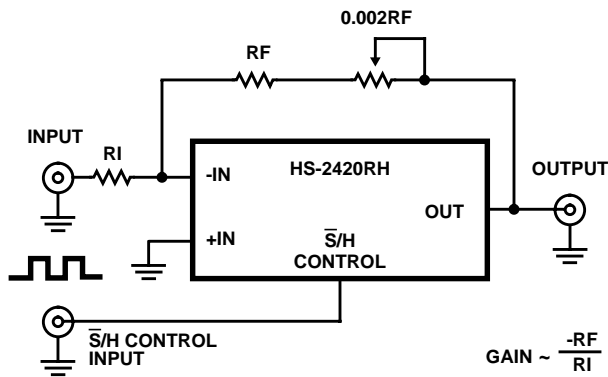


FIGURE 16. INVERTING CONFIGURATION

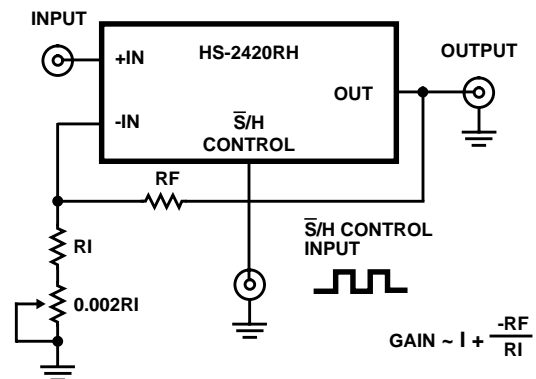


FIGURE 17. NONINVERTING CONFIGURATION

Offset and Gain Adjustment

Offset Adjustment

The offset voltage of the HS-2420RH may be adjusted using a 100kΩ trim pot, as shown in Figure 15. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the $\overline{S/H}$ control.
2. Adjust the trim pot for zero volts output in the hold mode.

Gain Adjustment

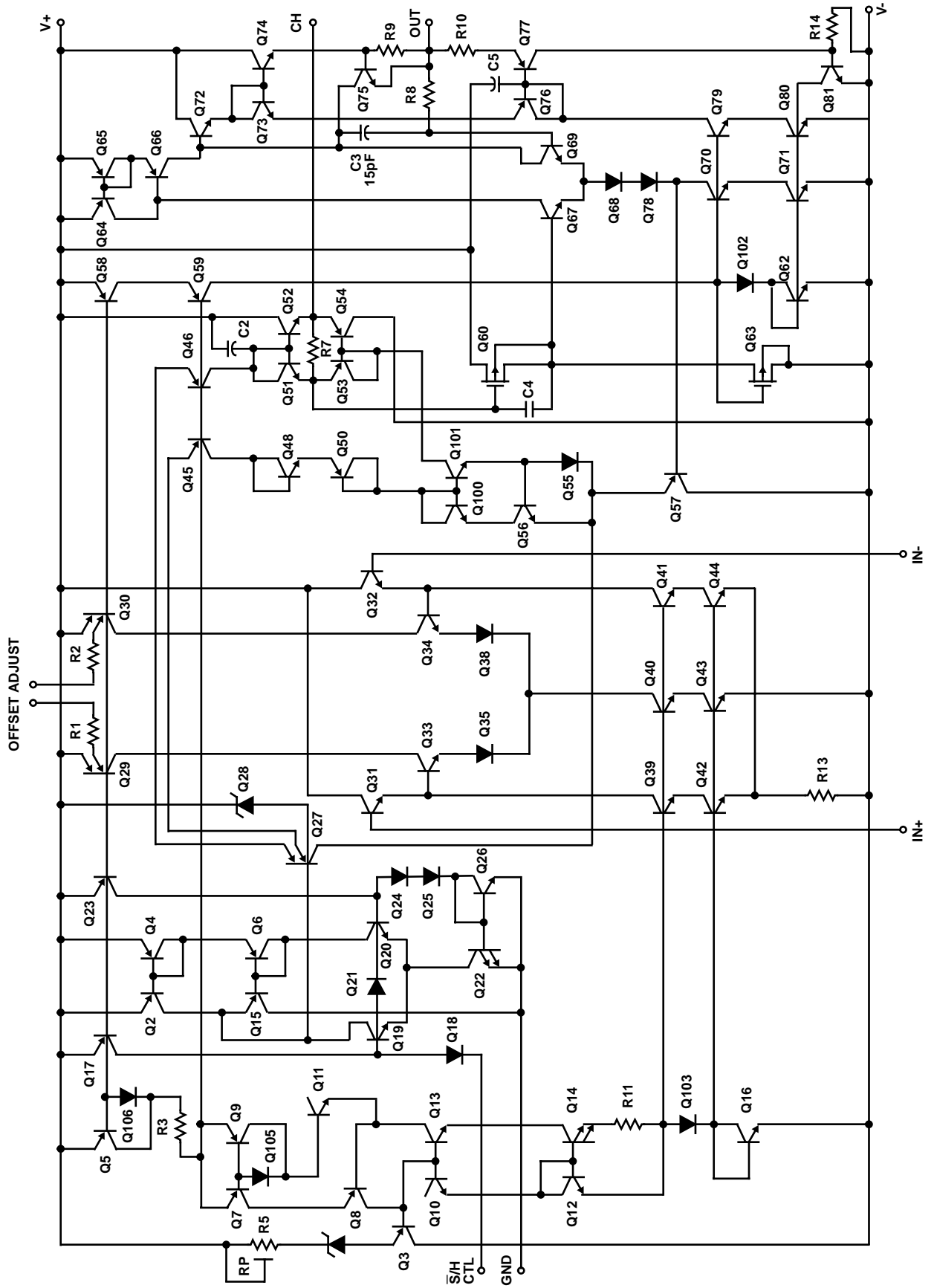
The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (CH = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage (V-10 NOMINAL). Adjust the trim pot for an output hold voltage of

$$\frac{(V-10 \text{ NOMINAL}) + (-10V)}{2}$$

Schematic



Intersil Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM) (Note 1)	100% Initial Electrical Test (T0)
GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Static Burn-In, Condition A, 240 Hours, +125°C or Equivalent, Method 1015
100% Die Attach	100% Interim Electrical Test 1 (T1)
100% Nondestructive Bond Pull, Method 2023	100% Delta Calculation (T0-T1)
Sample - Wire Bond Pull Monitor, Method 2011	100% PDA, Method 5004 (Note 2)
Sample - Die Shear Monitor, Method 2019 or 2027	100% Final Electrical Test
100% Internal Visual Inspection, Method 2010, Condition A	100% Fine/Gross Leak, Method 1014
CSI and/or GSI Pre-Cap (Note 7)	100% Radiographic (X-Ray), Method 2012 (Note 3)
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles	100% External Visual, Method 2009
100% Constant Acceleration, Method 2001, Condition per Method 5004	Sample - Group A, Method 5005 (Note 4)
100% PIND, Method 2020, Condition A	Sample - Group B, Method 5005 (Note 5)
100% External Visual	Sample - Group C, Method 5005 (Notes 5, 6)
100% Serialization	100% Data Package Generation (Note 8)
	CSI and/or GSI Final (Note 7)

NOTES:

1. Modified SEM Inspection, not compliant to MIL-STD-883, Method 2018. This device does not meet the Class S minimum metal step coverage of 50%. The metal does meet the current density requirement of $<2E^5A/cm^2$. Data provided upon request.
2. Failures from subgroup 1 and deltas are used for calculating PDA. The maximum allowable PDA = 5%.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B test, Group B samples, Group D test and Group D samples.
6. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D generic data. Generic data is not guaranteed to be available and is therefore not available in all cases.
7. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI Pre-Cap inspection, CSI Final Inspection, GSI Pre-Cap inspection, and/or GSI Final Inspection.
8. Data Package Contents:
Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
GAMMA Radiation Report. Contains Cover page, disposition, RAD Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
X-Ray report and film. Includes penetrometer measurements.
Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
Lot Serial Number Sheet (Good units serial number and lot number).
Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
Group B and D attributes and/or Generic data is included when required by the P.O.
The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

HS-2420RH

Metallization Topology

DIE DIMENSIONS:

97 mils x 61 mils x 19 mils

METALLIZATION:

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

GLASSIVATION:

Type: Silox

Thickness: $14\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

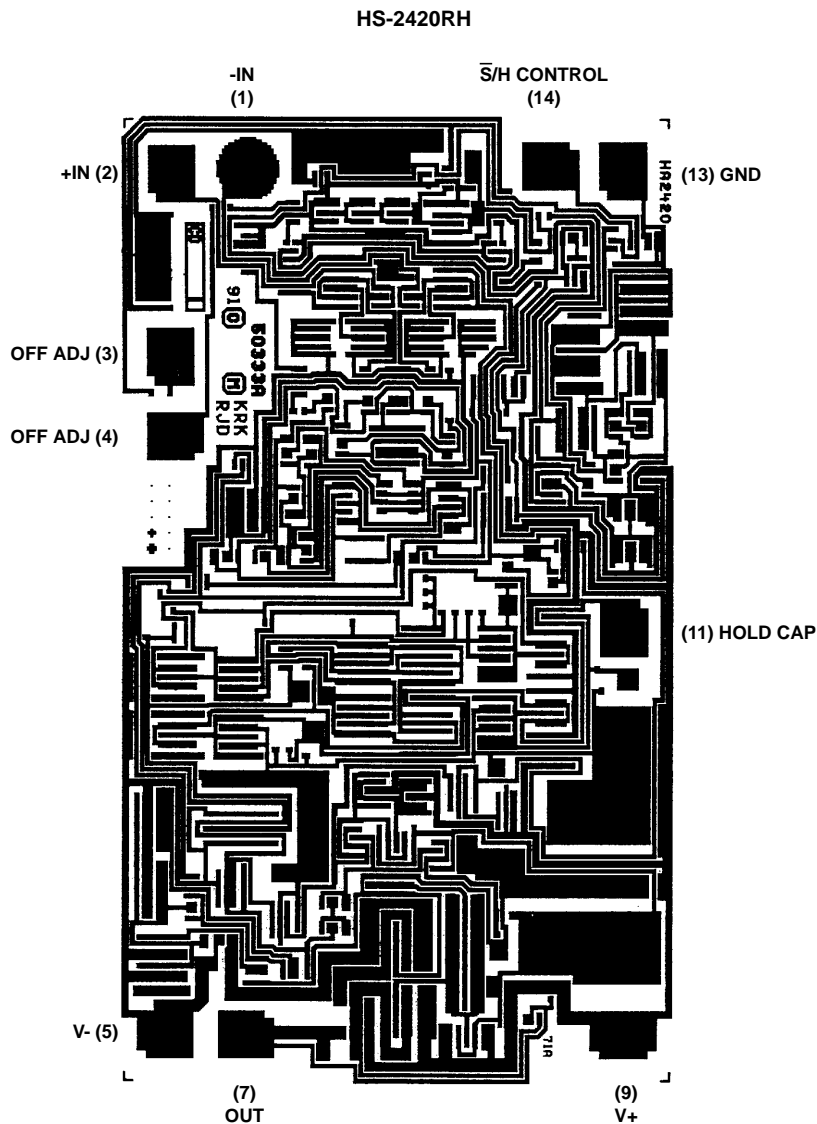
WORST CASE CURRENT DENSITY:

$2.0 \times 10^5 \text{A/cm}^2$

TRANSISTOR COUNT: 78

PROCESS: Bipolar-DI

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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