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# HM5118160B Series

1048576-word × 16-bit Dynamic Random Access Memory

# HITACHI

ADE-203-476 (Z)  
Preliminary  
Rev. 0.0  
Dec. 6, 1995

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## Description

The Hitachi HM5118160B is a CMOS dynamic RAM organized as 1,048,576-word × 16-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5118160B offers Fast Page Mode as a high speed access mode.

## Features

- Single 5 V ( $\pm 10\%$ )
- High speed
  - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 935 mW/825 mW/715 mW (max)
  - Standby mode: 11 mW (max)
    - : 0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - 1024 refresh cycles: 16 ms
    - : 128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)
- $2\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

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### Ordering Information

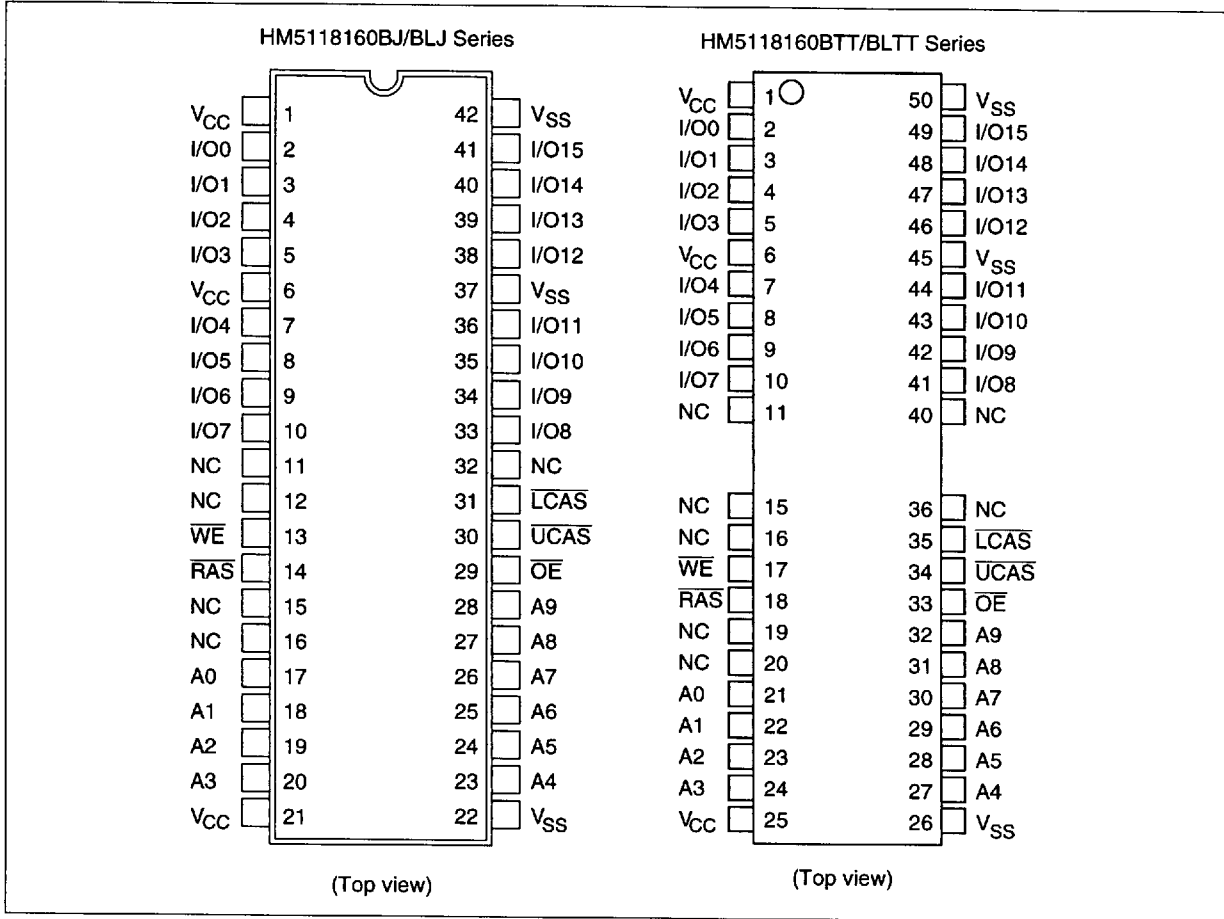
Type No.	Access time	Package
HM5118160BJ-6	60 ns	400-mil 42-pin plastic SOJ (CP-42D)
HM5118160BJ-7	70 ns	
HM5118160BJ-8	80 ns	
HM5118160BLJ-6	60 ns	
HM5118160BLJ-7	70 ns	
HM5118160BLJ-8	80 ns	
HM5118160BTT-6	60 ns	400-mil 50-pin plastic TSOP II (TTP-50/44DC)
HM5118160BTT-7	70 ns	
HM5118160BTT-8	80 ns	
HM5118160BLTT-6	60 ns	
HM5118160BLTT-7	70 ns	
HM5118160BLTT-8	80 ns	

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## Pin Arrangement

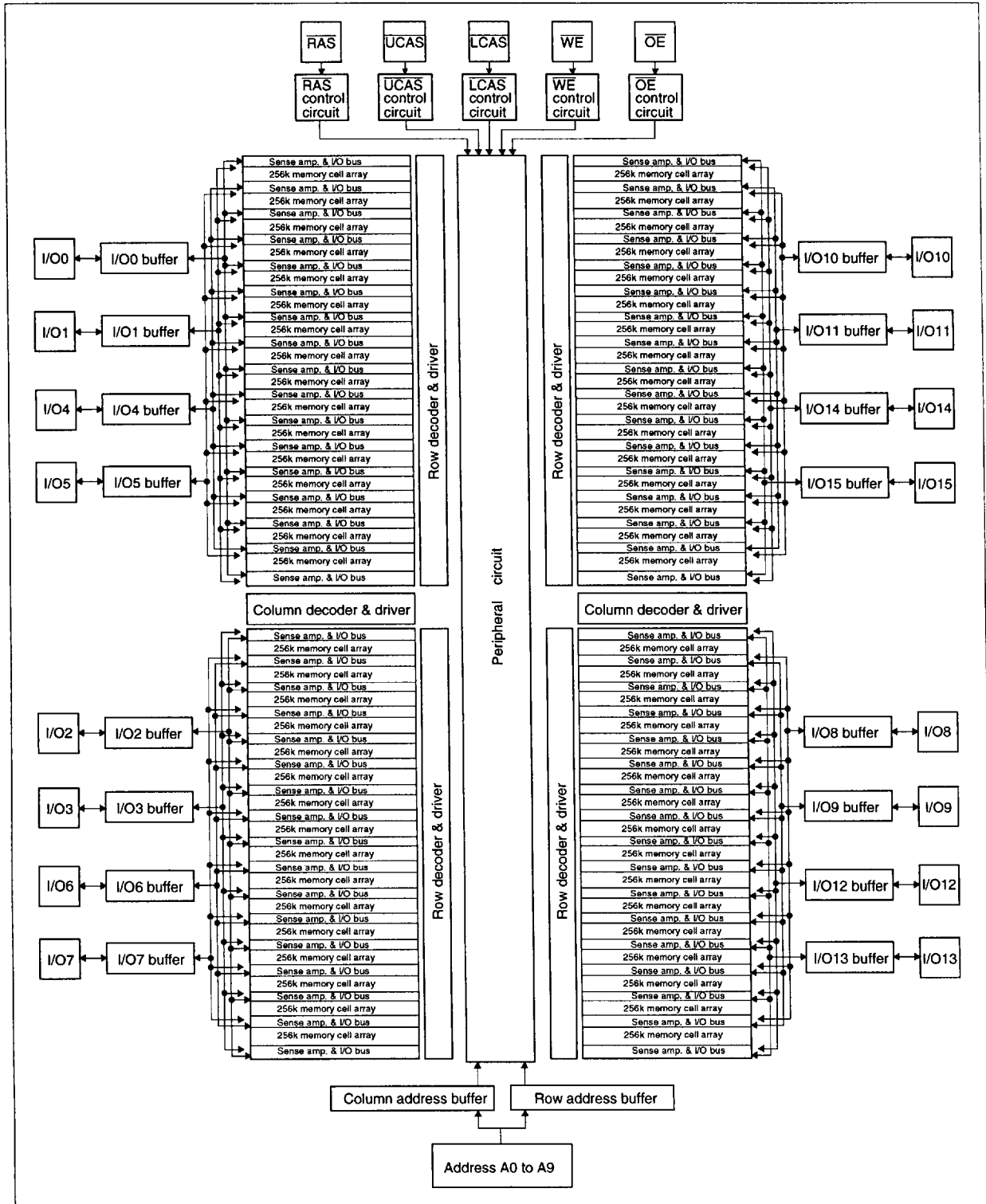


## Pin Description

Pin name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O0 to I/O15	Data input/Data output
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/Write enable
OE	Output enable
V <sub>CC</sub>	Power supply (+5 V)
V <sub>SS</sub>	Ground
NC	No connection

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## Block Diagram



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### Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output		Operation
H	D	D	D	D	Open		Standby
L	L	H	H	L	Valid	Lower byte	Read cycle
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L <sup>2</sup>	D	Open	Lower byte	Early write cycle
L	H	L	L <sup>2</sup>	D	Open	Upper byte	
L	L	L	L <sup>2</sup>	D	Open	Word	
L	L	H	L <sup>2</sup>	H	Undefined	Lower byte	Delayed write cycle
L	H	L	L <sup>2</sup>	H	Undefined	Upper byte	
L	L	L	L <sup>2</sup>	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
L	H	H	D	D	Open	Word	$\overline{\text{RAS}}$ -only refresh cycle
H to L	H	L	D	D	Open	Word	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or Self refresh cycle (L-version)
H to L	L	H	D	D	Open	Word	
H to L	L	L	D	D	Open	Word	
L	L	L	H	H	Open		Read cycle (Output disabled)

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2.  $t_{\text{WCS}} \geq 0$  ns Early write cycle

$t_{\text{WCS}} < 0$  ns Delayed write cycle

3. Mode is determined by the OR function of the  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ . (Mode is set by the earliest of  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  active edge and reset by the latest of  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  inactive edge.) However write OPERATION and output HIZ control are done independently by each  $\overline{\text{UCAS}}$ ,  $\overline{\text{LCAS}}$ .

ex. if  $\overline{\text{RAS}} = \text{H to L}$ ,  $\overline{\text{UCAS}} = \text{H}$ ,  $\overline{\text{LCAS}} = \text{L}$ , then  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle is selected.

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	1, 2
Input high voltage	$V_{IH}$	2.4	—	6.5	V	1
Input low voltage	$V_{IL}$	-1.0	—	0.8	V	1

Notes: 1. All voltage referred to  $V_{SS}$

2. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

### DC Characteristics ( $T_a = 0$ to +70°C, $V_{CC} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ )

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current <sup>1,2</sup>	$I_{CC1}$	—	170	—	150	—	130	mA	$t_{RC} = \min$
Standby current	$I_{CC2}$	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}, \overline{UCAS}, \overline{LCAS} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}, \overline{UCAS}, \overline{LCAS} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	150	—	150	—	150	$\mu\text{A}$	CMOS interface $\overline{RAS}, \overline{UCAS}, \overline{LCAS} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z
$\overline{RAS}$ -only refresh current <sup>2</sup>	$I_{CC3}$	—	170	—	150	—	130	mA	$t_{RC} = \min$

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DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V) (cont)

Parameter	Symbol	HM5118160B						Unit	Test conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Standby current <sup>1</sup>	I <sub>CC5</sub>	—	5	—	5	—	5	mA	$\overline{RAS} = V_{IH}$ $\overline{UCAS}, \overline{LCAS} = V_{IL}$ Dout = enable
CAS-before- $\overline{RAS}$ refresh current	I <sub>CC6</sub>	—	170	—	150	—	130	mA	t <sub>RC</sub> = min
Fast page mode current <sup>1, *3</sup>	I <sub>CC7</sub>	—	170	—	150	—	130	mA	t <sub>PC</sub> = min
Battery backup current <sup>4</sup> (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	500	—	500	—	500	μA	CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 31.3 μs t <sub>RAS</sub> ≤ 0.3 μs
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	300	—	300	—	300	μA	CMOS interface $\overline{RAS}, \overline{UCAS}, \overline{LCAS} \leq 0.2 V$ Dout = High-Z
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -5 mA
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 V$ ,  $0 V \leq V_{IL} \leq 0.2 V$ .

Capacitance (Ta = 25°C, V<sub>CC</sub> = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C <sub>I1</sub>	—	5	pF	1
Input capacitance (Clocks)	C <sub>I2</sub>	—	7	pF	1
Output capacitance (Data-in, Data-out)	C <sub>VO</sub>	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$  to disable Dout.

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AC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )\*<sup>1, \*2, \*18</sup>

### Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	$t_{RC}$	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	15	10000	18	10000	20	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	21
Column address hold time	$t_{CAH}$	10	—	15	—	15	—	ns	21
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	20	45	20	52	20	60	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	15	30	15	35	15	40	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	60	—	70	—	80	—	ns	23
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	—	5	—	5	—	ns	22
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	15	—	18	—	20	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7

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## HM5118160B Series

### Read Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	18	—	20	ns	9, 10, 17
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	15	—	18	—	20	ns	9, 25
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	12, 22
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	5	—	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	30	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	18	—	20	—	ns	5

### Write Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	14, 21
Write command hold time	$t_{\text{WCH}}$	10	—	15	—	15	—	ns	21
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	18	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	18	—	20	—	ns	23
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	15, 23
Data-in hold time	$t_{\text{DH}}$	10	—	15	—	15	—	ns	15, 23

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### Read-Modify-Write Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	155	—	181	—	205	—	ns	
RAS to $\overline{WE}$ delay time	$t_{RWD}$	85	—	98	—	110	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	15	—	18	—	20	—	ns	

### Refresh Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	5	—	ns	21
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	10	—	ns	22
RAS precharge to $\overline{CAS}$ hold time	$t_{RPC}$	0	—	0	—	0	—	ns	21

### Fast Page Mode Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	$t_{PC}$	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	—	40	—	45	ns	9, 17, 22
RAS hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM5118160B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	$t_{PRWC}$	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	60	—	68	—	75	—	ns	14, 22

Refresh



Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	16	ms	1024 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	1024 cycles

Self Refresh Mode (L-version)

		HM5118160BL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (Self refresh)	$t_{RASS}$	100	—	100	—	100	—	$\mu$ s	26
$\overline{RAS}$ precharge time (Self refresh)	$t_{RPS}$	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (Self refresh)	$t_{CHS}$	-50	—	-50	—	-50	—	ns	

- Notes:
1. AC measurements assume  $t_T = 5$  ns.
  2. An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{RAS}$ -only refresh or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh).
  3. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
  4. Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
  5. Either  $t_{OED}$  or  $t_{CDD}$  must be satisfied.
  6. Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
  7.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  8. Assumes that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  9. Measured with a load circuit equivalent to 2 TTL loads and 100 pF. ( $V_{OH} = 2.4$  V,  $V_{OL} = 0.4$  V)
  10. Assumes that  $t_{RCD} \geq t_{RCD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\geq t_{RAD} + t_{AA}$  (max).
  11. Assumes that  $t_{RAD} \geq t_{RAD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\leq t_{RAD} + t_{AA}$  (max).

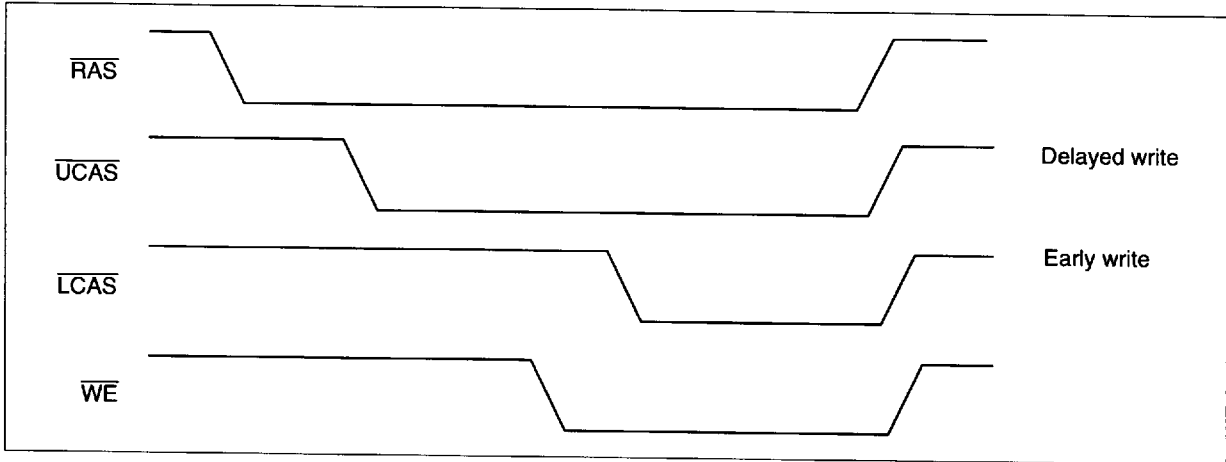
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12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
13.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ , and  $t_{AWD} \geq t_{AWD}(\text{min})$ , or  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to  $\overline{UCAS}$  and  $\overline{LCAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in delayed write or read-modify-write cycles.
16.  $t_{RASP}$  defines  $\overline{RAS}$  pulse width in fast page mode cycles.
17. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$ .
18. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device. After  $\overline{RAS}$  is reset, if  $t_{OEH} \geq t_{CWL}$ , the I/O pin will remain open circuit (high impedance); if  $t_{OEH} < t_{CWL}$ , invalid data will be out at each I/O.
19. When both  $\overline{UCAS}$  and  $\overline{LCAS}$  go low at the same time, all 16-bit data are written into the device.  $\overline{UCAS}$  and  $\overline{LCAS}$  cannot be staggered within the same write/read cycles.
20. All the  $V_{CC}$  and  $V_{SS}$  pins shall be supplied with the same voltages.
21.  $t_{ASC}$ ,  $t_{CAH}$ ,  $t_{RCS}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{CSR}$  and  $t_{RPC}$  are determined by the earlier falling edge of  $\overline{UCAS}$  or  $\overline{LCAS}$ .
22.  $t_{CRP}$ ,  $t_{CHR}$ ,  $t_{RCH}$ ,  $t_{CPA}$  and  $t_{CPW}$  are determined by the later rising edge of  $\overline{UCAS}$  or  $\overline{LCAS}$ .
23.  $t_{CWL}$ ,  $t_{DH}$  and  $t_{DS}$  should be satisfied by both  $\overline{UCAS}$  and  $\overline{LCAS}$ .
24.  $t_{CP}$  is determined by the time that both  $\overline{UCAS}$  and  $\overline{LCAS}$  are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH} \text{ min}/V_{IL} \text{ max}$  level.
26. Please do not use  $t_{RASS}$  timing,  $10 \mu\text{s} \leq t_{RASS} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100 \mu\text{s}$ , then  $\overline{RAS}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
27. If you use distributed CBR refresh mode with  $15.6 \mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6 \mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
28. If you use  $\overline{RAS}$  only refresh or CBR burst refresh mode in normal read/write cycle, 1024cycles of distributed CBR refresh with  $15.6 \mu\text{s}$  interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
30.  H or L (H:  $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$ , L:  $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$ )  
 Invalid Dout

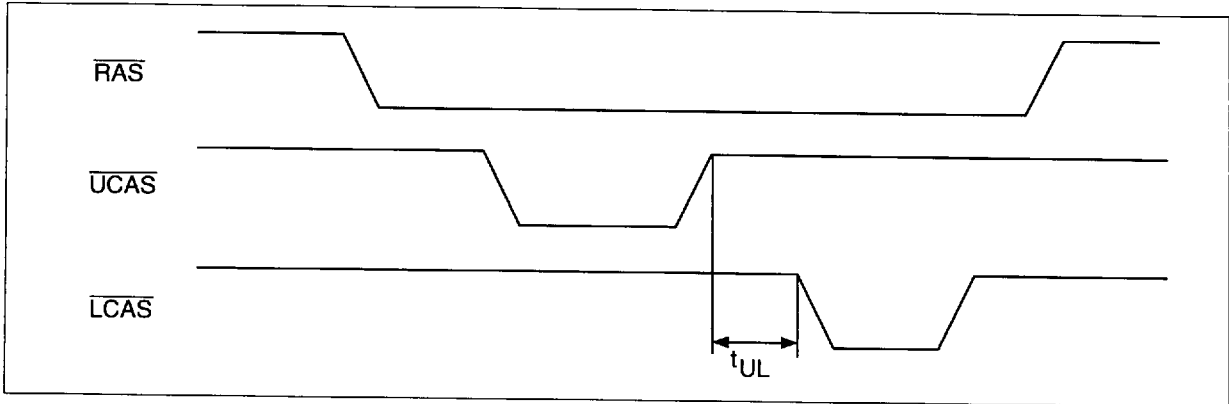
**Notes concerning  $\overline{2CAS}$  control**

Please do not separate the  $\overline{UCAS/LCAS}$  operation timing intentionally. However skew between  $\overline{UCAS/LCAS}$  are allowed under the following conditions.

1. Each of the  $\overline{UCAS/LCAS}$  should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied, fast page mode can be performed.

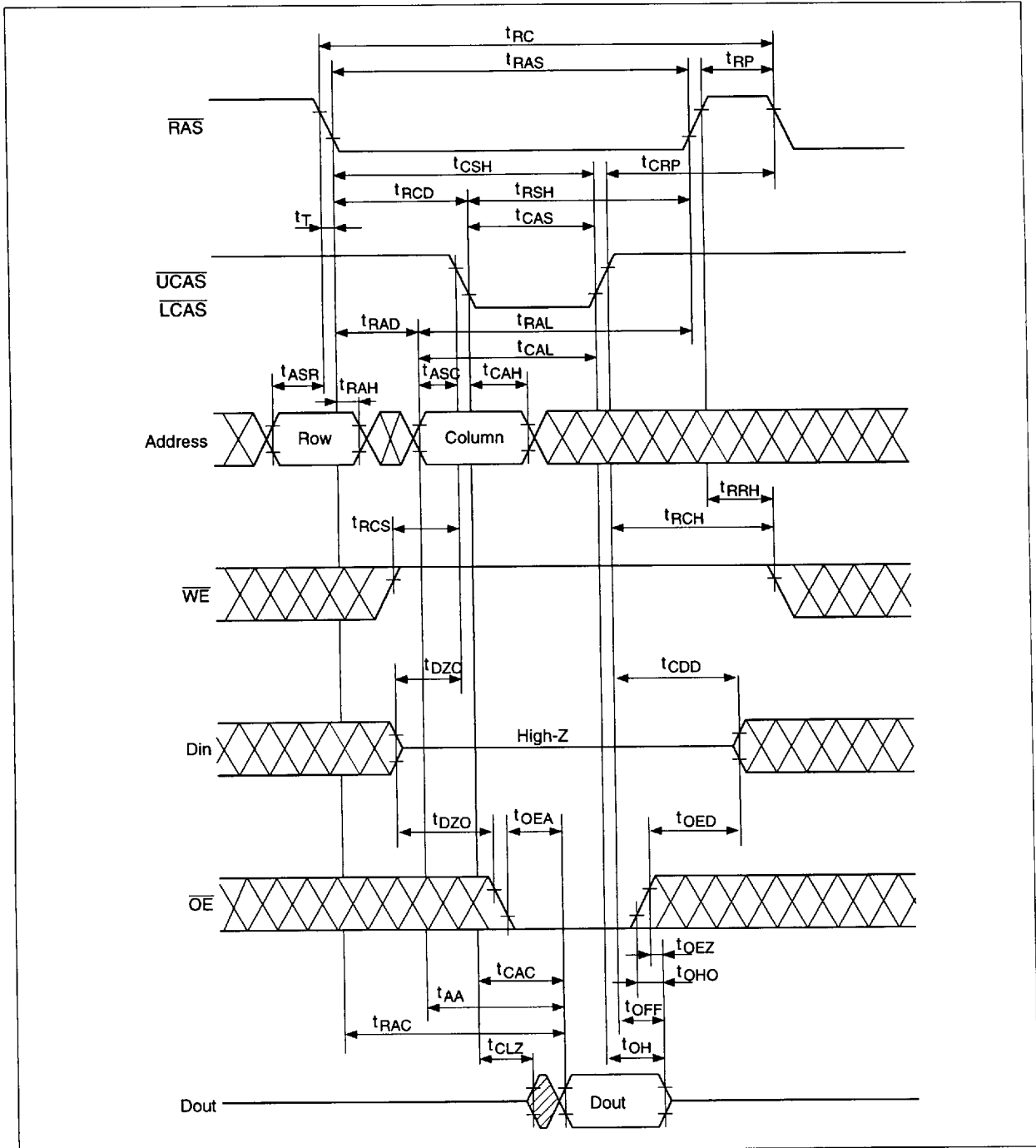


4. Byte control operation by remainnig  $\overline{UCAS}$  or  $\overline{LCAS}$  high is guaranteed

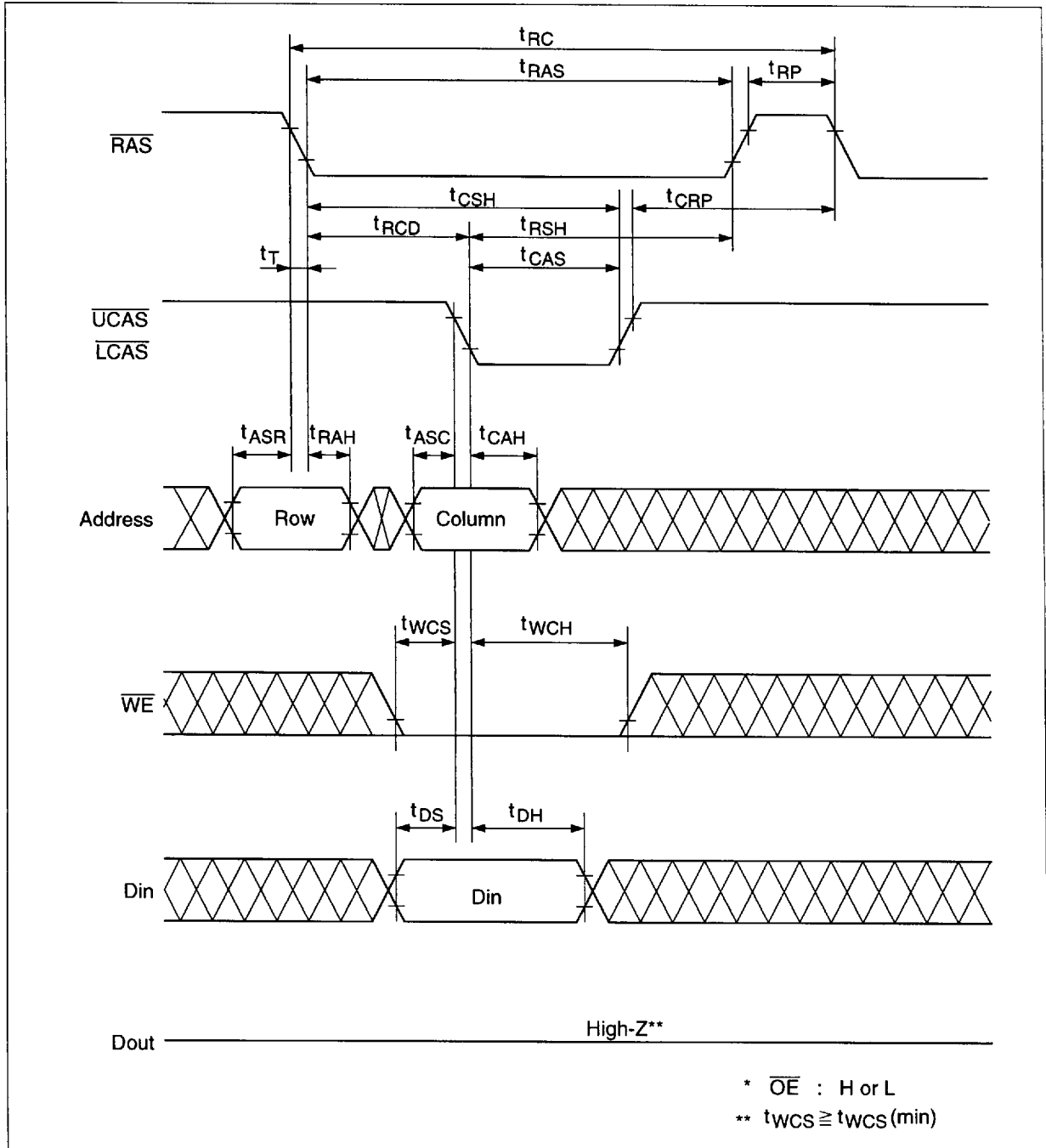
# HM5118160B Series

## Timing Waveforms\*30

### Read Cycle

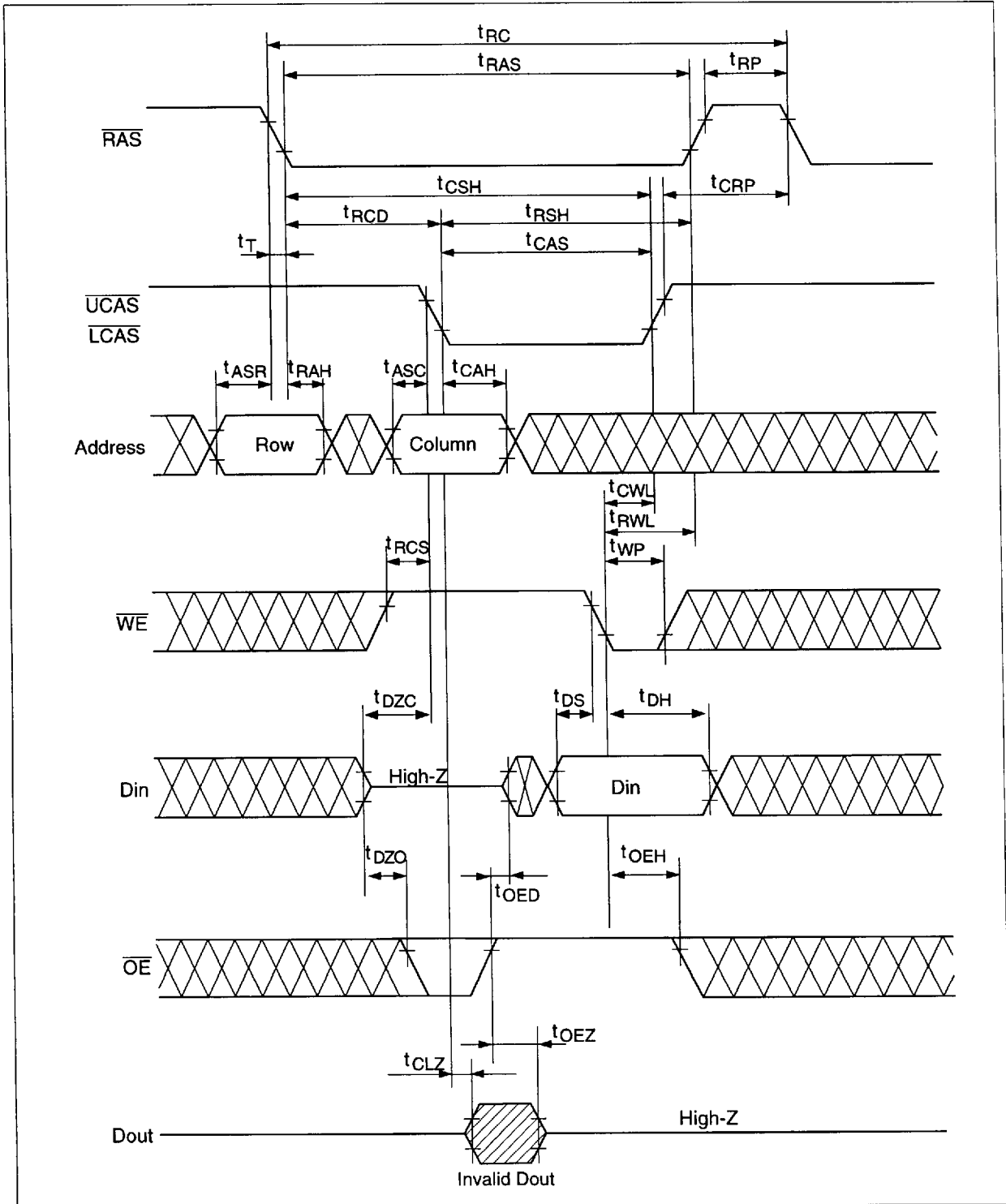


Early Write Cycle



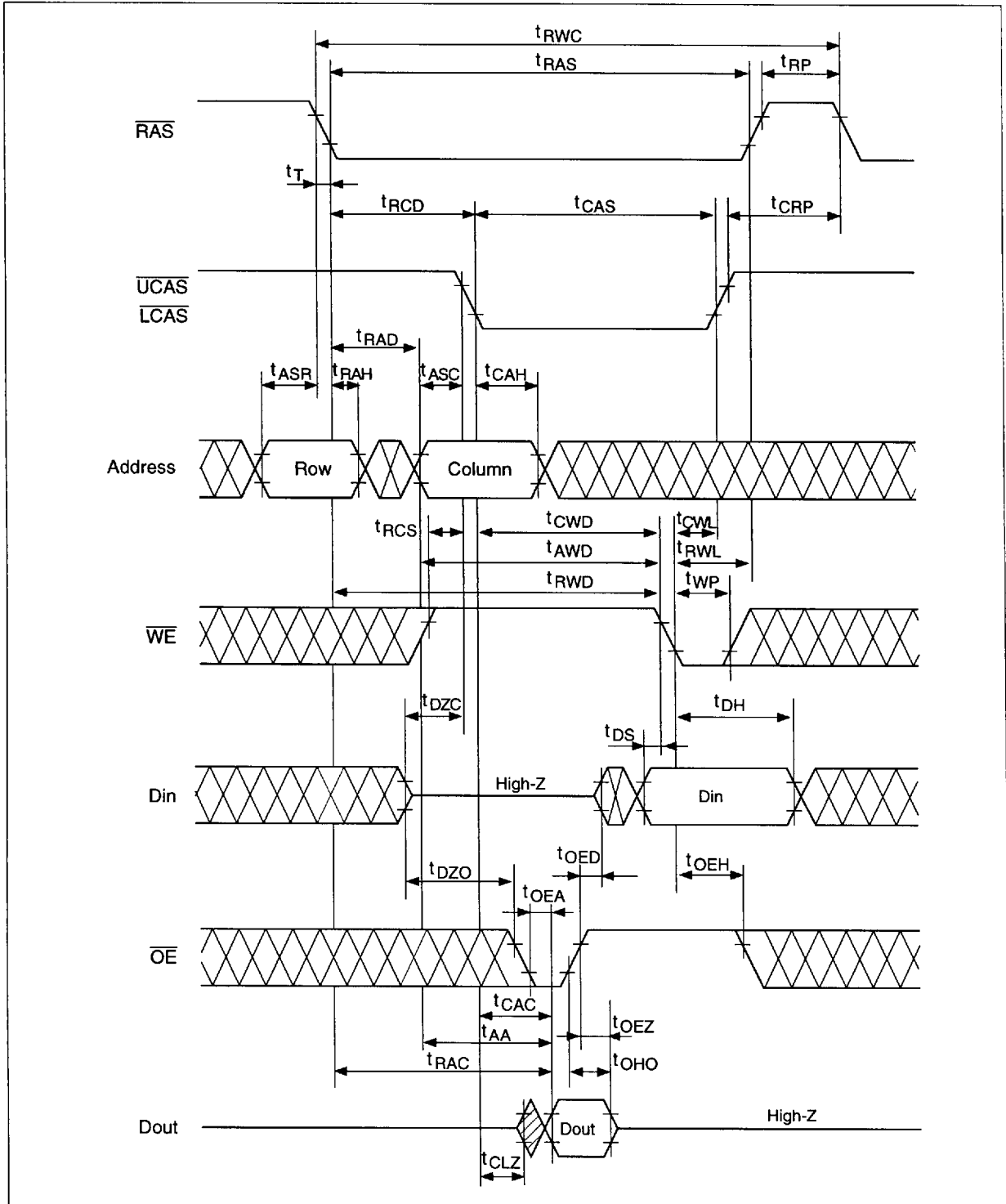
# HM5118160B Series

## Delayed Write Cycle<sup>\*18</sup>



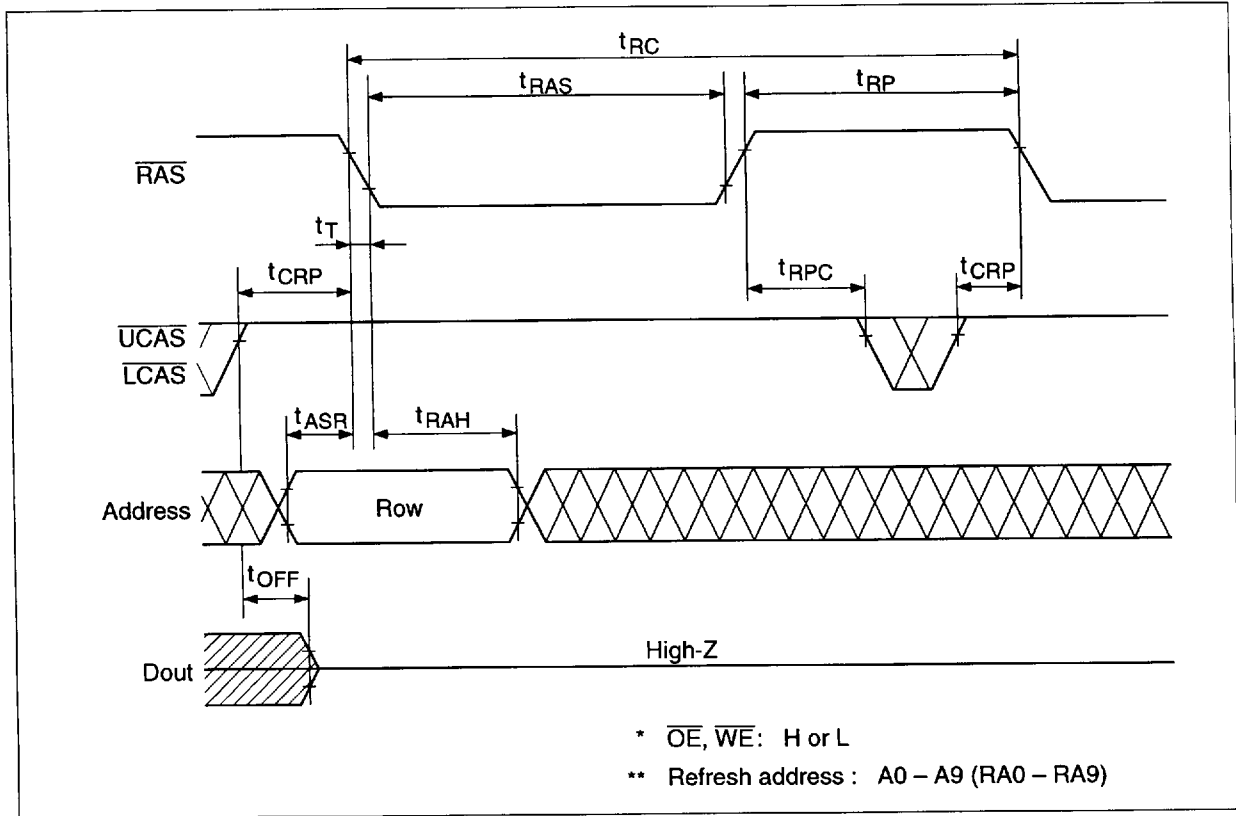


Read-Modify-Write Cycle<sup>\*18</sup>

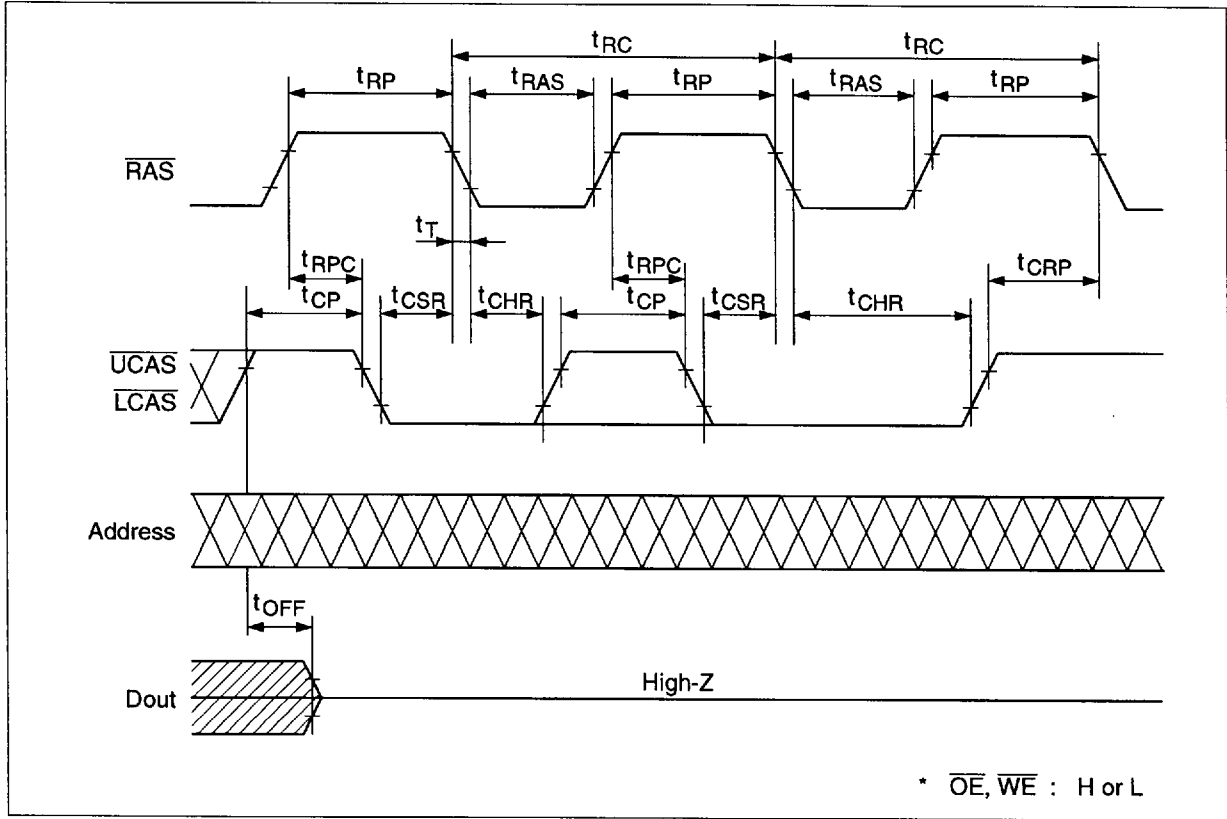


# HM5118160B Series

## RAS-Only Refresh Cycle

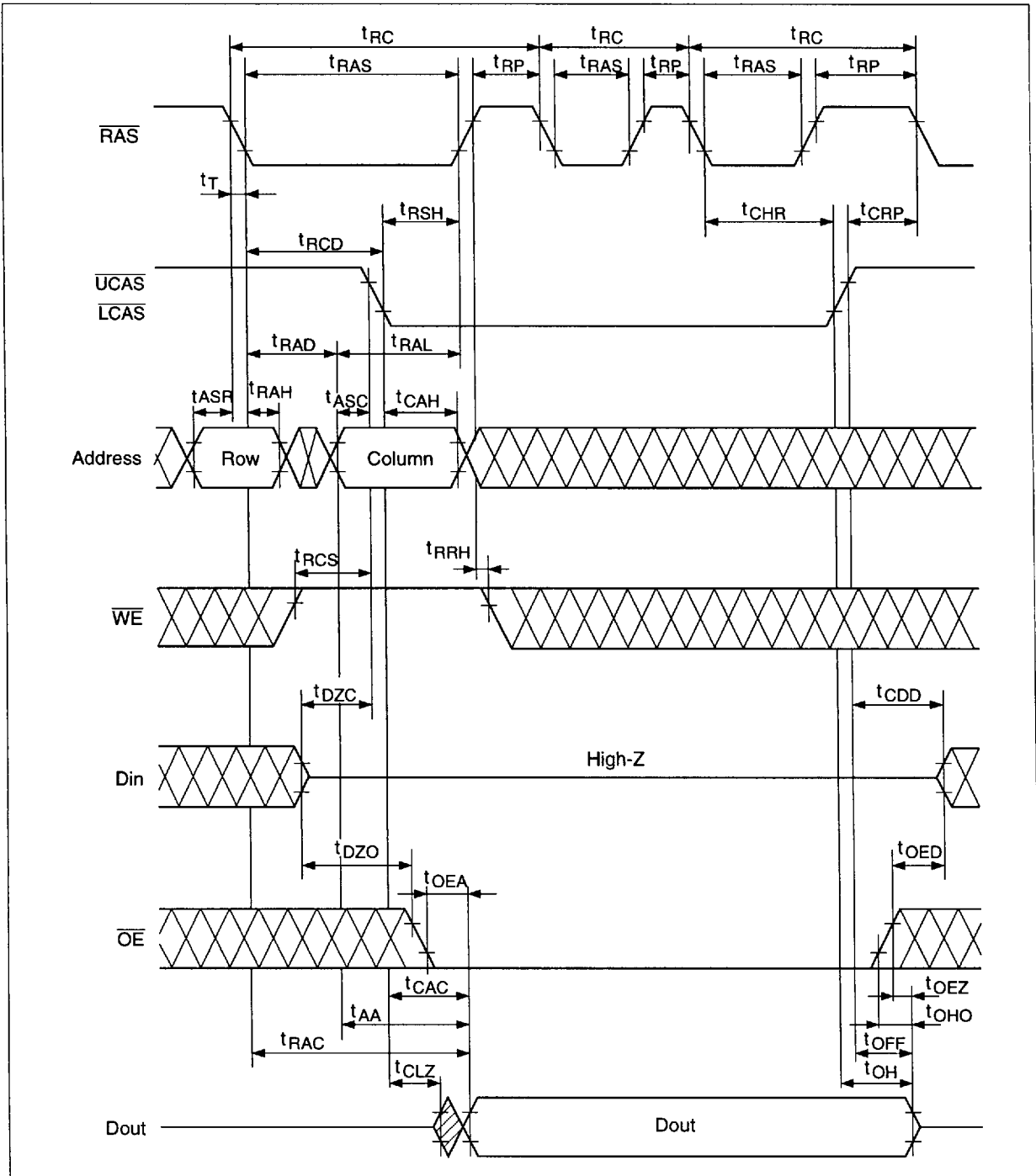


$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Cycle

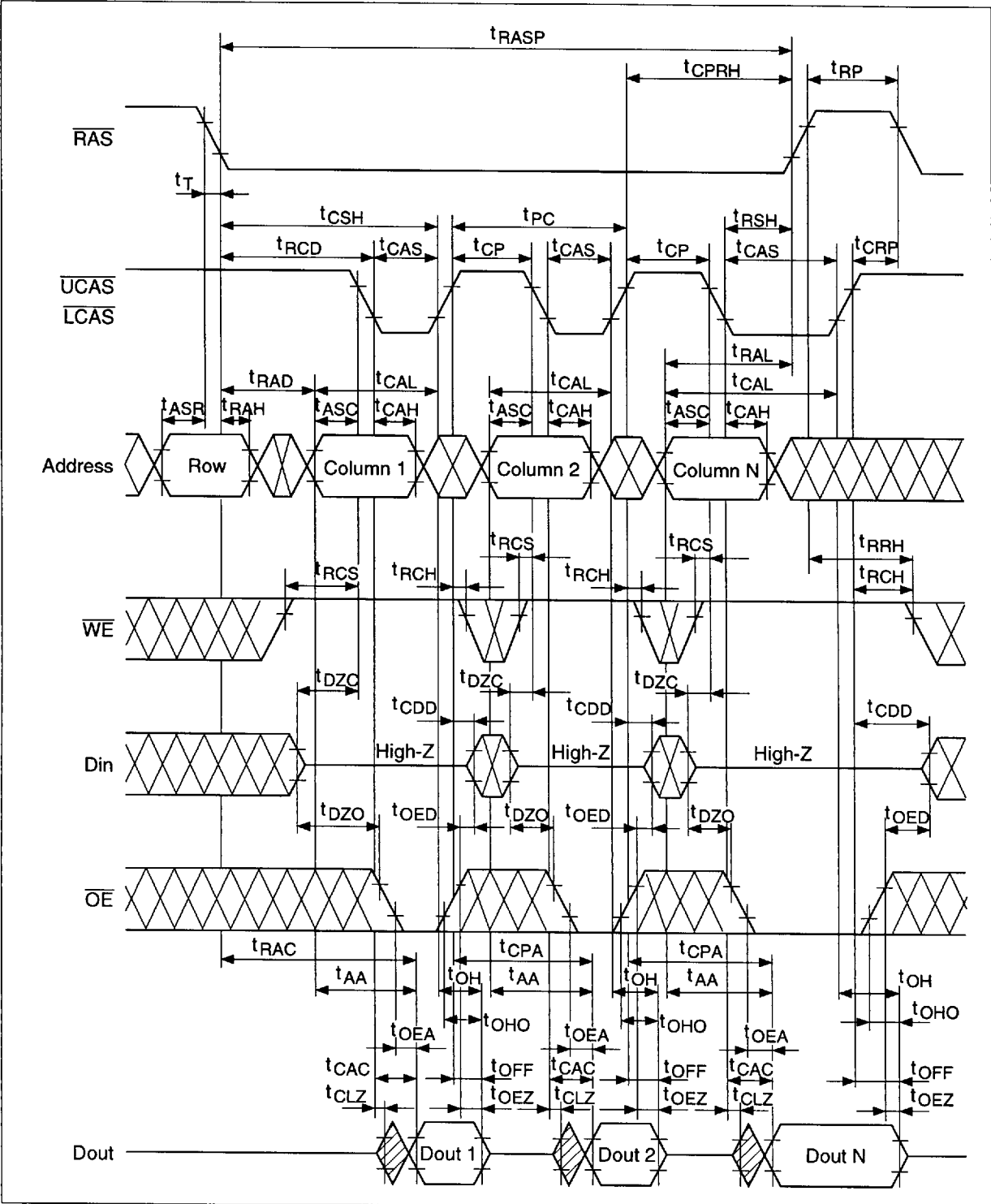


# HM5118160B Series

## Hidden Refresh Cycle

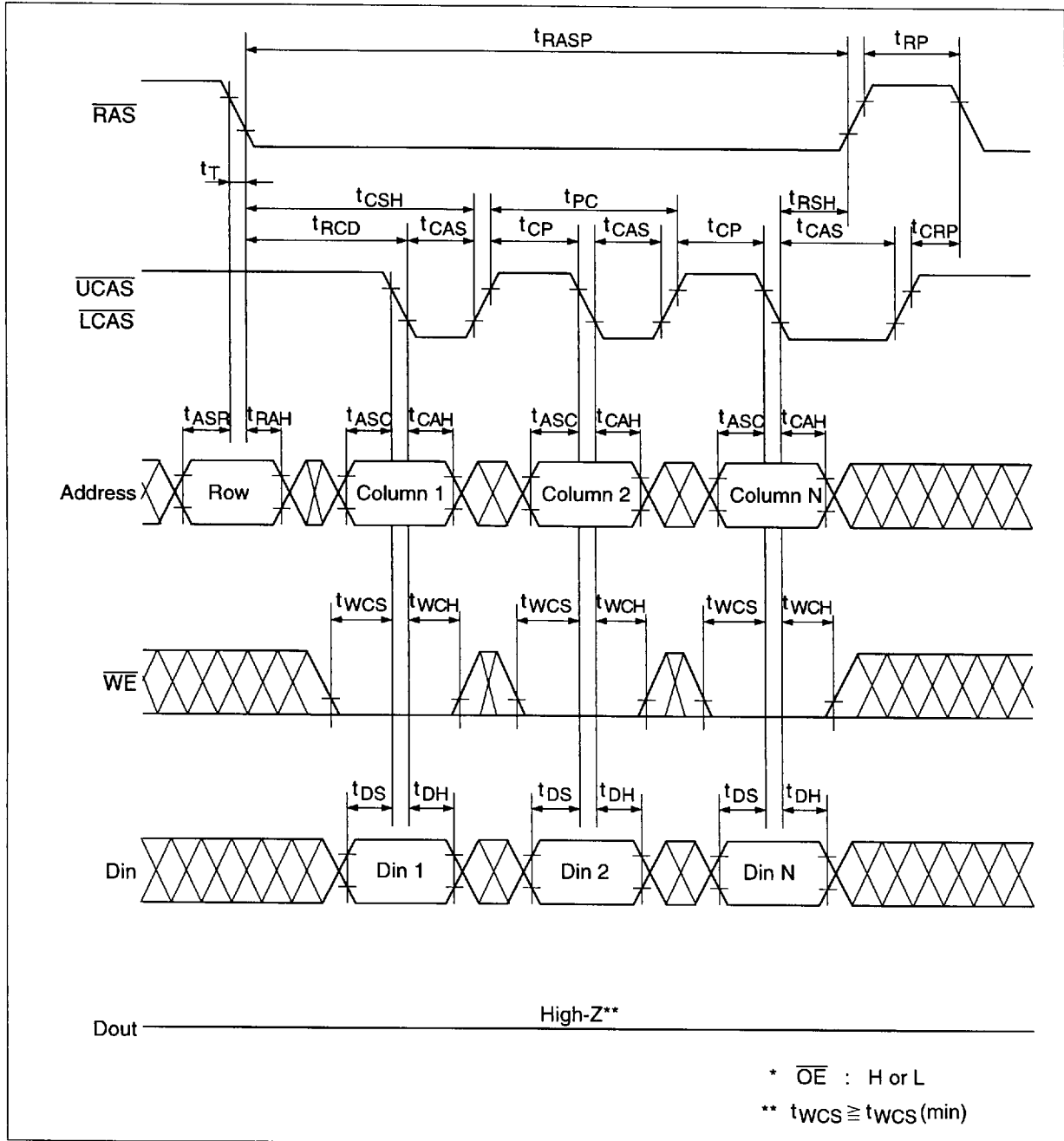


Fast Page Mode Read Cycle

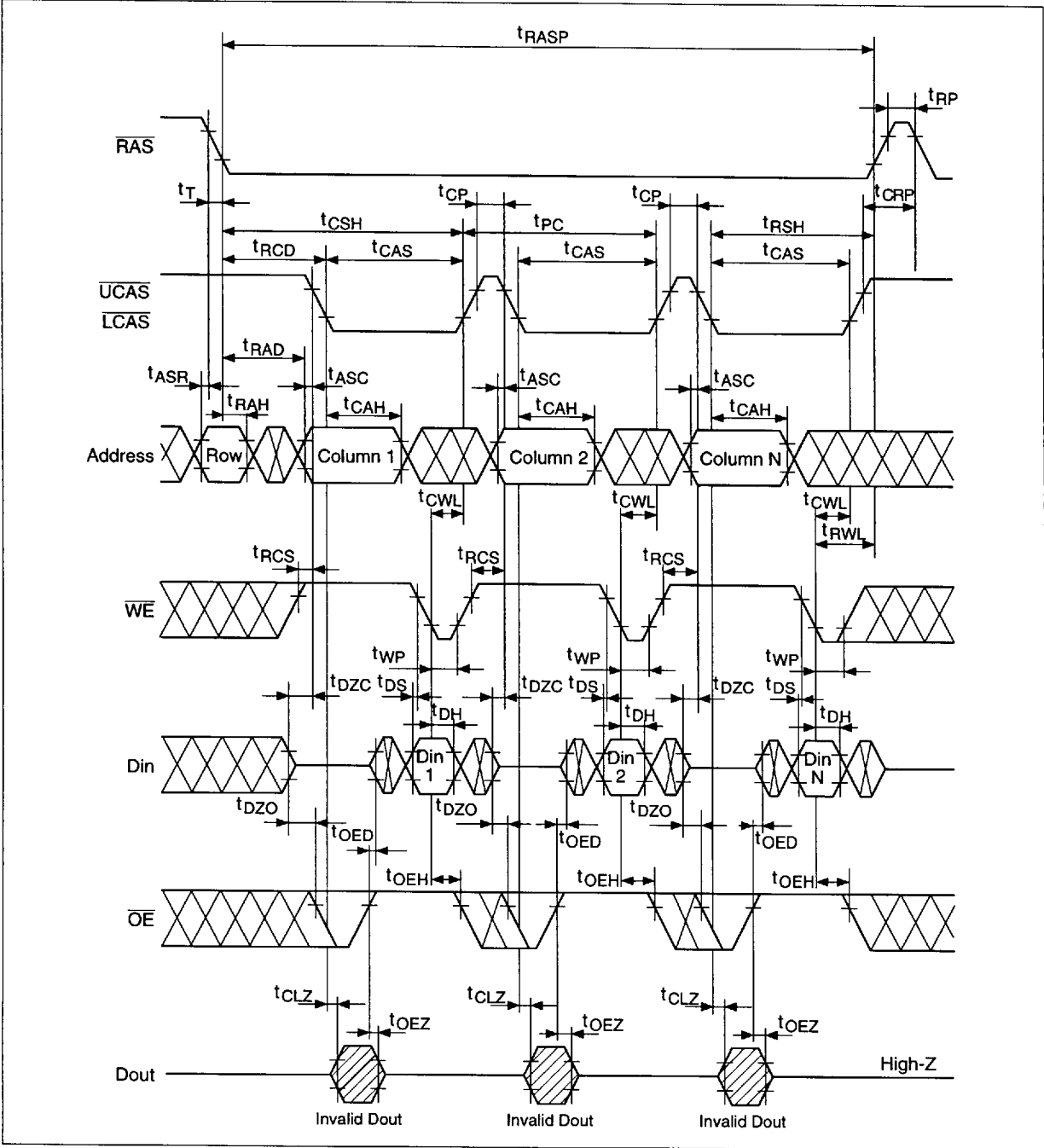


# HM5118160B Series

## Fast Page Mode Early Write Cycle

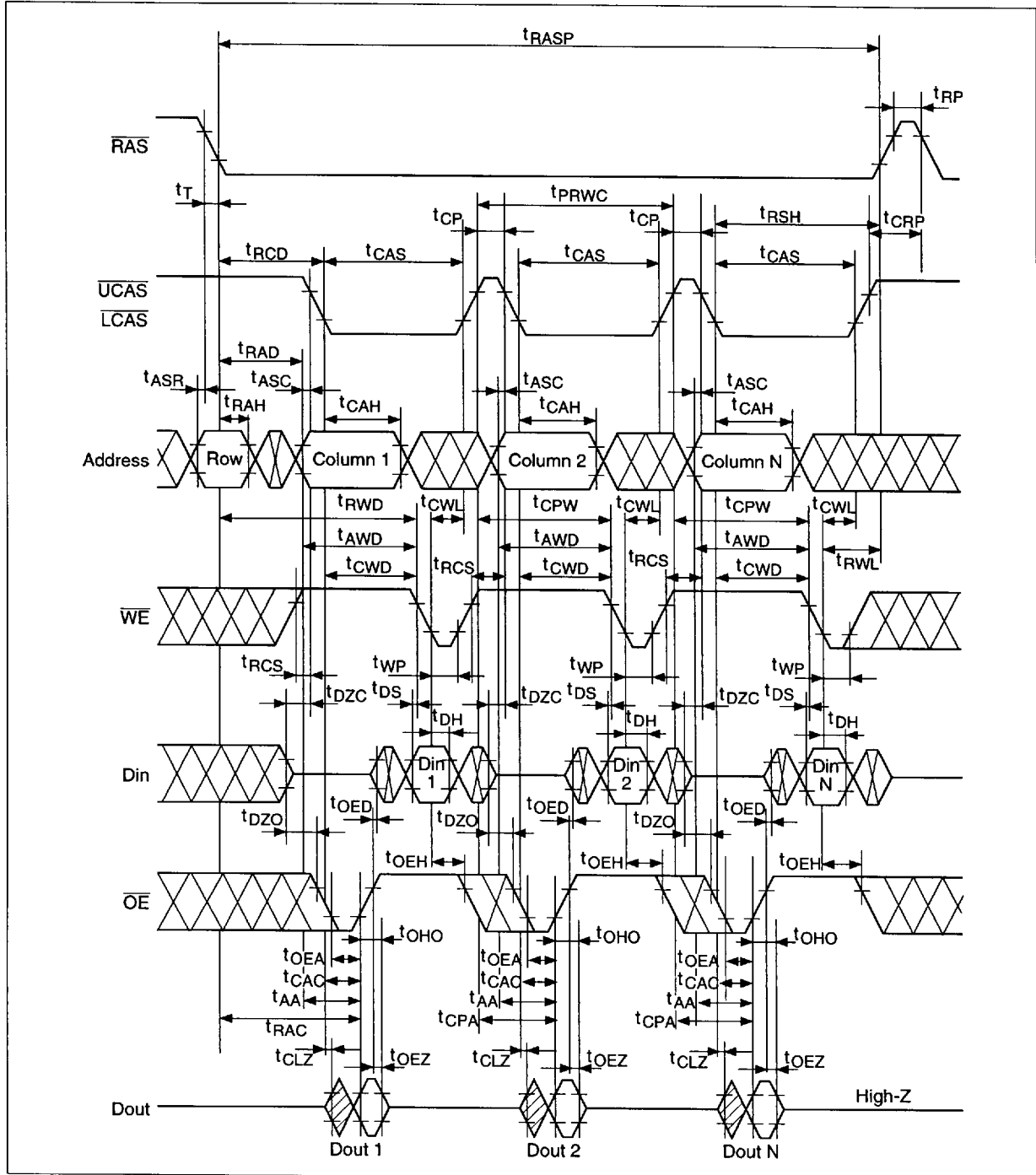


Fast Page Mode Delayed Write Cycle\*18



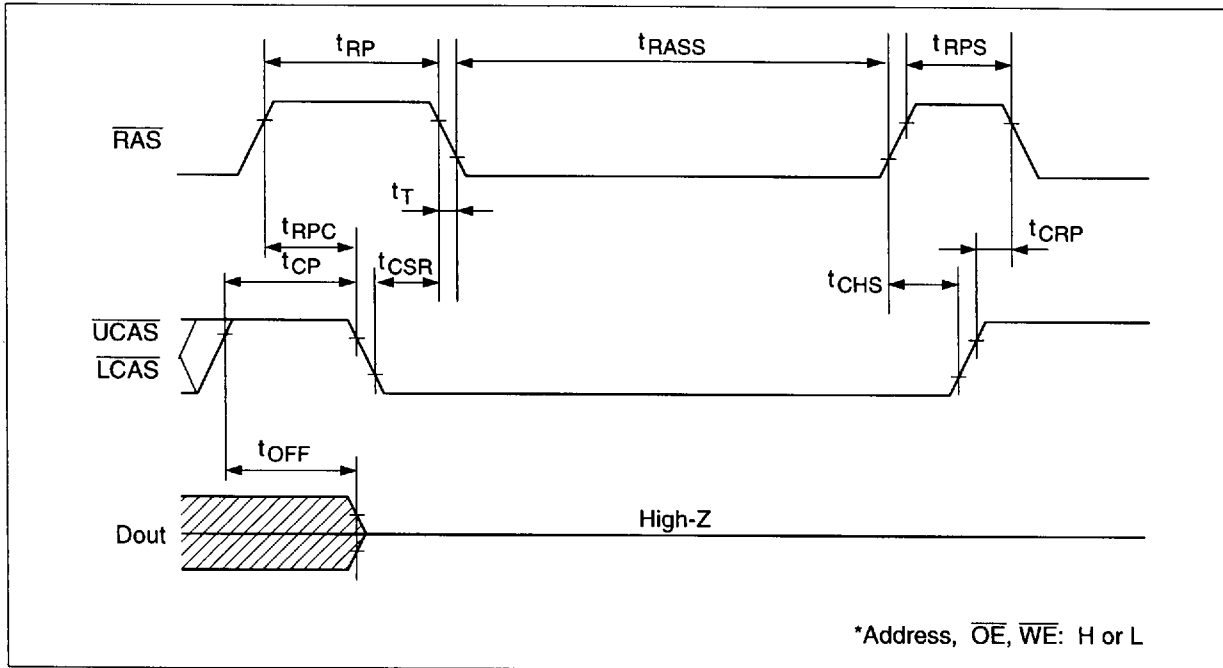
# HM5118160B Series

Fast Page Mode Read-Modify-Write Cycle\*18





Self Refresh Cycle (L-version) \*26, 27, 28, 29

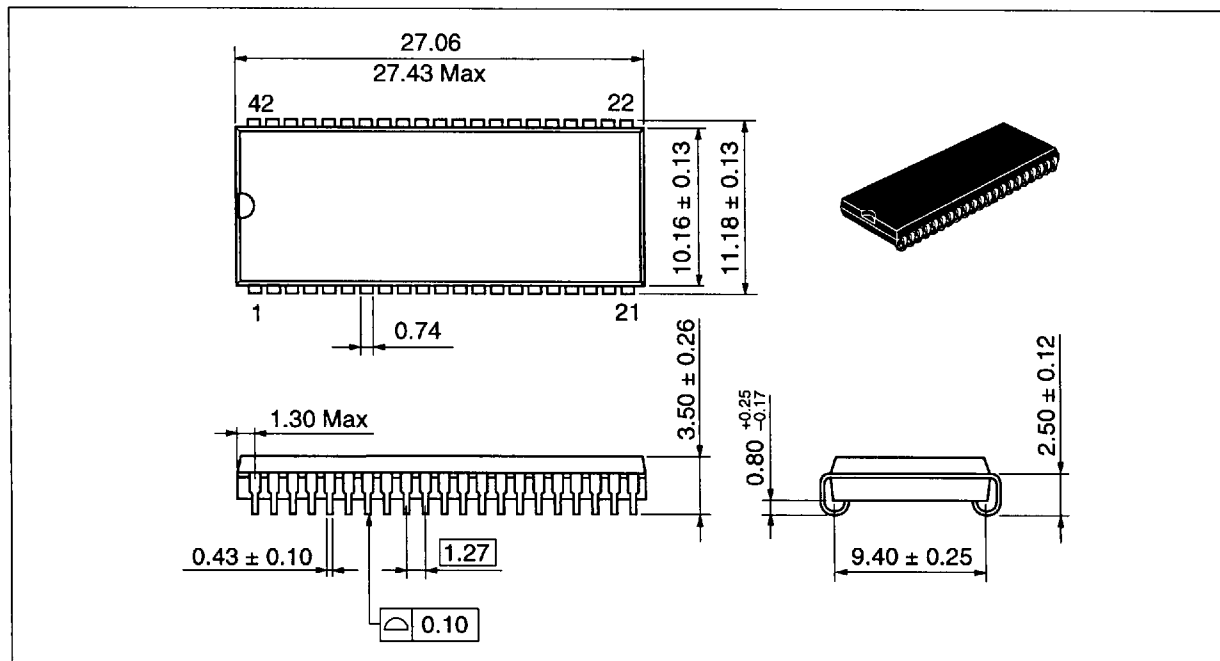


# HM5118160B Series

## Package Dimensions

HM5118160BJ/BLJ Series (CP-42D)

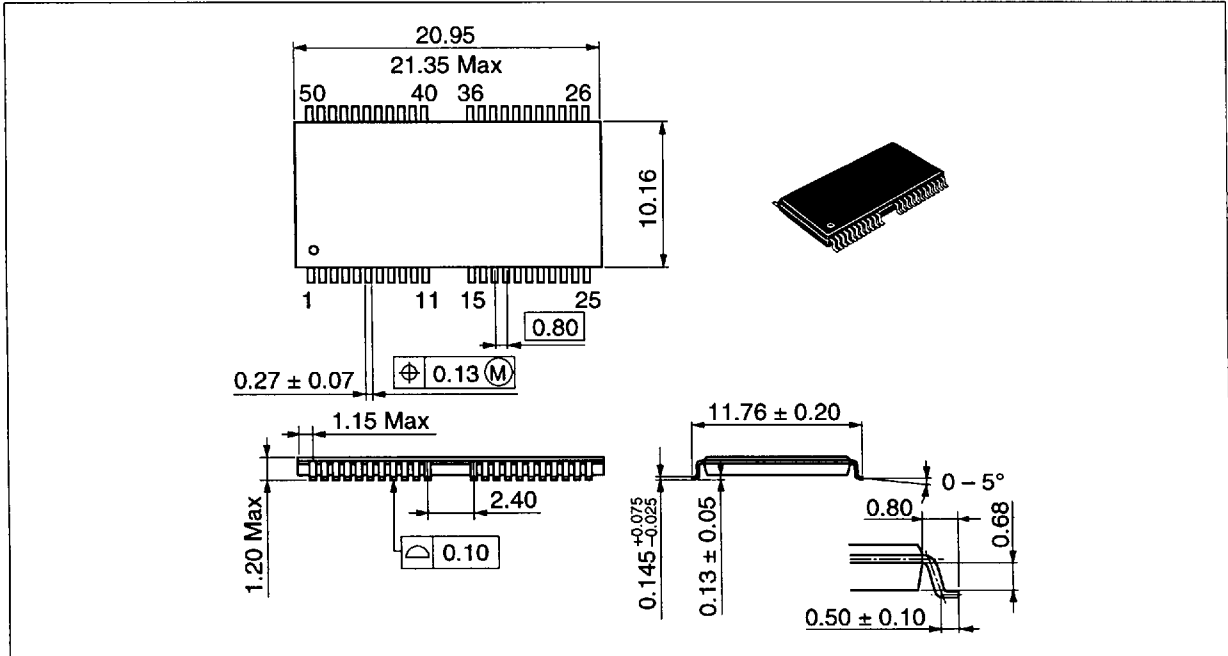
Unit: mm



# HM5118160B Series

HM5118160BTT/BLTT Series (TTP-50/44DC)

Unit: mm



HITACHI

27

4496203 0027208 881