

Radiation Hardened Synchronous Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(SI)
- Dose Rate Upset $>10^{10}$ RAD(SI)/s 20ns Pulse
- Cosmic Ray Upset Rate 2×10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
 - Standard Outputs..... 10 LSTTL Loads
- Military Temperature Range -55°C to $+125^{\circ}\text{C}$
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range 4.5V to 5.5V
- LSTTL Input Compatibility
 - $V_{IL} = 0.8V$ Max
 - $V_{IH} = V_{CC}/2$ Min
- Input Current Levels $I_I \leq 5\mu\text{A}$ at VOL, VOH

Description

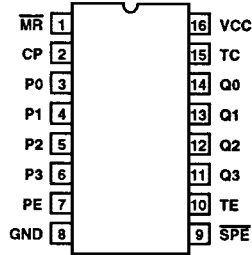
The Harris HCTS163MS is a Radiation Hardened synchronous presettable counter that feature look-ahead carry logic for use in high speed counting application. HCTS163MS is a binary counter, and is reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative to positive transition of the clock.

The HCTS163MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

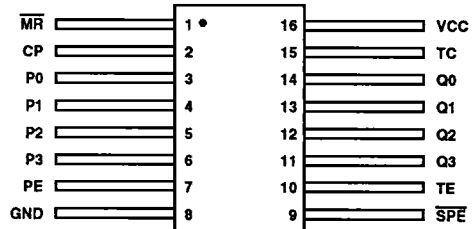
The HCTS163MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



HCTS163MS

Truth Table

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	PE	TE	\overline{SPE}	PN	QN	TC
Reset (clear)	l		X	X	X	X	L	L
Parallel Load	h (Note 3)		X	X	l	l	L	L
	h (Note 3)		X	X	l	h	H	(Note 1)
Count	h (Note 3)		h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	h (Note 3)	X	l (Note 2)	X	h (Note 3)	X	Qn	(Note 1)
	h (Note 3)	X	X	l (Note 2)	h (Note 3)	X	Qn	L

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

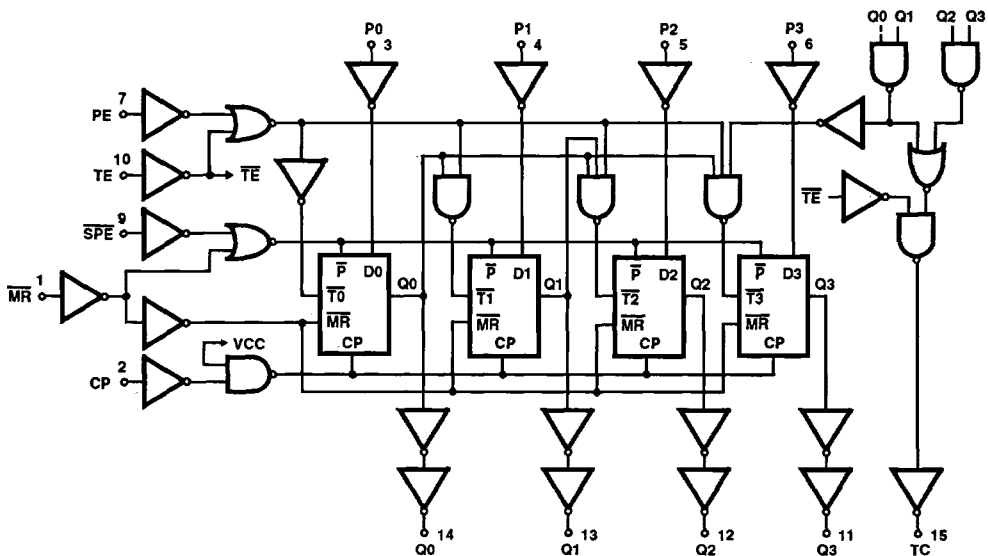
q = Lower case letter indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

= LOW-to-HIGH clock transition

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count (HLLH for 162 and HHHH for 163)
2. The HIGH-to-LOW transition of PE or TE on the 54/74163 and 54/74160 should only occur while CP is high for conventional operation
3. The LOW-to-HIGH transition of \overline{SPE} or \overline{MR} on the 54/74163 should only occur while CP is high for conventional operation

Functional Block Diagram



Specifications HCTS163MS

Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal)	±25mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W
Power Dissipation per Package (PD)		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	1W	
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 13mW/°C	

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 0.8V
Input Rise and Fall Times at 4.5 VCC (TR, TF)	50ns Max	Input High Voltage (VIH)	VCC/2 to VCC
Operating Temperature Range (TA)	-55°C to +125°C		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CP to Qn	TPHL TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns
CP to TC	TPHL TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns
MR to Qn, TC	TPHL	VCC = 4.5V	9	+25°C	2	50	ns
			10, 11	+125°C, -55°C	2	75	ns
TE to TC	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

- All voltages referenced to device GND.
- AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 52		pF
			+125°C	Typical 117		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	15	ns
			+125°C	-	22	ns

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP- ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC - 0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V

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TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP- ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	29	2	36	ns
CP to TC	TPLH TPLH	VCC = 4.5V	+25°C	2	33	2	40	ns
MR to Qn, TC	TPHL	VCC = 4.5V	+25°C	2	75	2	90	ns
TE to TC	TPHL	VCC = 4.5V	+25°C	2	29	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

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TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

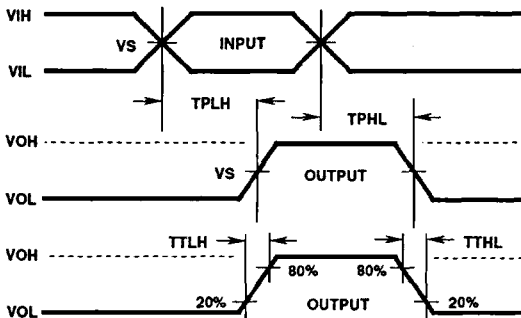
TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

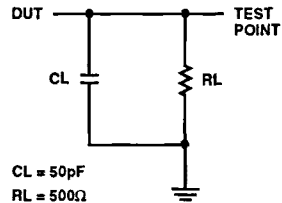
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
V_{IH}	3.00	V
V_S	1.30	V
V_{IL}	0	V
GND	0	V

AC Load Circuit



HCTS163MS

Die Characteristics

DIE DIMENSIONS:

104 x 86 mils

METALLIZATION:

Type: AlSi

Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2

Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

DIE ATTACH:

Material: Silver Epoxy

WORST CASE CURRENT DENSITY:

$< 2.0 \times 10^2 \text{ A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$

4 mils x 4 mils

Metallization Mask Layout

