CY7C1378
CY7C1379

ADVANCED INFORMATION

CYPRESS SEMICONDUCTOR

32K x 18 Synchronous Cache 3.3V RAM

SRAMs

Features

- **Supports 50-MHz Pentium® processor cache systems with zero wait states**
- **32K by 18 common I/O**
- **Fast clock-to-output times**
  - **12.5 ns with 0-pF load**
  - **14 ns with 85-pF load**
- **Two-bit wraparound counter supporting the Pentium™ and 486 burst sequence (7C1378)**
- **Two-bit wraparound counter supporting the linear burst sequence (7C1379)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **Industry-standard pinout**
- **52-pin PLCC and PQFP packaging**

Functional Description

The CY7C1378 and CY7C1379 are 3.3V 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 12.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C1378 is designed for Intel Pentium and i486 CPU−based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1379 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram

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Pin Configuration

PLCC
Top View
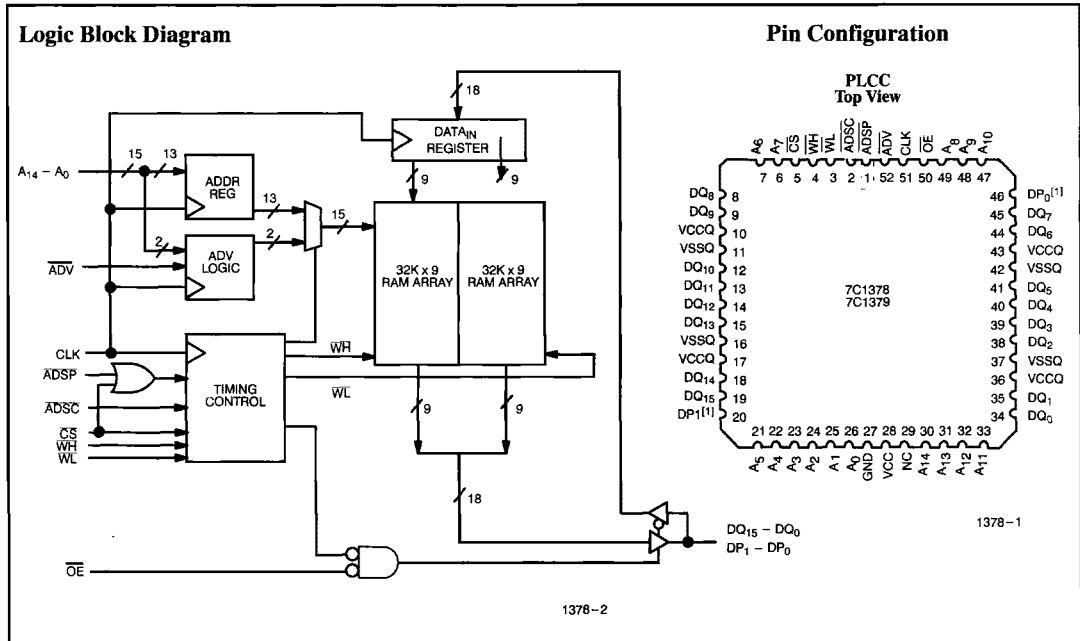
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Selection Guide

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Maximum Access Time (ns) (0-pF Load)		12.5	16.5	19.5
Maximum Operating Current (mA)	Commercial	180	160	150
	Military			170

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Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_x.