FEATURES

- **Very Low Power Consumption ..... 1.5mW Max**
- **Low Input Offset Voltage ..... 1mV Max**
- **Very Low Drift ..... 3μV/°C Typ**
- **High Output-Drive Current ..... 25mA Typ**
- **Single or Dual Supply Operation**
- **Ideal for CMOS Logic Interface**
- **LM139 Pinout**
- **Available in Die Form**

ORDERING INFORMATION†

25°C V_{OS} (mV)	HERMETIC DIP PACKAGE	OPERATING TEMPERATURE RANGE
1	CMP404AY*	MIL
1	CMP404EY	IND
2	CMP404FY	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

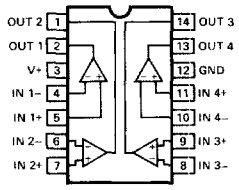
GENERAL DESCRIPTION

Four precision-input comparators provide excellent speed with low power consumption through use of a novel Schottky-clamped design. These open-collector output comparators only consume 365 microwatts each, yet they make accurate 5mV decisions in only four microseconds. In addition, they can drive load currents of 25mA. This output stage is ideal for driving relays, lamps, and LEDs.

The low input-offset-voltage makes the CMP-404 an ideal companion to CMOS logic when the stability and accuracy of a bipolar technology is needed along with low power consumption. The open-collector outputs with pull-up resistors provide CMOS interface with excellent noise immunity. Improved isolation between comparators was achieved by use of an independent bias circuit for each comparator. This is especially important when one comparator is detecting low-level signals while an adjacent comparator is being driven by a high-level signal. In single-supply operation, the inputs can operate at ground. The CMP-404 can operate from 5 to 30 volts single supply or ±2.5 to ±15 volts dual supply.

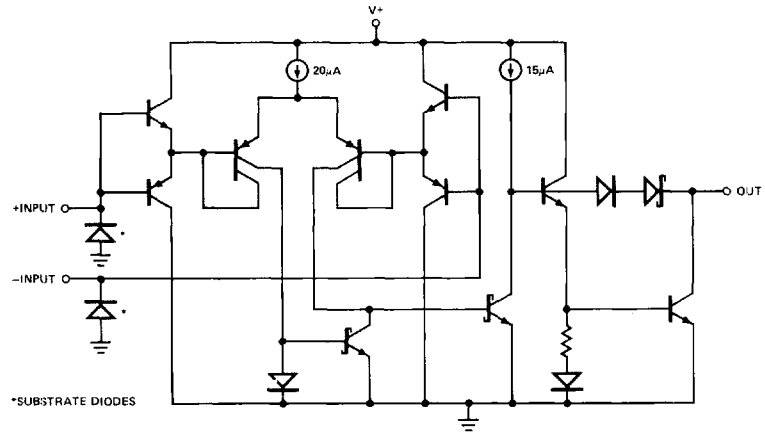
Window comparators, limit comparators, multivibrators, one shots, voltage-controlled oscillators, and set-point detectors are common applications.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC (1/4 OF CMP-404)



8 VOLTAGE COMPARATORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... 36V or ±18V
Input Voltage ..... –0.3V to V+
Output Voltage ..... –0.3 to 36V
Derate Above 100°C by ..... 10mW/°C
Thermal Resistance (Θ_{jA}) ..... 100°C/W
Operating Temperature Range
CMP-404EY/FY ..... –25°C to +85°C
CMP-404 AY ..... –55°C to +125°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Input Current (Note 2) 20mA
Output Short-Circuit to V+ (Note 3) 50mA
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{jA} (Note 4)	Θ_{jC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

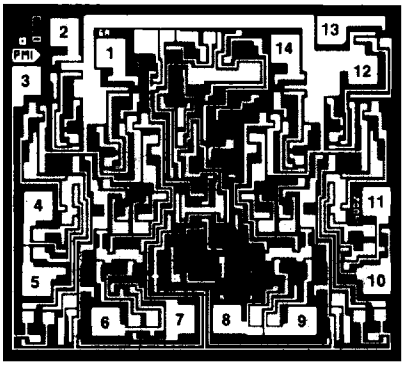
NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Limit for input current that flows when input voltage signals exceed V+ or GND forward biasing internal junctions.
3. Short circuits to V+ can cause excessive heating and eventual destruction. The maximum output current is 50mA.
4. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = 5V, R_L = 5.1kΩ and –55°C ≤ T_A ≤ +125°C for CMP-404AY; –25°C ≤ T_A ≤ +85°C for CMP-404EY/FY, unless otherwise noted.

			CMP-404A/E			CMP-404B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 50Ω, T_A = 25°C	—	—	1	—	—	2	mV
		R_S = 50Ω, Full Temp	—	—	2	—	—	3	mV
Average Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	—	3	—	—	3	—	µV/°C
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C	—	3	10	—	3	25	nA
		$I_{IN(+)} - I_{IN(-)}$, Full Temp	—	—	50	—	—	100	nA
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C	—	10	50	—	10	100	nA
		$I_{IN(+)}$ or $I_{IN(-)}$, Full Temp	—	—	100	—	—	200	nA
Voltage Gain	A_V	R_L = 15kΩ	50	400	—	50	400	—	V/mV
Small-Signal Response Time	t_r	V_{OD} = 5mV, V_{STEP} = 100mV R_L = 5.1kΩ, T_A = 25°C (Note 4)	—	3.5	5	—	3.5	5	µs
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, R_L = 5.1kΩ	—	0.8	—	—	0.8	—	µs
Input Voltage Range	CMVR	T_A = 25°C	0	—	V+ –1.5	0	—	V+ –1.5	V
		T_A = Full Temp	0	—	V+ –2	0	—	V+ –2	V
Common-Mode Rejection Ratio	CMRR	R_L = 15kΩ, (Note 6)	75	85	—	75	85	—	dB
Saturation Voltage	V_{OL}	T_A = 25°C, (Note 2)	—	0.32	0.4	—	0.32	0.4	V
		Full Temp, (Note 2)	—	—	0.5	—	—	0.5	V
Output Sink Current	I_{SINK}	$V_{IN(-)}$ = 1V $V_{IN(+)}$ = 0V, V_O = 2V, (Note 5)	10	25	—	10	25	—	mA
Output Leakage Current	I_{LEAK}	T_A = 25°C, (Note 3)	—	0.01	0.1	—	0.01	0.1	µA
		Full Temp, (Note 3)	—	—	0.4	—	—	0.4	µA
Power Supply Rejection Ratio	PSRR	V– = 5V to 30V, R_L = 15kΩ	75	100	—	65	100	—	dB
Supply Current	I+	R_L = ∞	—	220	300	—	220	350	µA

NOTES:
1. Typical values are reported for T_A = 25°C.
2. I_{SINK} = 1mA, $V_{IN(-)}$ = 1V, $V_{IN(+)}$ = 0V
3. $V_{IN(-)}$ = 0V, $V_{IN(+)}$ = 1V, V_O = 30V
4. Guaranteed by design. See response-time test circuit.
5. Output Sink Current should be limited to 50mA by external resistance.
6. Applies over the CMVR range.

DICE CHARACTERISTICS



DIE SIZE 0.069 × 0.077 inch, 5313 sq. mils
(1.753 × 1.956 mm, 3.43 sq. mm)

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND
13. OUTPUT (4)
14. OUTPUT (3)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at V+ = 5V, R_L = 5.1kΩ, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404G LIMIT	UNITS
Input Offset Voltage	V_{OS}	R_S = 50Ω	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$	100	nA MAX
Voltage Gain	A_V	R_L = 15kΩ	50	V/mV MIN
Input Voltage Range	CMVR		V− −1.5	V MAX
Common-Mode Rejection Ratio	CMRR	R_L = 15kΩ	75	dB MIN
Power Supply Rejection Ratio	PSRR	V− = 5V to 30V, R_L = 15kΩ	65	dB MIN
Saturation Voltage	V_{OL}	I_{SINK} = 1mA	0.4	V MAX
Output Sink Current	I_{SINK}	$V_{IN(-)}$ = 1V $V_{IN(+)}$ = 0V, V_O = 2V	10	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(-)}$ = 0V $V_{IN(+)}$ = 1V, V_O = 30V	0.1	μA MAX
Supply Current	I+	R_L = ∞	300	μA MAX

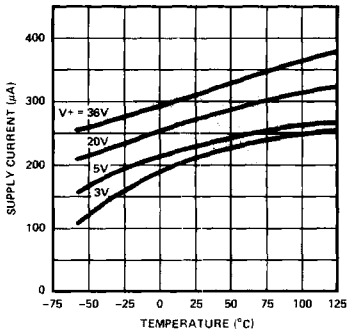
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 5V, unless otherwise noted.

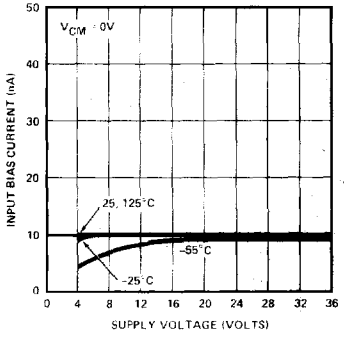
PARAMETER	SYMBOL	CONDITIONS	CMP-404G TYPICAL	UNITS
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, R_L = 5.1kΩ	0.8	μs
Small-Signal Response Time	t_r	V_{OD} = 5mV, V_{STEP} = 100mV R_L = 5.1kΩ	3.5	μs

TYPICAL PERFORMANCE CHARACTERISTICS

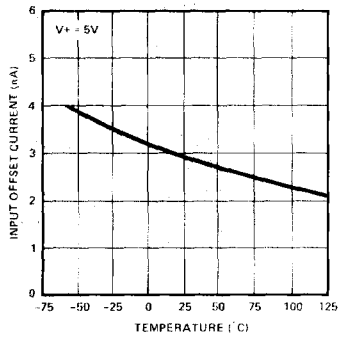
SUPPLY CURRENT vs TEMPERATURE



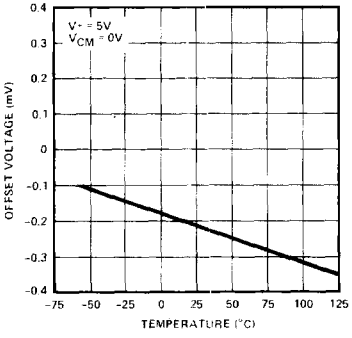
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



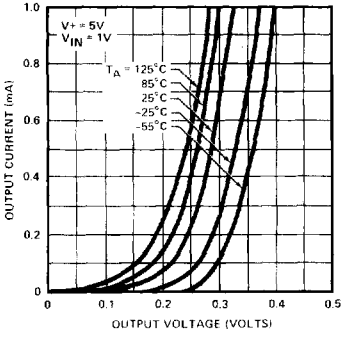
INPUT OFFSET CURRENT vs TEMPERATURE



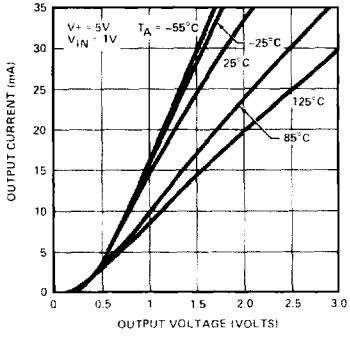
OFFSET VOLTAGE vs TEMPERATURE



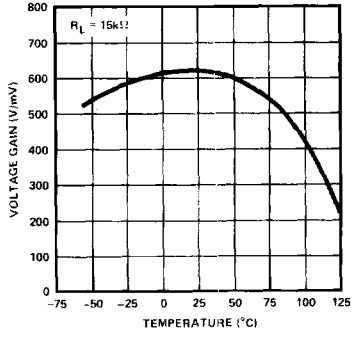
OUTPUT CURRENT vs OUTPUT VOLTAGE



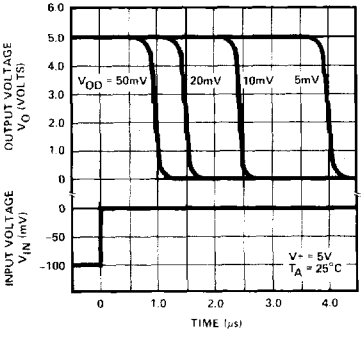
OUTPUT CURRENT vs OUTPUT VOLTAGE



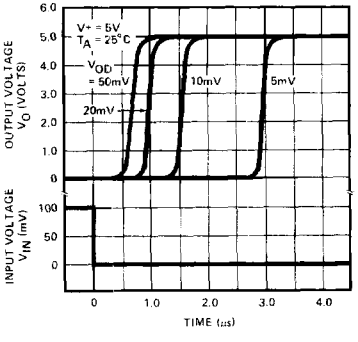
OPEN-LOOP GAIN vs TEMPERATURE



NEGATIVE RESPONSE TIME vs OVERDRIVE

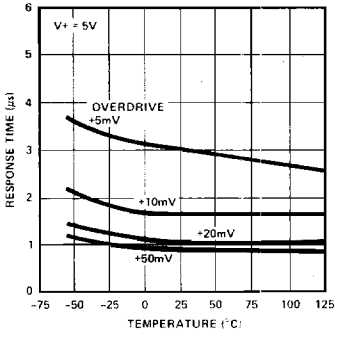


POSITIVE RESPONSE TIME vs OVERDRIVE

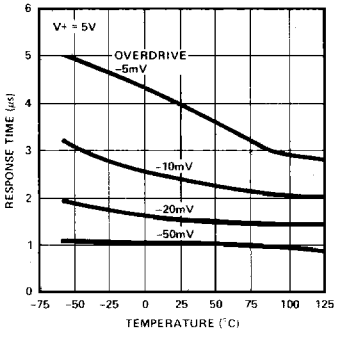


TYPICAL PERFORMANCE CHARACTERISTICS

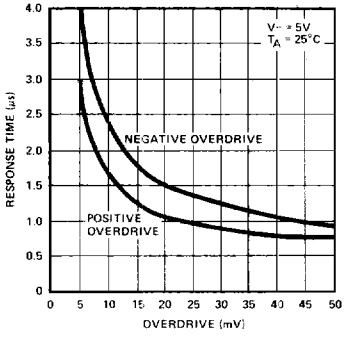
POSITIVE RESPONSE TIME vs TEMPERATURE



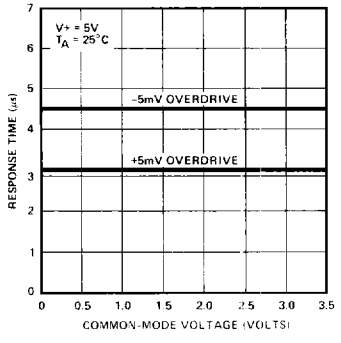
NEGATIVE RESPONSE TIME vs TEMPERATURE



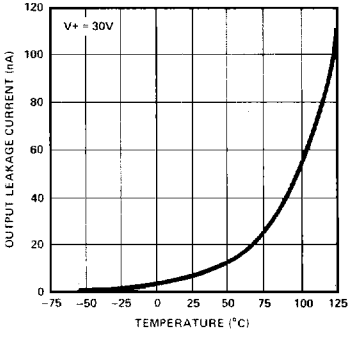
RESPONSE TIME vs OVERDRIVE



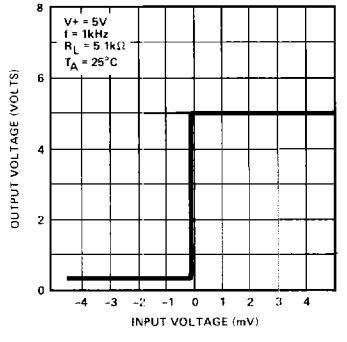
RESPONSE TIME vs COMMON-MODE VOLTAGE



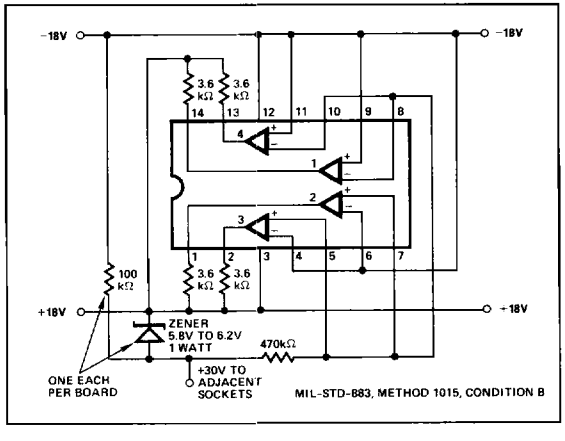
OUTPUT LEAKAGE vs TEMPERATURE



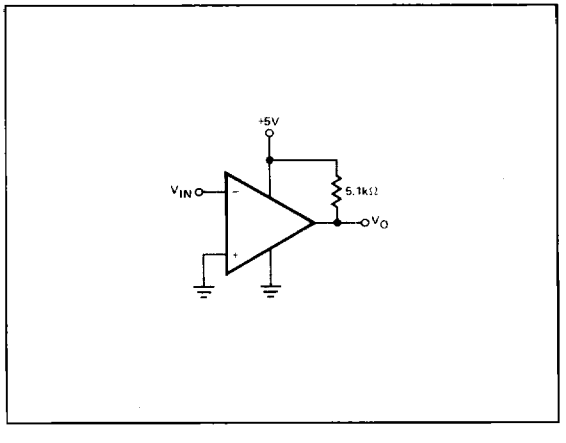
INPUT-OUTPUT TRANSFER CHARACTERISTIC



BURN-IN CIRCUIT



RESPONSE-TIME TEST CIRCUIT



APPLICATIONS INFORMATION

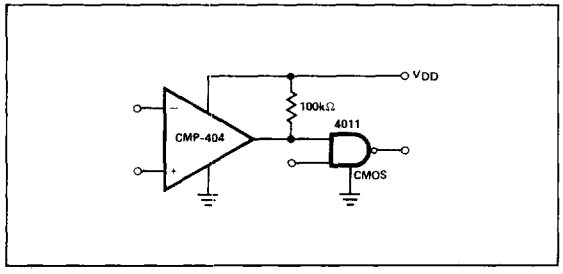
The use of non-saturated switching within the CMP-404 design results in optimized response time. The high-gain output stage drives large load currents with a minimum saturation voltage (V_{OL}). This provides excellent noise margin when driving LSTTL loads. An independent bias network for each comparator inside the CMP-404 minimizes crosstalk between comparators. This proves especially important when one comparator is detecting low-level signals while adjacent comparators are making transitions.

Input signals should be confined to between the power supply rails. Input signals exceeding either V+ or GND will forward-bias internal junctions. Input current during forward bias should be limited to 20mA.

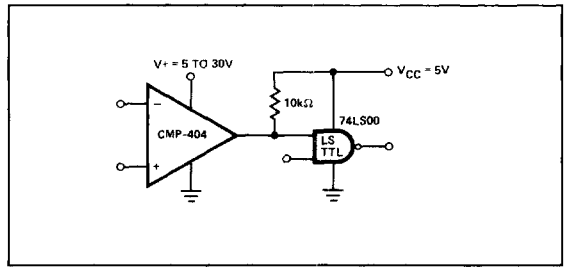
Exceeding the positive end of the common-mode input-voltage-range will cause the comparator output transistor to turn on, thus resulting in a continuous logic-low output state.

The open-collector output stage can be easily wire-OR-ed to make window comparators. The open-collector output also simplifies shifting of logic levels between different supply levels. The output transistors easily drive high-current loads, which is especially useful in fault-detector circuits for driving high-level enunciators (piezo horns, relays, lamps, or red LEDs).

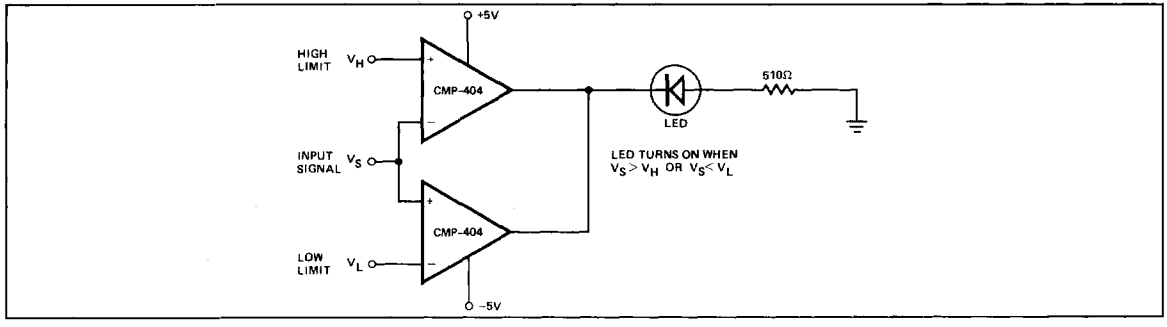
CMOS INTERFACING



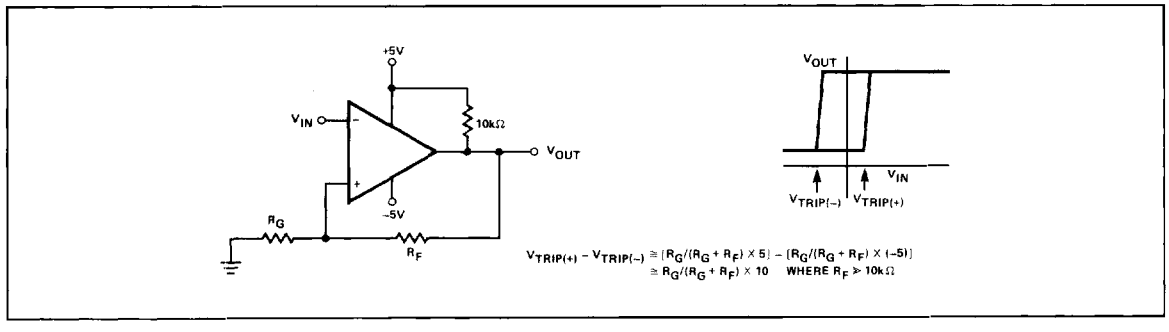
TTL INTERFACING



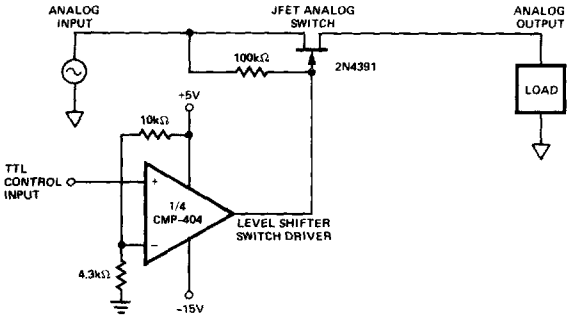
LIMIT DETECTOR (WINDOW COMPARATOR)



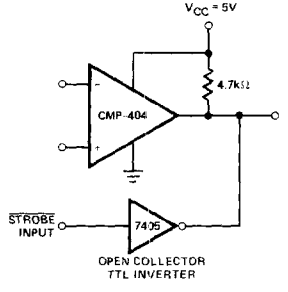
SETTING UP HYSTERESIS



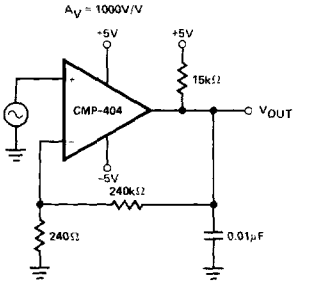
TTL-COMPATIBLE ANALOG SWITCH



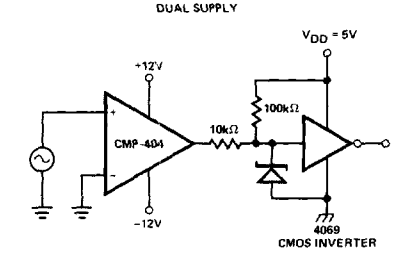
OUTPUT STROBING

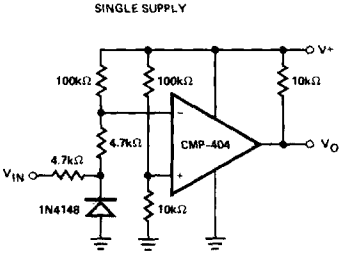


LOW-FREQUENCY OPERATIONAL AMPLIFIER

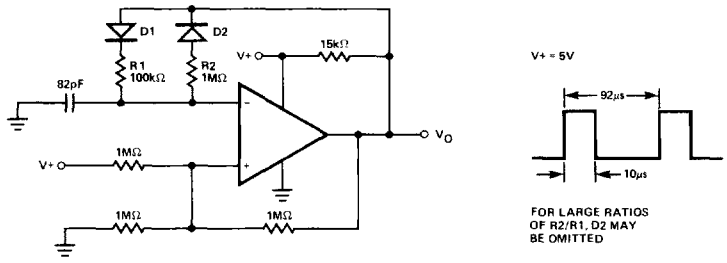


ZERO-CROSSING DETECTOR CIRCUITS

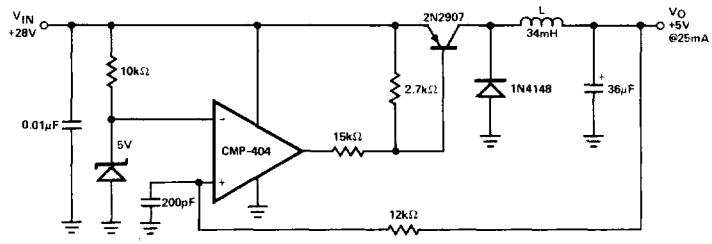




PULSE GENERATOR



REGULATED DC-TO-DC CONVERTER



NOTE:
OPERATING FREQUENCY OF 2.4kHz IS DETERMINED PRIMARILY BY VALUE OF L. THE INDUCTOR MUST HAVE A SATURATION CURRENT HIGHER THAN ITS PEAK OPERATING CURRENT.