Features

- Floating channel designed for bootstrap operation.
- Fully operational up to +600V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Independent low and high side channels.
- Input logic HIN/LIN active high
- Undervoltage lockout for both channels
- 3.3V, 5V, and 15V input logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for two channels
- Lead-Free and RoHS Compliant
- Automotive qualified*

Typical Applications

- High power DC-DC SMPS converters
- Other high frequency applications

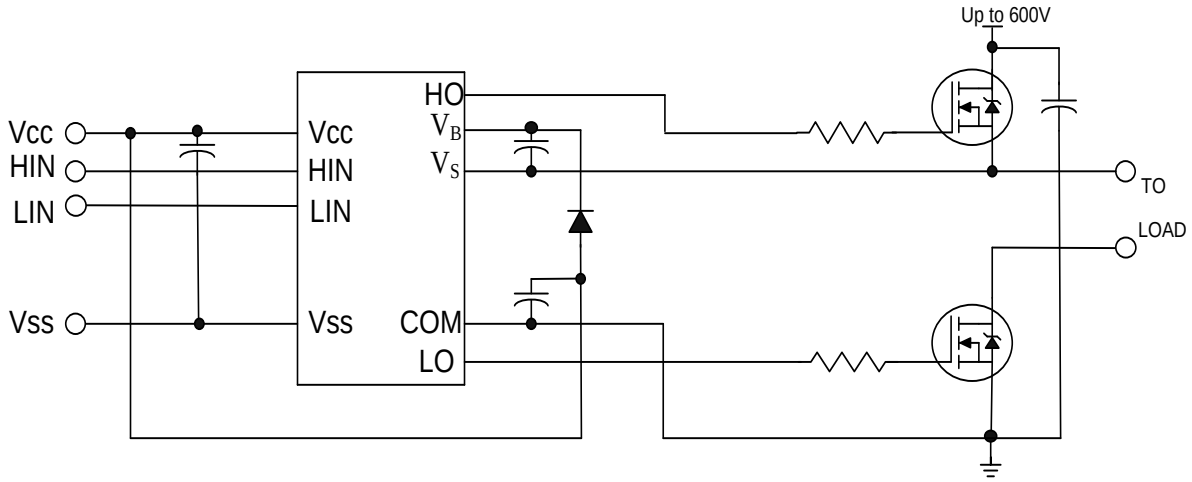
Product Summary

V_{OFFSET}	≤ 600V
V_{OUT}	10 – 20V
I_{o+} & I_{o-} (typical)	3.5A & 3.5A
t_{ON} & t_{OFF} (typical)	90ns & 90ns
Delay Matching (max)	25ns

Package Options

16-Lead SOIC Narrow Body

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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Description

The AUIRS2191S is a high power, high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels, ideal for DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600V. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
Moisture Sensitivity Level		MSL3†† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M1 (100V) (per AEC-Q100-003)
	Human Body Model	Class H1B (1000V) (per AEC-Q100-002)
	Charged Device Model	Class C4 (1000V) (per AEC-Q100-011)
IC Latch-Up Test		Class II Level A (per AEC-Q100-004)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply voltage	-0.3	620	V
V_S	High side floating supply offset voltage	V_B – 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S – 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage	-0.3	20	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	V_{SS} – 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground	V_{CC} – 20	V_{CC} + 0.3	
dV_S/dt	Allowable V_S offset supply transient	---	50	V/ns
P_D	Package power dissipation @ $T_A \leq$+25 ºC	---	1.0	W
$R_{\Theta JA}$	Thermal resistance, junction to ambient	---	100	ºC/W
T_J	Junction temperature	---	150	ºC
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS, VSS, and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	†	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	V_{SS}	V_{CC}	
V_{SS}	Logic ground	-5	5	
T_A	Ambient temperature	-40	125	ºC

† Logic operation for V_S of –5 V to 600 V. Logic state held for V_S of –5 V to $-V_{BS}$. (Please refer to Design Tip DT97-3 for more details)

Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (VCC or VBS) = 15V. The VIN, VTH parameters are referenced to VSS and are applicable to all logic input leads: HIN and LIN. The VO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	---	---	V	V_{CC} = 9.8V – 20V
V_{IL}	Logic "0" input voltage	---	---	0.8		
V_{OH_2mA}	High level output voltage, V_{BIAS}-V_O	---	---	2.5		I_o= 2 mA
V_{OH_20mA}	High level output voltage, V_{BIAS}-V_O	---	---	3.3		I_o= 20 mA
V_{OL}	Low level output voltage, V_O	---	---	0.1		I_o= 2 mA
I_{LK}	Offset supply leakage current	---	---	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	---	100	200		V_{IN} = 0V or 3.3V
I_{QCC}	Quiescent V_{CC} supply current	---	150	300		V_{IN} = 0V or 3.3V
I_{QBS18}	Quiescent V_{BS} supply current	---	180	300		V_{IN} = 0V or 3.3V V_{BS}=18V
I_{QCC18}	Quiescent V_{CC} supply current	---	300	450		V_{IN} = 0V or 3.3V V_{CC}=18V
I_{QBS20}	Quiescent V_{BS} supply current	---	850	1500		V_{IN} = 0V or 3.3V V_{BS}=20V
I_{QCC20}	Quiescent V_{CC} supply current	---	1500	2500		V_{IN} = 0V or 3.3V V_{CC}=20V
I_{IN+}	Logic "1" input bias current	---	3.5	7		V_{IN} = 3.3V
I_{IN-}	Logic "0" input bias current	---	---	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	8.8		
$V_{BSUVHYS}$	V_{BS} supply undervoltage hysteresis	0.3	0.7	---		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{CCUVHYS}$	V_{CC} supply undervoltage hysteresis	0.3	0.7	---		
I_{O+}	Output high short circuit pulsed current (†)	2.6	3.5	---	A	V_O = 0 V, PW ≤ 10 µs, Tj = 25°C
I_{O-}	Output low short circuit pulsed current(†)	2.6	3.5	---		V_O = 15 V, PW ≤ 10 µs Tj = 25°C
I_{O+}	Output high short circuit pulsed current (†)	1.8	3.5	---	A	V_O = 0 V, PW ≤ 10 µs,
I_{O-}	Output low short circuit pulsed current(†)	1.8	3.5	---		V_O = 15 V, PW ≤ 10 µs

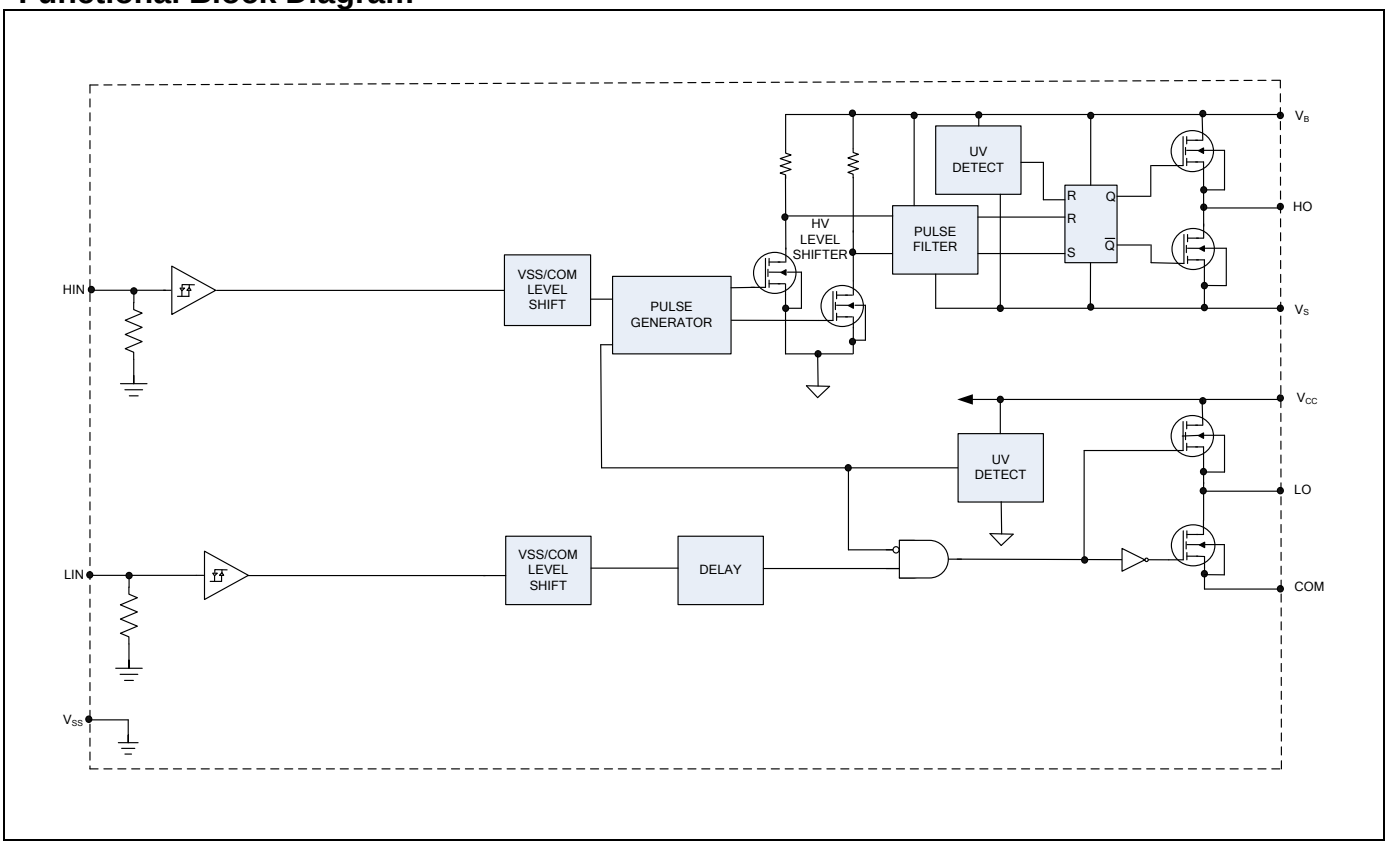
(†) Guaranteed by design

Dynamic Electrical Characteristics

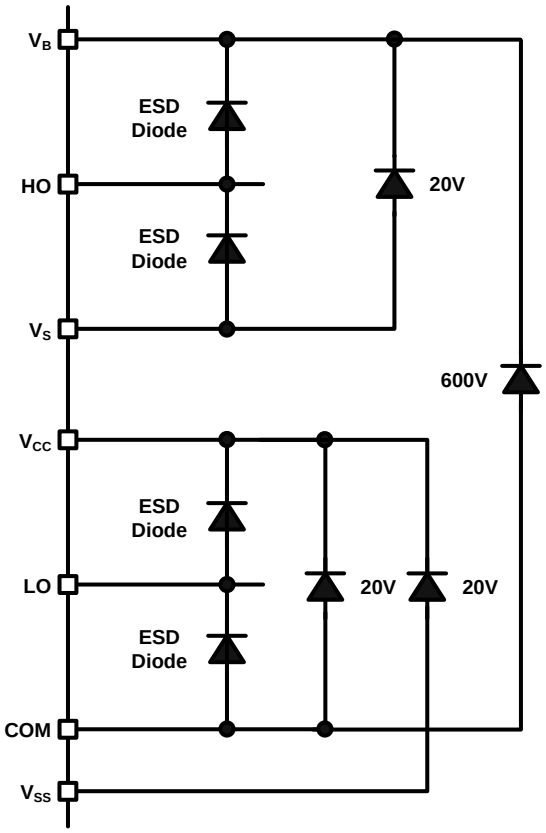
Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤125°C with bias conditions of V_{BIAS} (VCC, VBS) = 15V, CL = 1000 pF. The dynamic electrical characteristics are measured using the test definitions shown in Figure 3.

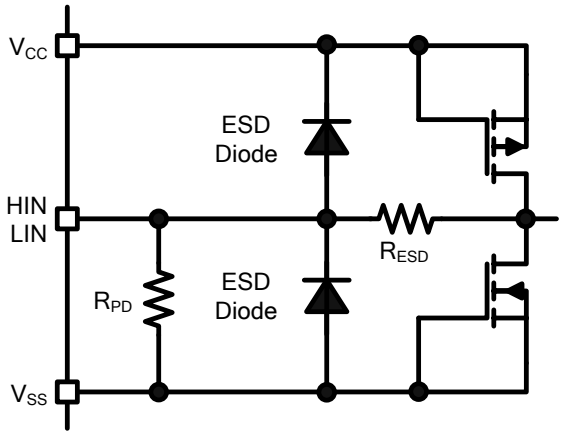
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{ON}	Turn-on propagation delay	50	90	175	ns	V_S = 0V
t_{OFF}	Turn-off propagation delay	50	90	175		V_S = 0V or 600V
t_R	Turn-on rise time	5	15	60		
t_F	Turn-off fall time	5	15	60		
MT	Delay matching, HS & LS turn-on/off	---	---	25		

Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams: AUIRS2191

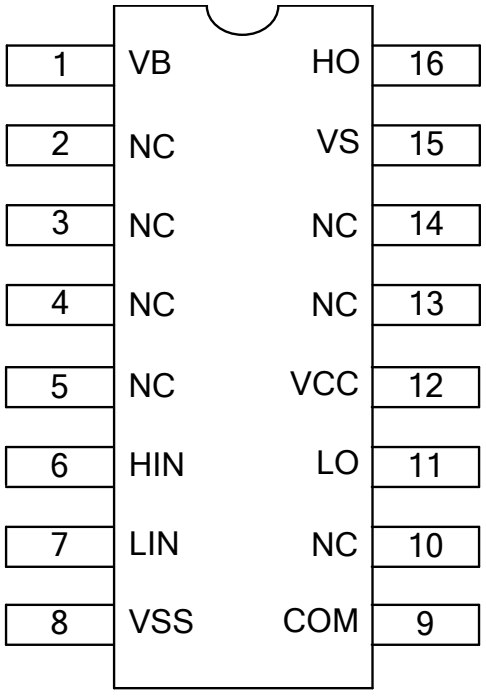




Lead Definitions: AUIRS2191

Pin#	Symbol	Description
1	VB	High-side floating supply
6	HIN	Logic inputs for high-side gate driver output (HO), in phase (referenced to V_{SS})
7	LIN	Logic inputs for low-side gate driver output (LO), in phase (referenced to V_{SS})
8	VSS	Low-side logic return
9	COM	Low-side return
11	LO	Low-side gate drive output
12	VCC	Low-side supply voltage
15	VS	High voltage floating supply return
16	HO	High-side gate drive output

Lead Assignments



16 Lead SOIC

Application Information and Additional Details

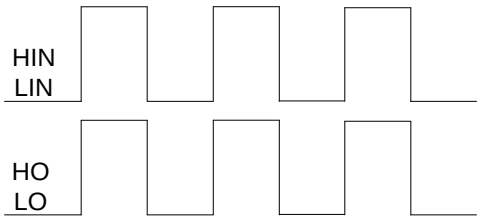


Figure 1. Input/Output Timing Diagram

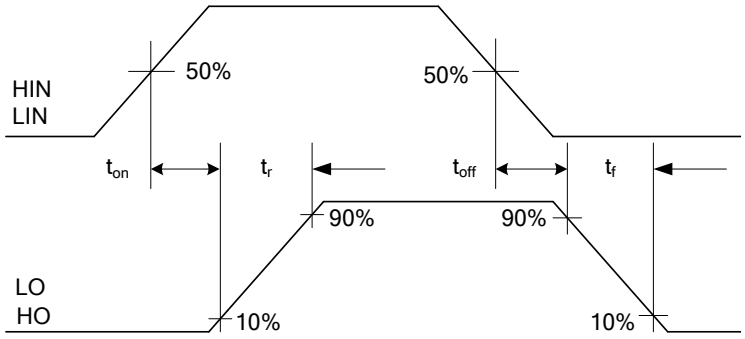


Figure 2. Switching Time Waveform Definitions

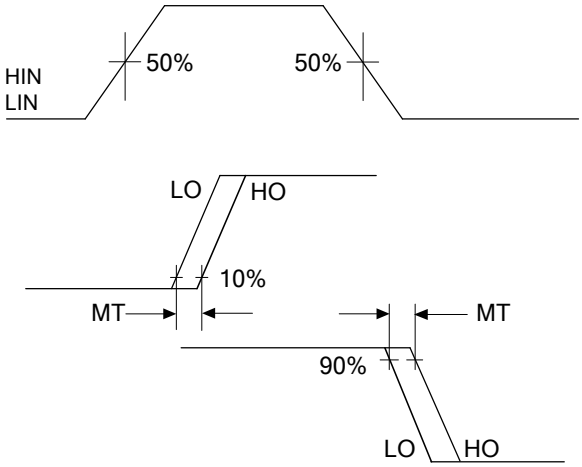


Figure 3. Delay Matching Waveform Definitions

Tolerability to Negative VS Transients

The AUIRS2191S has been seen to withstand negative V_S transient conditions on the order of -30V for a period of 400 ns. An illustration of the AUIRS2191S performance can be seen in Figure 7, where points above the line represent pulses that the circuit can withstand (with V_{CC}=V_{BS}= 15V and T_A = 25°C).
Effect of ambient temperature on tolerability to negative Vs Transient is quite contained, in fact tests performed at -40^C and at 125^C showed how, for a given pulse duration, the AUIRS2191S can withstand negVs pulse of absolute amplitude 5V lower than what represented by the line in Figure 7.
So, in whole temperature range the curve of Figure 7 has to be risen up of 5V.
Even though the AUIRS2191S has been shown able to handle these negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

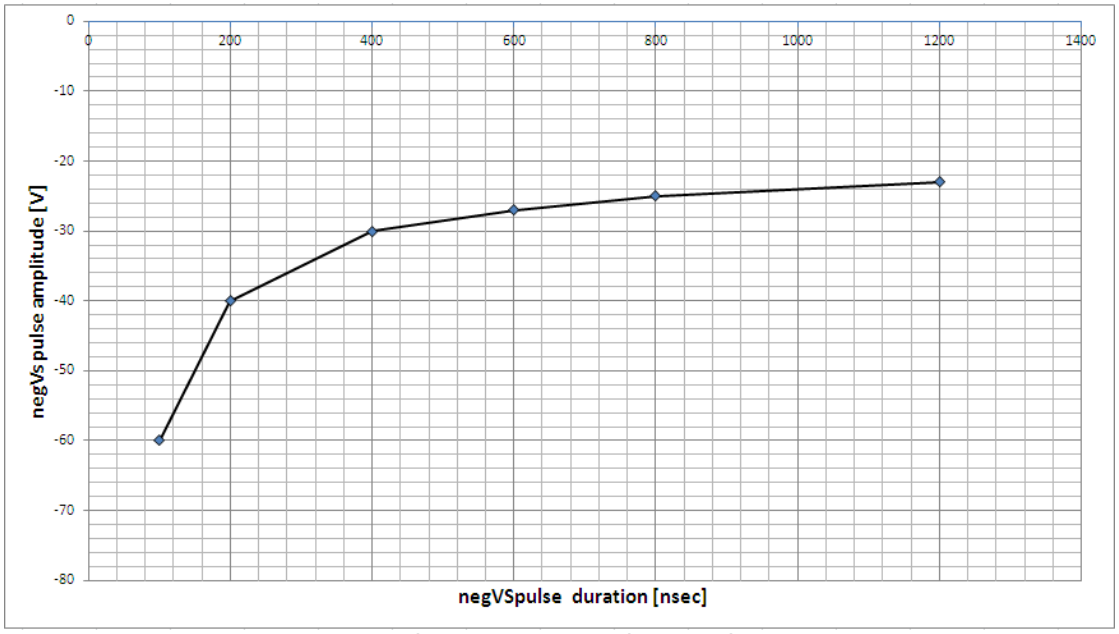


Figure 7: -Vs Transient results

Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2191S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

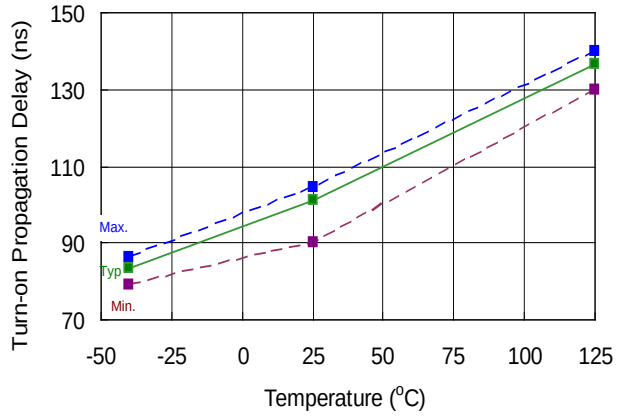


Figure 4. Turn-On Time vs. Temperature

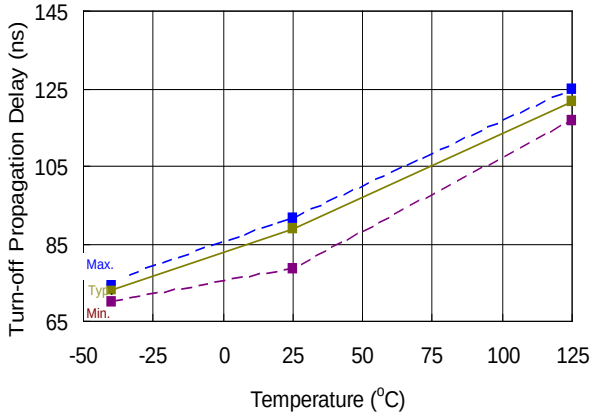


Figure 5. Turn-Off Time vs. Temperature

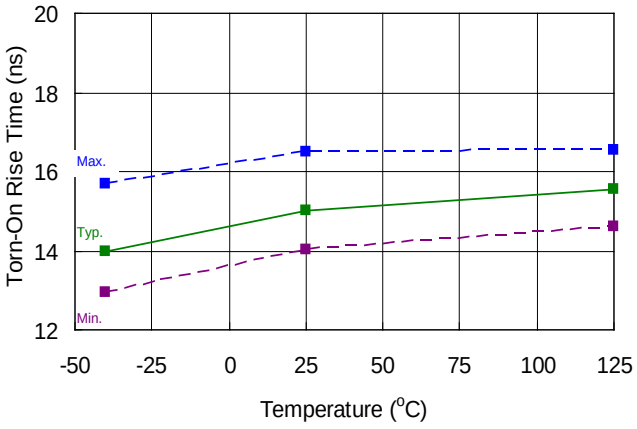


Figure 6. Turn-On Rise Time vs. Temperature

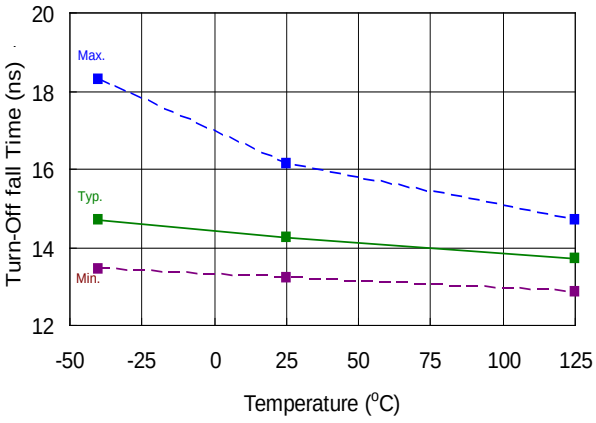


Figure 7. Turn-Off Fall Time vs. Temperature

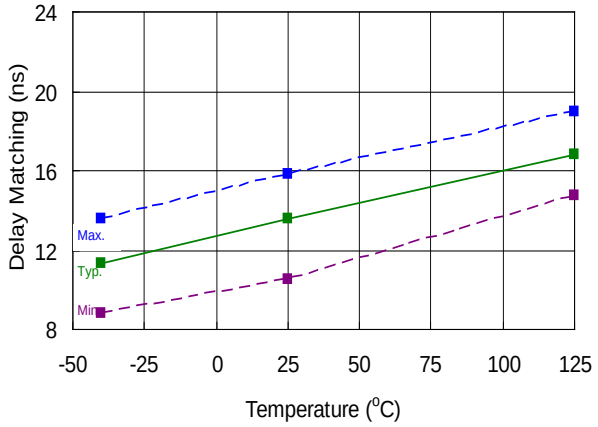


Figure 8. Delay Matching Time vs. Temperature

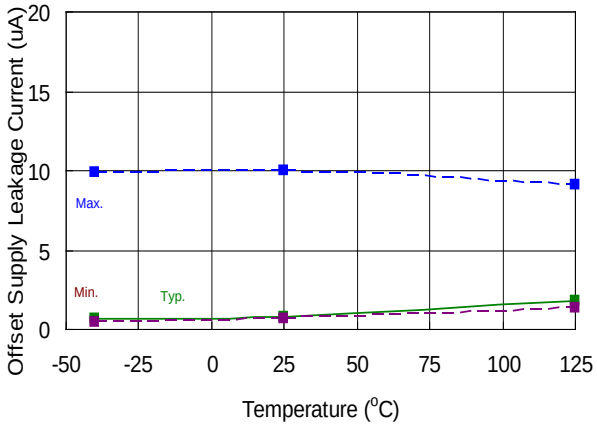


Figure 9. Offset Supply Current vs. Temperature

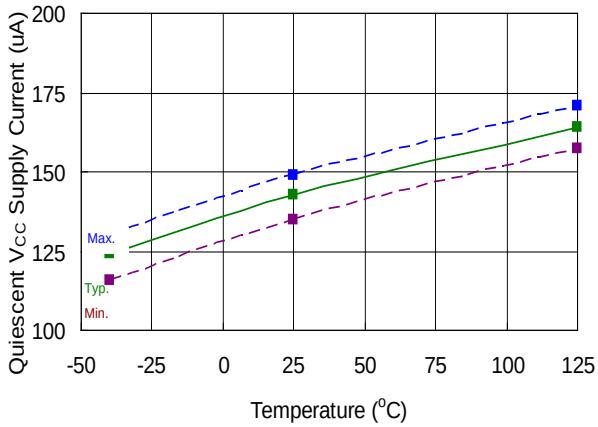


Figure 10. V_{CC} Supply Current vs. Temperature

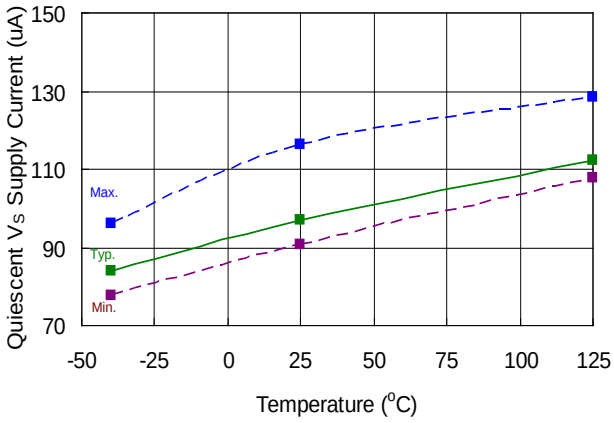


Figure 11. V_{BS} Supply Current vs. Temperature

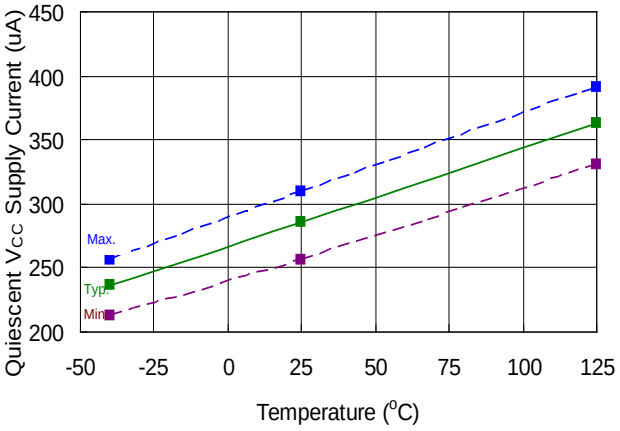


Figure 12. V_{CC} = 18V Supply Current vs. Temperature

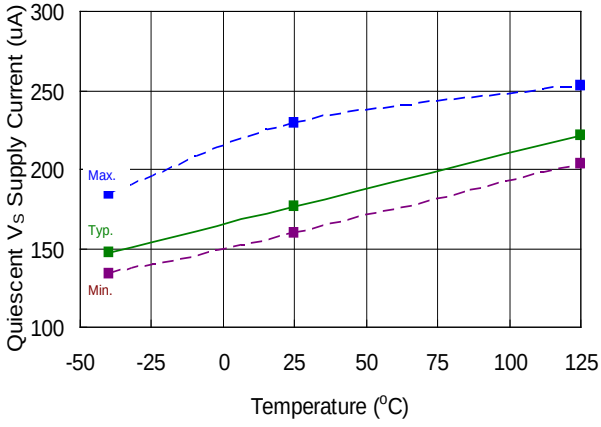


Figure 13. V_{BS} = 18V Supply Current vs. Temperature

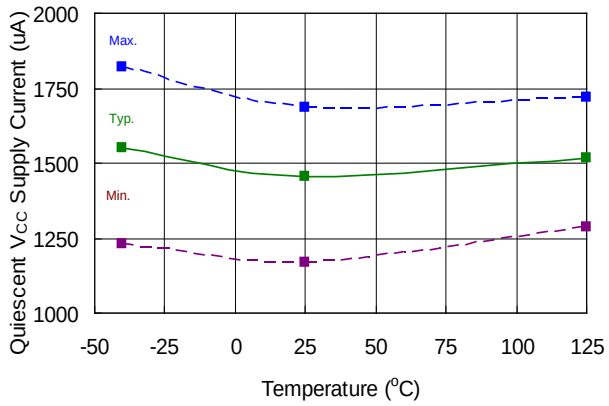


Figure 14. V_{CC} = 20V Supply Current vs. Temperature

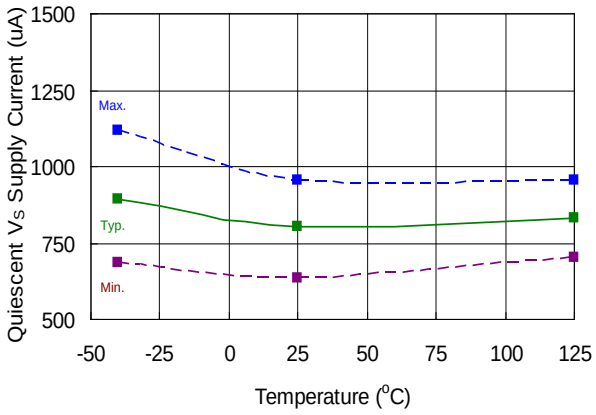


Figure 15. V_{BS} = 20V Supply Current vs. Temperature

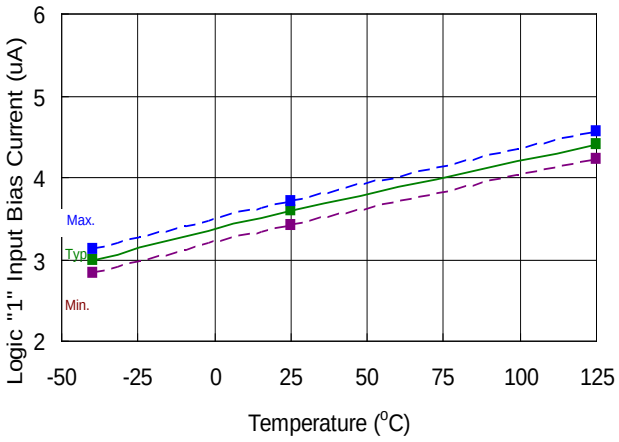


Figure 16. Logic “1” Input Bias Current vs. Temperature

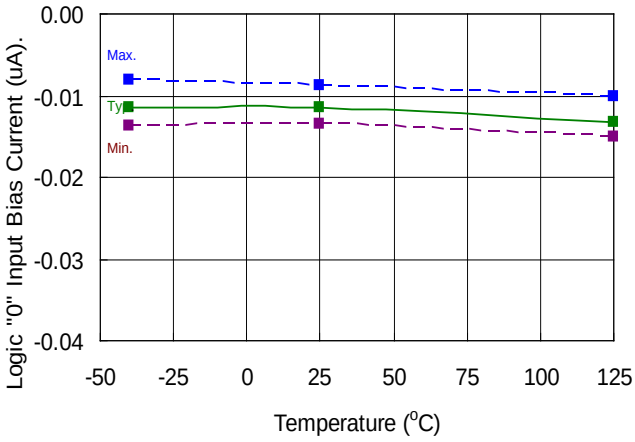
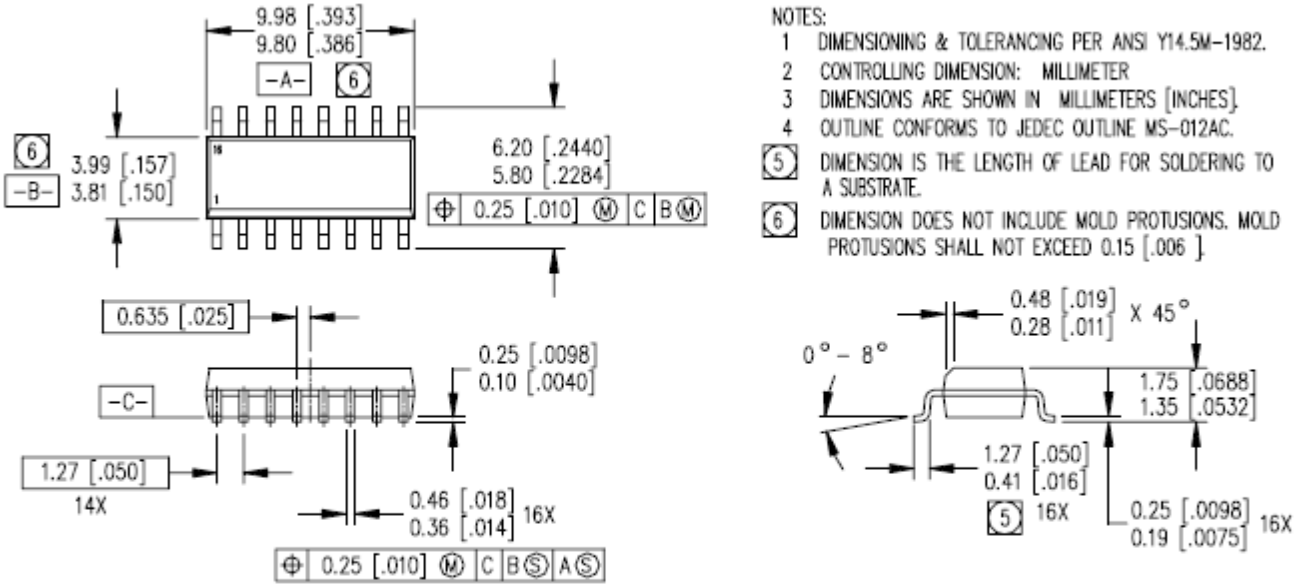
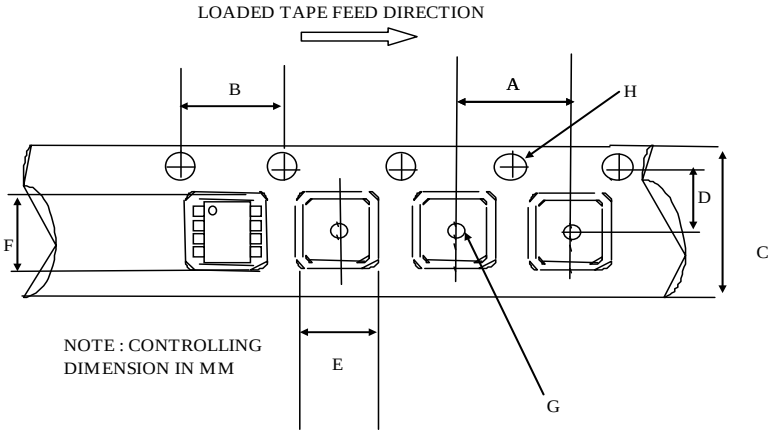


Figure 17. Logic “0” Input Bias Current vs. Temperature

Package Details: SOIC16N

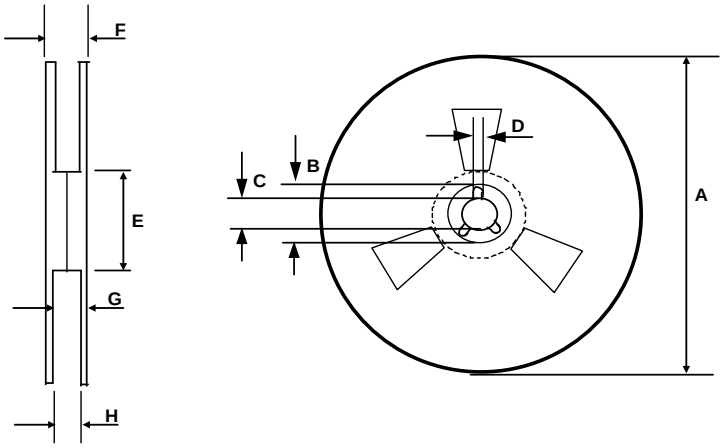


Package Details: SOIC16N, Tape and Reel



CARRIER TAPE DIMENSION FOR 16SOICN

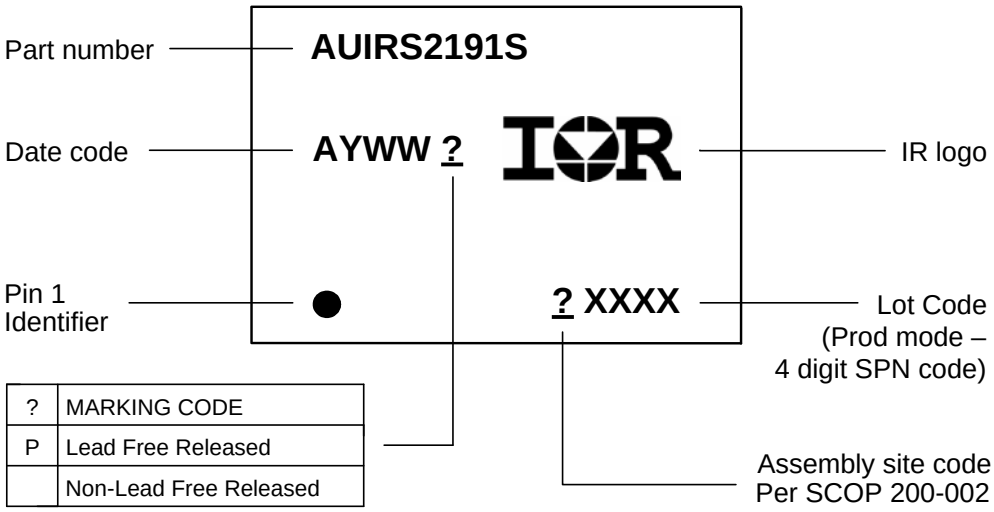
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2191S	SOIC16N	Tube/Bulk	45	AUIRS2191S
		Tape and Reel	***2500***	AUIRS2191STR

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Revision History

Date	Comment
Feb. 5, 2009	Original document
Jan. 22, 2010	Added timing, Iqxx, input bias tri-temp graphs; updated min. timing parameter; updated actual part marking;
Jan. 27, 2010	Io+ and Io- unit corrected (from uA to A) Test condition changed (from 7V to 9.8V) in table of Stat el char, Vih and Vil. Iqcc and Iqbs specified also at 18V and at 20V of supply voltage. Tr and tf typ and max changed. Abs Max Rat: Vs Max changed from VB+20 to VB+0.3 Stat Elec Char: "IIN and IO parameters are referenced to COM" sentence modified in heading. I_o changed from 0 to 2 mA in V_{OH} and V_{OL} test conditions. I/O Pin Eq Cir Diag: clamp voltage values changed from 25V to 20V. Changed MT max to 25nS from 15nS; added temperature range spec: -40°C ≤ Tj ≤ 125°C on top of statics and dynamic electrical characteristics tables.
Feb. 01, 2010	Added typ. and max. value for Iqcc_18, Iqcc_20, Iqbs_18, Iqbs_20, and their tri-temp graphs; added guranteed by design note for IO+/-
Mar. 15, 2010	Added CDM ESD level to qual info page; Corrected Voh max. spec to 3.3V with test condition of I0=2mA.
May 26th, 2010	I_{IN+} Typ and max change; Io+ and Io- min added; tR and tF max change; Iqcc20 max = 2500uA Ton max = 175ns, Toff max = 175ns.
Jun 08th 2011	V_{BSUV-} change from 9.0V down to 8.8V
Oct. 26, 2011	Added "Lead-Free and RoHS Compliant" to front page, updated latch up rating on qual info page; updated "Important Notice" with latest version 2.
Oct. 27, 2011	Added NTSOA
Jun. 11, 2012	V_{OH} parameter spitted into V_{OH_2mA} and V_{OH_20mA}
Oct 24th, 2012	negVs SOA change introducing tri-temp info.
Jan. 18, 2013	Page1: removed Plasma Display from typical application; Page 3 – removed "plasma display" from description statement; Page 4 –removed note II from qual information page

