Hard Disk Pulse Detector

GENERAL DESCRIPTION

The XR-541 is a disk drive Pulse detector designed for use with RLL and MFM coding schemes. Signals from the read/write preamplifier are qualified by an amplitude verifying gating threshold before constant width pulses are output.

The XR-541 is available in 24 Pin Plastic DIP, JEDEC S.O., and 28 Pin PLCC packages. It employs +5V and +12V supplies.

FEATURES

RLL and MFM Decoding
High Performance AGC Preamplifier
Adjustable Detection Threshold
Wide Dynamic Range
Compatible with Embedded Servo
Separate Analog and Digital Grounds
TTL Level Output and Control
Replaces SS1541 Read Data Processor

## APPLICATIONS

Winchester Disk Drives
Removable Cartridge Disk Drives

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage
V_{CC}	6.5V
V_{DD}	14.0V
Storage Temperature	-65°C to I50°C
Operating Junction Temperature	150°C
Power Dissipation	
24 Pin Plastic DIP	1W
Derate Above 25°C	8mW/°C
24 Pin JEDEC SO	1W
Derate Above 25°C	8mW/°C
28 Pin PLCC	1W
Derate Above 25°C	8mW/°C
TTL Input Voltage	-0.3V to 5.5V
Differential Input Signal	+/-3.3V

PIN ASSIGNMENT
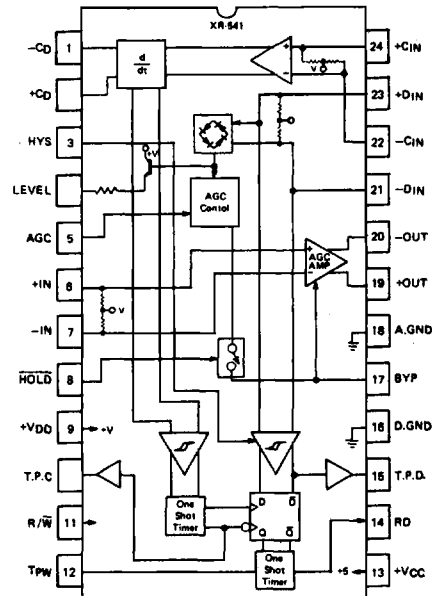
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-541-1CP	24 Pin DIP/1ns	0°C to 70°C
XR-541-1CJ	28 Pin PLCC/1ns	0°C to 70°C
XR-541-1D	24 Pin S.O./1ns	0°C to 70°C
XR-541-3CP	24 Pin DIP/3ns	0°C to 70°C
XR-541-3CJ	28 Pin PLCC/3ns	0°C to 70°C
XR-541-3D	24 Pin S.O./3ns	0°C to 70°C

SYSTEM DESCRIPTION

Signal from the disk head preamplifier are A.C. coupled into the XR-541. A low pass filter may be employed here to reduce system bandwidth and noise. The input amplifier is AGC controlled, allowing reliable operation with signal levels ranging from 20 mV to 660 mV p-p. A low pass filter removes unwanted components as the signal enters the differentiator and level detection threshold circuitry. Only when the signal rises above this user adjustable threshold is the output one-shot timer enabled.

Detection threshold is set by the voltage on the HYS Pin. Test points are provided for alignment of the delays from the clock input and the gating flip-flop. Dual grounds reduce coupling between the digital sections and the low level signal inputs.

XR-541

DC ELECTRICAL CHARACTERISTICS
Test Conditions: $T_A = 25°$, $V_{CC} = 5V$, $V_{DD} = 12V$, $R/\overline{W}$= High (>2.0V). Unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current		4	14	mA	V_{CC} = 5.5V
I_{DD}	Supply Current		50	70	mA	V_{DD} = 13.2V
P_D	Power Dissipation		600	730	mW	
DIGITAL SIGNALS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input "Low" Current	-0.4			mA	V_{IL}= 0.4V
I_{IH}	Input "High" Current			100	µA	V_{IH}=2.4V
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 4mA $\overline{RD}$ Output
V_{OH}	Output "High" Voltage	2.4			V	I_{OH}=-0.4mA $\overline{RD}$ Output
AGC AMPLIFIER						
$A_V$min	Minimum Gain		0.1	4	V/V	Differential V_{OUT} from 1.0V
A_{Vmax}	Maximum Gain	83	250		V/V	to 2.5Vp-p
R_{IN}	Differential Input Resistance		5		KΩ	
C_{IN}	Differential Input Capacitance			10	pF	
Z_{IN}	Common Mode Input Impedance		1.8		KΩ	$R/\overline{W} \geq 2.4V$ BothSides
			250	500	Ω	$R/\overline{W} \leq 0.8V$ Both Sides
e_{ni}	Input Noise Voltage			30	nV/√Hz	Az=maximum:15MHz bandwidth
BW	Preamplifier Bandwidth	30	60		MHz	Av = maximum: -3dB point
CMRR	Common Mode Rejection Ratio	40	60		dB	V_{IN} = 100mVp-p at 5 MHz. Av = Max.
PSRR	Power Supply Rejection Ratio	30	40		dB	ΔV_{CC} or ΔV_{DD} = 100mV
Vout	Output Voltage Swing	3.0	6		Vp-p	Vp-p at 5 MHz. Av = Max $R_L \geq 600Ω$ Differential. V_{AGC} = 5.5V
Iout	Output Current Swing	13.2	14		mA	
R_O	Output Resistance			32	Ω	
C_O	Output Capacitance			15	pF	
V_{DIN} $\overline{V_{AGC}}$	V(DIN+) - V(DIN-) Voltage Swing -vs-V_{AGC}	370	480	560	mVpp/ V	V_{IN} From 30mVp-p to 550mVp-p V(DIN+) -V(DIN-) From 500Vp-p to 1.5Vp-p
ΔVDIN $\overline{V_{AGC}}$	V(DIN+) - V(DIN-) Change		1	8	%	VAGC = constant. V_{CC} 110%, V_{DD}±10%. T_AFrom 0°C to 70°C.
I_{AGC}	AGC Fast Charge Current	1.3	1.6	2.0	mA	V(DIN+) - V(DIN-) = 1.6V
I_{AGC}	AGC Slow Charge Current	140	180	220	µA	V(DIN+) - V(DIN-) = 1.6V. VAGC
	Fast to Slow Attack Switching Point		1.25		—	$\dfrac{V_{DIN} \text{ (initial)}}{V_{DIN} \text{ (Final)}}$
	AGC Capacitor Discharge Current		4.5		µA	Operate (HOLD="High")V_{DIN}=0
		-200	-	200	nA	Hold (HOLD="Low")V_{DIN}=0
t_A	AGC Attack Time		4		µs	Note 1.
t_D	AGC Decay Tvm		50		µs	Note 2.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
WINDOW THRESHOLD COMPARATOR						
R_{IN}	Differential Input Resistance	5		11	$K\Omega$	
C_{IN}	Differential Input Capacitance			6	pF	
Z_{IN}	Common Mode Input Impedance		2		$K\Omega$	V_{HYS} = 0V. R(DIN+ to DIN-)$\leq$1.5KΩ
V_{OS}	Threshold Comparator Offset Voltage	-10		10	Mv	
	Peak Window Threshold Voltage -vs-V_{HYS}	0.16	0.22	0.25	V/v	V_{DIN} Referred. V_{HYS} From 1V to 3V.
I_{HYS}	HYS Pin Input Current	-20		0	μA	V_{HYS} From 1V to 3V.
V_{LEVEL}	V_{LEVEL} -vs- V_{DIN}	1.5	2.0	2.5	V/Vp-p	V_{DIN} From0.6V to 1.3Vp-p 10KΩ Load to Ground
I_{LEVEL}	LEVEL Maximum Output Current	3.0			mA	
$R_O(LEVEL)$	LEVEL Output Resistance		180		Ω	I_{LEVEL} = 500mA
V_{OLD}	Test Point D Output Low Voltage	V_{DD} -4		V_{DD} -2.8	V	$|IOL|\leq$500mA
V_{OHD}	Test Point D Output High Voltage	V_{DD} -2.5		V_{DD} -1.8	V	$I_{OH}\leq$ 500mA
DIFFERENTIATOR						
R_{IN}	Differential Input Resistance	5.8		11	$K\Omega$	$|V_{CIN}|$ = 100mVp-p at 2.5 MHz
CIN	Differential Input Capacitance			6	pF	$|V_{CIN}|$= 100mVp-p at 2.5 MHz
A_{VD}	Differentiator Preamp Gain	1.7	1.8	2.2	V/V	V_{DIF}/V_{CIN}: R_{DIF} = 2kΩ
Z_{IN}	Common Mode Input Impedance		2		$K\Omega$	
V_{OS}	Differentiator Offset Voltage	-10		10	mV	Capacitive Differentiator Network
I_D	Differentiator Drive Current	11.3			mA	
V_{OLC}	Test Point "C" Output Low Voltage		V_{DD}-3.0		V	$I_{OL}\leq$ 500mA
V_{OC}	Test Point "C" Output		400		mVp-p	$I_{OL},I_{OH}\leq$500mA
t_c	Test Point "C" Pulse Width		30		ns	$I_{OH}\leq$ 500mA
CONTROL TIMING						
T_{W-R}	Write to Read Transition Time	1.2	2	3.0	μs	Transition to High R_{IN}.
T_{R-W}	Read to Write Transition Time		0.25	1.0	μs	
T_{R-H}	Read to Hold Transition Time			1.0	μs	
DYNAMIC DATA CHARACTERISTICS						
Additional Test Conditions: V_{CIN}, V_{DIN}=1.0Vp.p2.5MHz Sine Wave,V_{HYS}=1.8V,C_D=65pF, R_D=100Ω,C_{pw}=60pF, $\overline{RD}$ is loaded with 4KΩ to +V_{cc} & 10pF to GND. Refer to Figure 2, Figure 3 and Figure 4						
T_{D1}	D Flip-Flop Set Up Time	0			ns	Delay from V_{DIN} Passing threshold to V_{DIF} Peaking
T_{D3}	Propagation Delay		65	110	ns	Delay from V_{DIN} = V_{CIN} Peaking to $\overline{RD}$ out.
PP	Pulse Pairing			1 3	ns ns	XR-541-1 (Note 3) XR-541-3 (Note 3)

XR-541

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
T_{PW}	Output Data Pulse Width Accuracy	-15		15	%	Error from $T_{PW}= 0.67\ C_{PW}$: C_{PW} from 50pF to 200pF
T_r	Output Rise Time		7	14	ns	To $V_{OH} = 2.4V$
T_f	Output Fall Time		6	18	ns	To $V_{OL} = 0.4V$

NOTE 1: Time from Write to Read transition to V_{OUT} reaching 110% of final value using $400mV_{p-p}$ 2.5 MHz sine wave.
(See Figure 1A, Figure 1B.)

NOTE 2: Time from Vin dropping from $300mV_{p-p}$ to $150mV_{p-p}$ to V_{OUT} recovering within 90% of final value using 2.5MHz sine wave.
(See figure 1C, Figure 1D.)

NOTE 3: Pulse Pairing as defined as: as shown in Figure 3.

$$\frac{1}{2}\left[\frac{Tpp1 - Tpp2}{Tpp1 + Tpp2}\right]$$

Circuit is as shown in Figure 4. $V_{CIN} = V_{DIN} = 1Vp\text{-}p$ 2.5 MHz sine wave.

(A)

R/W Input

AGC Attack Time

t_a

(B)

110%

V_{OUT}

(C) AGC Decay Time
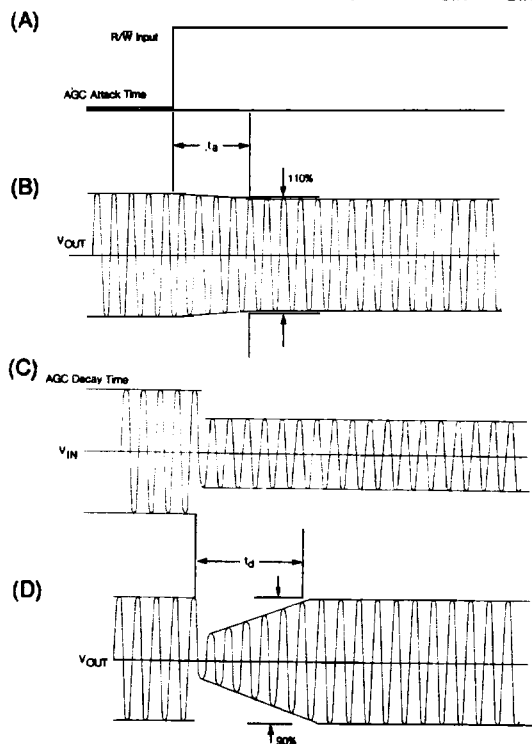
V_{IN}

t_d

(D)

V_{OUT}

90%

Figure 1. XR-541 AGC Characteristics
(A) R/W Control Input
(B) AGC Attack Time
(C) Stepped Input Test Signal
(D) AGC Decay Tim

XR-541 Pin Description (28 Pin PLCC)

Pin	Symbol	Description
1,2	$-C_D$, $+C_D$	**Differentiator Network Terminals.**
3	HYS	**Window Gating Hysteresis.** Window gating comparator level is adjusted by this pin.
5	Level	**AGC Amplifier Level Output.** Rectified Analog signal is output for closing the AGC loop.
6	AGC	**AGC Charge Current Input.** Determins if AGC bypass capacitor is charging at the fast rate, slow rate, or is discharging.
7,8	+IN, -IN	**AGC Preamplifier Input.** Signal input from external read preamplifier.
9	HOLD	**AGC Gain Hold.** When low, AGC Amplifier Gain is held constant.
10	V_{DD}	**+12V Supply.**
11	T.P.C.	**Test Point for monitoring "Clock" path.**
12	R/W	**Read/Write Control.** A TTL low places the device in standby mode.

13	T_{PW}	**One Shot Timing Select.** Output pulse time is set using a capacitor to +VCC.
15	V_{CC}	**+5V Supply.**
16	$\overline{RD}$	**Read Data Output.** Active low digital output.
18	T.P.D.	**Test Point for monitoring "Data" path.**
19	DGND	**Digital Ground.**
20	BYP	**AGC Control Pin.** A capacitor to ground sets AGC time constants.
21	AGND	**Analog Ground.**
22,23	+OUT,-OUT	**AGC Amplifier Output.**
24,27	$-D_{IN}, +D_{IN}$	**"Data" path Input.**
26,28	$-C_{IN}, +C_{IN}$	**"Clock" path Input.**

CIRCUIT OPERATION

Standby/Write Mode

During Data Write operations (R/$\overline{W}$ low), the XR-541 AGC input impedance is lowered to reduce the time constant caused by the input coupling capacitors, which limits the speed of Write to Read recovery. The AGC is reset to maximum gain, and the digital circuitry is disabled.

Read Mode

AGC

The analog head signal is A.C. coupled from the head preamplifier to the AGC inputs. The signal is amplified and output through low impedance drivers. Nominal peak output voltage is user-determinable by applying a voltage to the AGC Pin, according to the relationship:

$$V_{AGCOUT} \text{ (p-p)} = 0.48 \ V_{AGC}$$

Where V_{AGCOUT} is the peak to peak pre-amplifier output voltage and V_{AGC} is the DC control voltage on the AGC pin.

For most applications, a peak to peak output voltage of 2 volts is ideal.

AGC gain is held constant between pulses by the capacitor on the BYP Pin. Two rates of current charge this capacitor depending on the relative amplitude. A high level, 1.8mA, provides rapid attack characteristics needed for fast Write to Read recovery time. A low level, 180µA, allows slower gain tracking adjustment and reduces third order harmonic generation.

Preamplifier output is passed through a multiple order Bessel lowpass filter and applied to the Clock and Data inputs. For some applications, different delays are required for the Clock and Data inputs. For this reason, the XR-541 separates these inputs; many applications do not need separate timing and Clock Inputs and Data Inputs are directly connected. Internal path delays are carefully matched.

Hold

In the "Hold" mode, (Hold = low) no current charges C_{BYP} The constant voltage on C_{BYP} keeps the amplifier gain constant at the present valve. This feature is intended to facilitate embedded servo applications, where fixed gain is essential for amplitude comparison used in head positioning.

Data Path

Amplified signal output from the filter is applied to the +D_{IN}/-D_{IN} terminals to allow amplitude qualification of the signal and AGC loop closure. When this input amplitude exceeds the hysteresis threshold, the D flip-flop data inputs are toggled.

These inputs will not change state again until the signal changes direction and crosses the hysteresis threshold on the opposite side of 'zero'. See figures 2a, 2d. Hysteresis comparator output is buffered and appears at T.P.D. for testing or evaluation purposes.

Clock Path

Amplified signal output from the filter is applied to the +C_{IN}/-C_{IN} terminals to determine precise data peak timing. The clock path consists of a differentiator, a zero crossing comparator, and a one-shot timer.

The differentiator phase shifts the incoming waveform, converting data peaks into zero crossings. A capacitor, C_D- typically 20pF to 150pF, determines the amount of

phase shift. Although a phase shift of 90° across all input frequencies would be ideal, this implies an infinte bandwidth. Noise considerations usually dictate adding a resistor, and occasionally an inductor, to limit the differentiator noise bandwidth. With a series RLC network, the differentiator transfer function becomes:

$$A_V = \frac{-2000\ Cs}{LCs^2 + (R + R_1)\ Cs + 1}$$

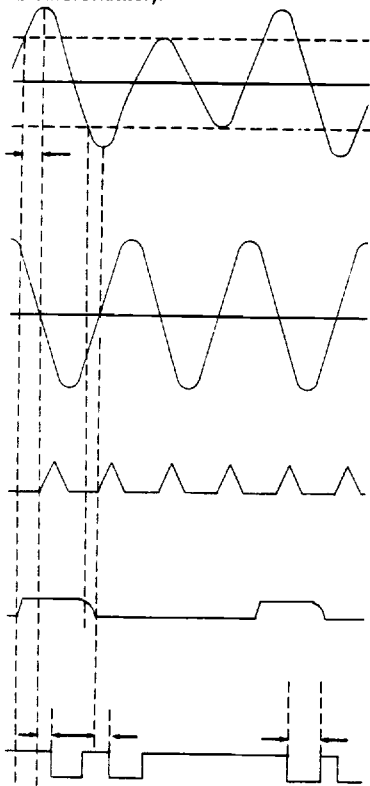where s = jw and R_1 = 92Ω (internal impedance of the differentiator).

Figure 2. XR-541 Timing Diagram

(A). AGC Amplifier Output (also V_{CIN} & V_{DIN}) showing ±window comparator thresholds.
(B). Differentiator Circuit waveform (V_{CD}).
(C). Test Point "C" Output. Flip-flop clock input.
(D). Test Point "D" Output. Flip-flop D input.
(E). $\overline{RD}$ Output.

Differentiator output is applied to a zero crossing comparator. This comparator fires a bi-directionally triggered one-shot timer whose output is used as the clock of the D flip-flop. Buffered one-shot output appears at T.P.C. for alignment purposes.

Data Output

After the signal is time and amplitude qualified, the D flip-flop toggles. This fires a one shot timer which outputs constant width active low digital data pulse, $\overline{RD}$. The period of this pulse is programmed by a capacitor, Cpw, from pin Tpw to $+V_{CC}$ and is proportioned to this capacitor by the formula:

$$Tpw = 0.67\ Cpw$$

Where Tpw is in ns and Cpw is in pF.
Recommended Cpw values range from 50pF to 200 pf.

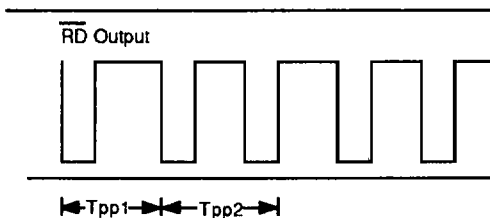The active low $\overline{RD}$ output has a fan out of 1 TTL gate.

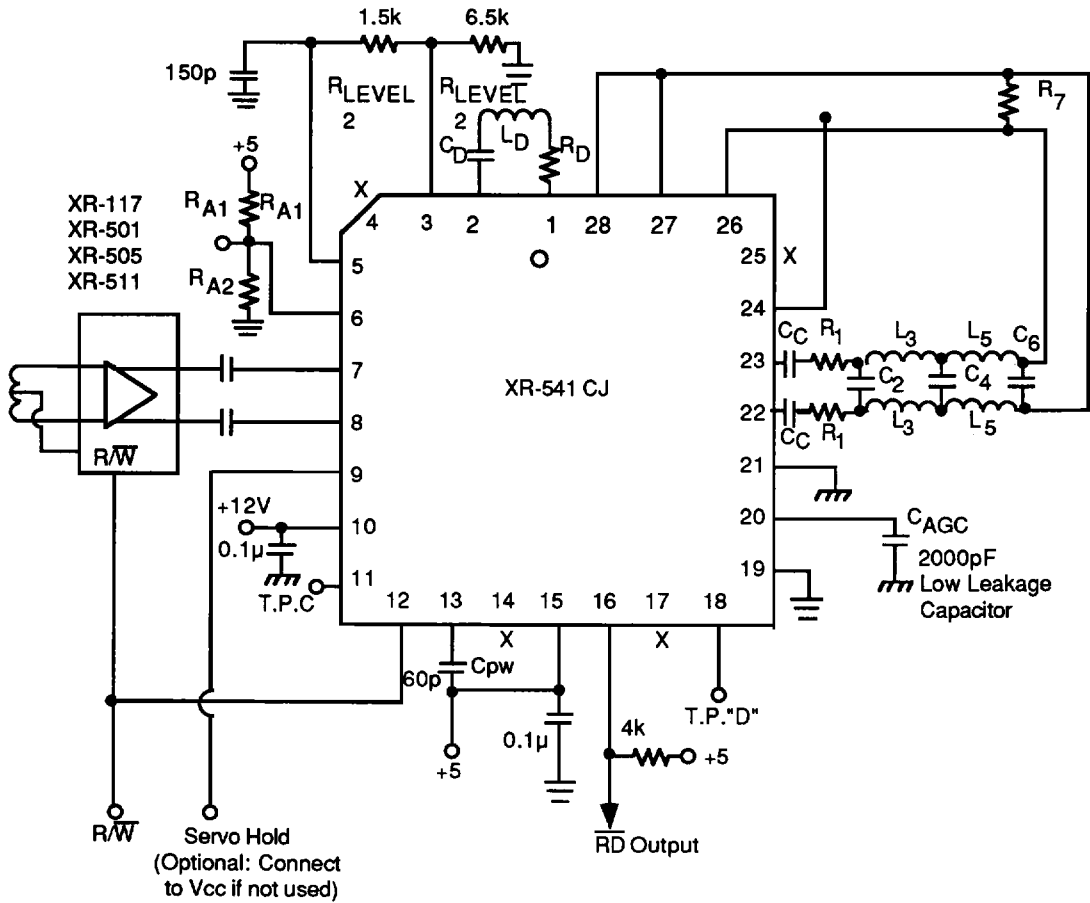**Figure 3. Pulse Pairing Definition**

Figure 4. XR-541 Application Circuit

XR-541

Pin	Signal		Pin	Signal
1	−C_D		24	+C_IN
2	+C_D		23	+D_IN
3	HYS		22	−C_IN
4	LEVEL		21	−D_IN
5	AGC		20	−OUT
6	+IN		19	+OUT
7	−IN		18	A GND
8	HOLD		17	BYP
9	+V_DD		16	D GND
10	T.P.C		15	T.P.D
11	R/W̄		14	R̄D̄
12	TPW		13	+V_CC

XR-541CP

XR-541CJ (PLCC) Pinout