

Quad channel high side driver for automotive applications

Features

| | | |
|-----------------------------------|------------|-----------------|
| Max transient supply voltage | V_{CC} | 41V |
| Operating voltage range | V_{CC} | 4.5 to 28V |
| Max on-state resistance (per ch.) | R_{ON} | 50 m Ω |
| Current limitation (typ) | I_{LIMH} | 27 A |
| Off-state supply current | I_S | 2 $\mu A^{(1)}$ |

1. Typical value with all loads connected.

■ General

- Inrush current active management by power limitation
- Very low stand-by current
- 3.0 V CMOS compatible inputs
- Optimized electromagnetic emissions
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC european directive

■ Diagnostic functions

- Open drain status output
- On-state open-load detection
- Off-state open-load detection
- Output short to V_{CC} detection
- Overload and short to ground (power limitation) indication
- Thermal shutdown indication

■ Protections

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Over temperature shutdown with auto restart (thermal shutdown)
- Reverse battery protected (see [Application schematic^{\(1\)} on page 22](#))



PowerSSO-24

- Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads

Description

The VNQ5E050K-E is a quad channel high-side driver manufactured in the ST proprietary VIPower™ M0-5 technology and housed in the tiny PowerSSO-24 package.

The VNQ5E050K-E is designed to drive automotive grounded loads delivering protection, diagnostics and an easy 3 V and 5 V CMOS compatible interface with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, over temperature shut-off with auto restart and over-voltage active clamp.

A dedicated active low digital status pin is associated with every output channel in order to provide *Enhanced* diagnostic functions including fast detection of overload and short-circuit to ground, over temperature indication, short-circuit to V_{CC} diagnosis and ON & OFF-state open-load detection.

The diagnostic feedback of the whole device can be disabled by pulling the STAT_DIS pin up, thus allowing wired-ORing with other similar devices.

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1 Block diagram and pin configuration

Figure 1. Block diagram

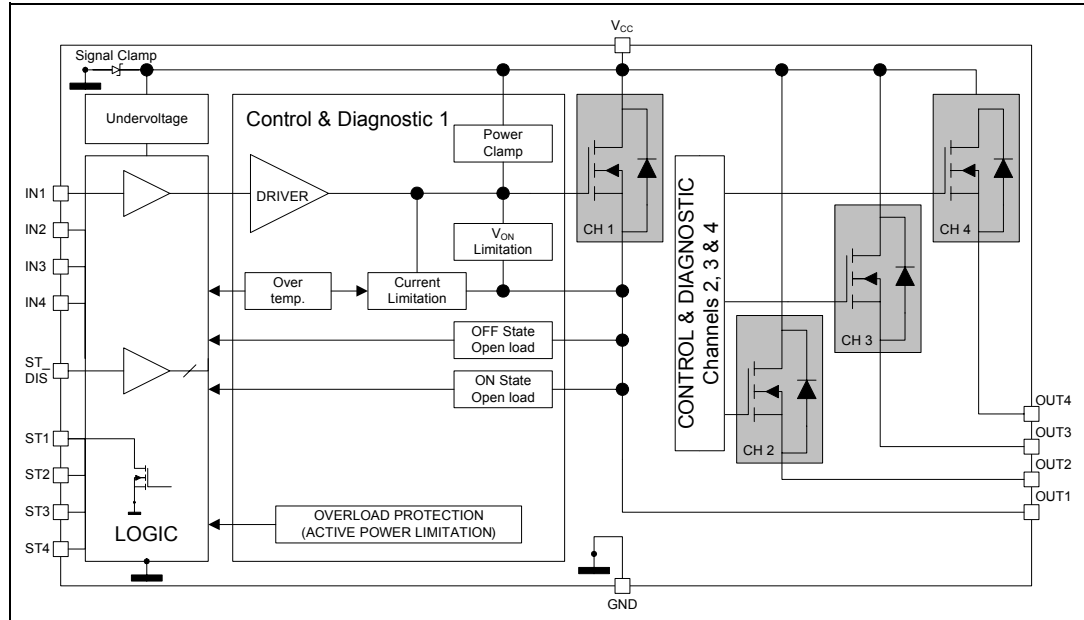


Table 1. Pin function

| Name | Function |
|-----------------|--|
| V _{CC} | Battery connection. |
| OUTPUTn | Power output. |
| GND | Ground connection. Must be reverse battery protected by an external diode/resistor network. |
| INPUTn | Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state. |
| STATUSn | Open drain digital diagnostic pin. |
| STAT_DIS | Active high CMOS compatible pin, to disable the STATUS pin. |

Figure 2. Configuration diagram (top view)

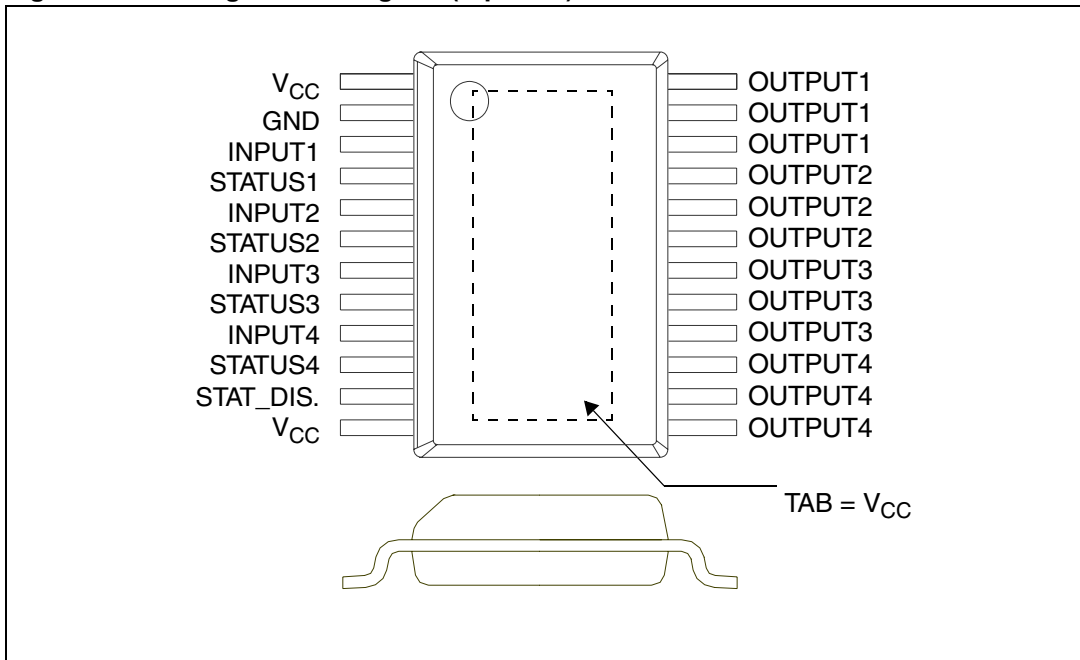
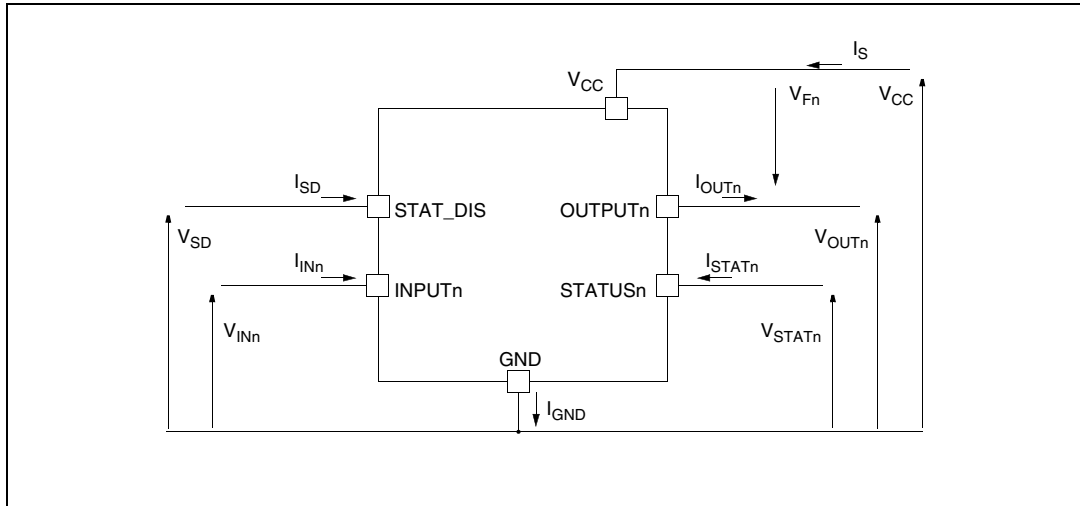


Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Status | N.C. | Output | Input | STAT_DIS |
|------------------|-------------|------|-------------|-----------------------|-----------------------|
| Floating | X | X | X | X | X |
| To ground | Not allowed | X | Not allowed | Through 10KΩ resistor | Through 10KΩ resistor |

2 Electrical specifications

Figure 3. Current and voltage conventions⁽¹⁾



1. $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|---|--------------------|------|
| V_{CC} | DC supply voltage | 41 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 15 | A |
| I_{IN} | DC input current | +10/-1 | mA |
| I_{STAT} | DC status current | +10/-1 | mA |
| I_{STAT_DIS} | DC status disable current | +10/-1 | mA |
| E_{MAX} | Maximum switching energy (single pulse) ($L = 3\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_{OUT} = I_{limL}(\text{Typ.})$) | 104 | mJ |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|------------------|---|-------------|------|
| V _{ESD} | Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF) | | |
| | – Input | 4000 | V |
| | – Status | 4000 | V |
| | – STAT_DIS | 4000 | V |
| | – Output | 5000 | V |
| | – V _{CC} | 5000 | V |
| V _{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T _j | Junction operating temperature | -40 to 150 | °C |
| T _{stg} | Storage temperature | - 55 to 150 | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|---|-------------------------------|------|
| R _{thj-case} | Thermal resistance junction-case (max) (with one channel ON) | 2.8 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient (max) | See Figure 36 | °C/W |

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$, unless otherwise stated.

Table 5. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|--------|-----------------------|------------------------|----------------|
| V_{CC} | Operating supply voltage | | 4.5 | 13 | 28 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 4.5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| R_{ON} | On-state resistance ⁽¹⁾ | $I_{OUT} = 2\text{ A}$; $T_j = 25^\circ\text{C}$ $I_{OUT} = 2\text{ A}$; $T_j = 150^\circ\text{C}$ $I_{OUT} = 2\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25^\circ\text{C}$ | | | 50 100 65 | mΩ mΩ mΩ |
| V_{clamp} | Clamp voltage | $I_S = 20\text{ mA}$ | 41 | 46 | 52 | V |
| I_S | Supply current | Off-state; $V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = 0\text{ V}$; $T_j = 25^\circ\text{C}$ On-state; $V_{IN} = 5\text{ V}$; $V_{CC} = 13\text{ V}$; $I_{OUT} = 0\text{ A}$ | | 2 ⁽²⁾ 8 | 5 ⁽²⁾ 14 | μA mA |
| $I_{L(off1)}$ | Off-state output current ⁽¹⁾ | $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25^\circ\text{C}$ $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125^\circ\text{C}$ | 0 0 | 0.01 | 3 5 | μA μA |
| V_F | Output - V_{CC} diode voltage ⁽¹⁾ | $-I_{OUT} = 2\text{ A}$; $T_j = 150^\circ\text{C}$ | | | 0.7 | V |

1. For each channel.

2. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 13\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|--------------------------------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $R_L = 6.5\Omega$ (see Figure 6.) | | 20 | | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L = 6.5\Omega$ (see Figure 6.) | | 35 | | μs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L = 6.5\Omega$ | | See Figure 26. | | V/μs |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L = 6.5\Omega$ | | See Figure 28. | | V/μs |
| W_{ON} | Switching energy losses during t_{won} | $R_L = 6.5\Omega$ (see Figure 6.) | | 0.19 | | mJ |
| W_{OFF} | Switching energy losses during t_{woff} | $R_L = 6.5\Omega$ (see Figure 6.) | | 0.25 | | mJ |

Table 7. Status pin ($V_{SD}=0$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|------------------------------|--|------|------|------|---------------|
| V_{STAT} | Status low output voltage | $I_{STAT} = 1.6 \text{ mA}$, $V_{SD}=0\text{V}$ | | | 0.5 | V |
| I_{LSTAT} | Status leakage current | Normal operation or $V_{SD}=5\text{V}$, $V_{STAT} = 5\text{V}$ | | | 10 | μA |
| C_{STAT} | Status pin input capacitance | Normal operation or $V_{SD}=5\text{V}$, $V_{STAT} = 5\text{V}$ | | | 100 | pF |
| V_{SCL} | Status clamp voltage | $I_{STAT} = 1\text{mA}$ $I_{STAT} = -1\text{mA}$ | 5.5 | -0.7 | 7 | V V |

Table 8. Protections ⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--|--|---------------|---------------|---------------|--------------------|
| I_{limH} | DC short circuit current | $V_{CC} = 13\text{V}$ $5\text{V} < V_{CC} < 28\text{V}$ | 19 | 27 | 38 38 | A A |
| I_{limL} | Short circuit current during thermal cycling | $V_{CC} = 13\text{V}$ $T_R < T_j < T_{TSD}$ | | 7 | | A |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^{\circ}\text{C}$ |
| T_R | Reset temperature | | $T_{RS} + 1$ | $T_{RS} + 5$ | | $^{\circ}\text{C}$ |
| T_{RS} | Thermal reset of STATUS | | 135 | | | $^{\circ}\text{C}$ |
| T_{HYST} | Thermal hysteresis ($T_{TSD} - T_R$) | | | 7 | | $^{\circ}\text{C}$ |
| t_{SDL} | Status delay in overload conditions | $T_j > T_{TSD}$ (see Figure 4.) | | | 20 | μs |
| V_{DEMAG} | Turn-off output voltage clamp | $I_{OUT} = 2\text{A}$; $V_{IN} = 0$; $L = 6\text{mH}$ | $V_{CC} - 41$ | $V_{CC} - 46$ | $V_{CC} - 52$ | V |
| V_{ON} | Output voltage drop limitation | $I_{OUT} = 0.1\text{A}$ (see Figure 5.) $T_j = -40^{\circ}\text{C} \dots +150^{\circ}\text{C}$ | | 25 | | mV |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Open-load detection ($8V < V_{CC} < 18V$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|-----------|---------|
| I_{OL} | Open-load on-state detection threshold | $V_{IN} = 5V$ | 10 | | 70 | mA |
| $t_{DOL(on)}$ | Open-load on-state detection delay | $I_{OUT} = 0A$ (see Figure 4.) | | | 200 | μs |
| t_{POL} | Delay between INPUT falling edge and STATUS rising edge in open-load condition | $I_{OUT} = 0A$ (see Figure 4.) | 200 | 550 | 1200 | μs |
| V_{OL} | Open-load off-state voltage detection threshold | $V_{IN} = 0V$ | 2 | | 4 | V |
| t_{DSTKON} | Output short circuit to V_{CC} detection delay at turn-off | See Figure 4. | 180 | | t_{POL} | μs |
| $I_{L(off2)}$ | Off-state output current ⁽¹⁾ | $V_{IN} = 0V$; $V_{OUT} = 4V$ (see Section 3.4: Open-load detection in off-state) | -75 | | 0 | μA |
| td_vol | Delay response from output rising edge to STATUS falling edge in open-load | $V_{IN} = 0V$; $V_{OUT} = 4V$ | | | 20 | μs |

1. For each channel.

Table 10. Logic input

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|-----------------------------|-----------------------------------|------|------|------|---------|
| V_{IL} | Input low level | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9V$ | 1 | | | μA |
| V_{IH} | Input high level | | 2.1 | | | V |
| I_{IH} | High level input current | $V_{IN} = 2.1V$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1mA$ $I_{IN} = -1mA$ | 5.5 | -0.7 | 7 | V V |
| V_{SDL} | STAT_DIS low level voltage | | | | 0.9 | V |
| I_{SDL} | Low level STAT_DIS current | $V_{SD} = 0.9V$ | 1 | | | μA |
| V_{SDH} | STAT_DIS high level voltage | | 2.1 | | | V |
| I_{SDH} | High level STAT_DIS current | $V_{SD} = 2.1V$ | | | 10 | μA |
| $V_{SD(hyst)}$ | STAT_DIS hysteresis voltage | | 0.25 | | | V |
| V_{SDCL} | STAT_DIS clamp voltage | $I_{SD} = 1mA$ $I_{SD} = -1mA$ | 5.5 | -0.7 | 7 | V V |

Figure 4. Status timings

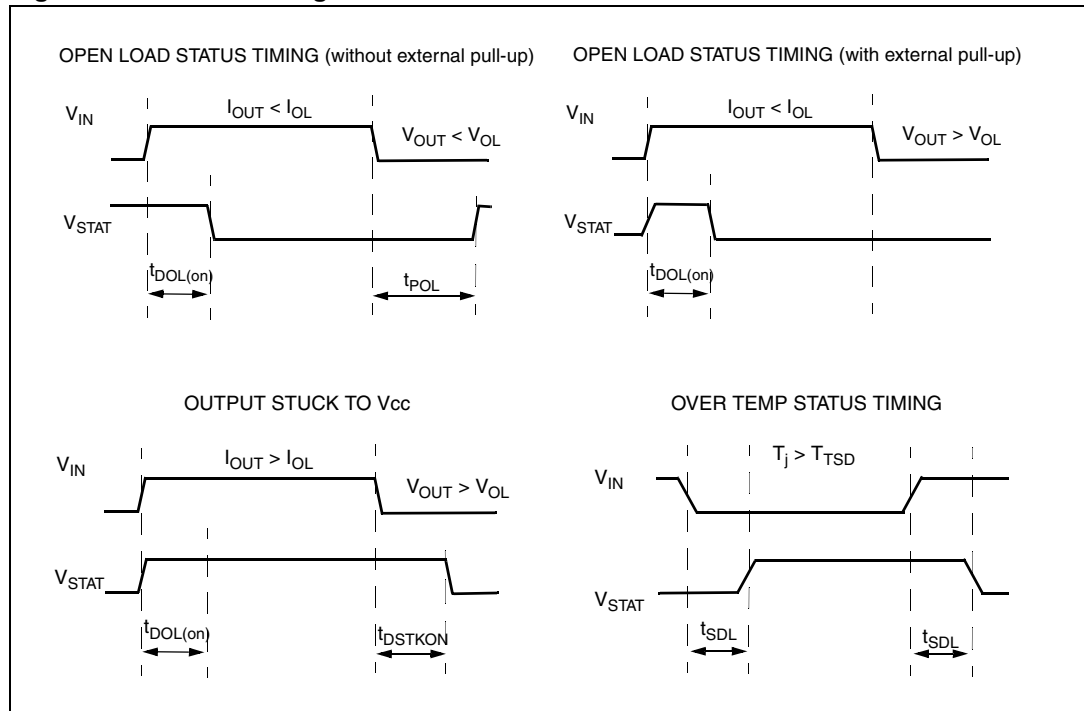


Figure 5. Output voltage drop limitation

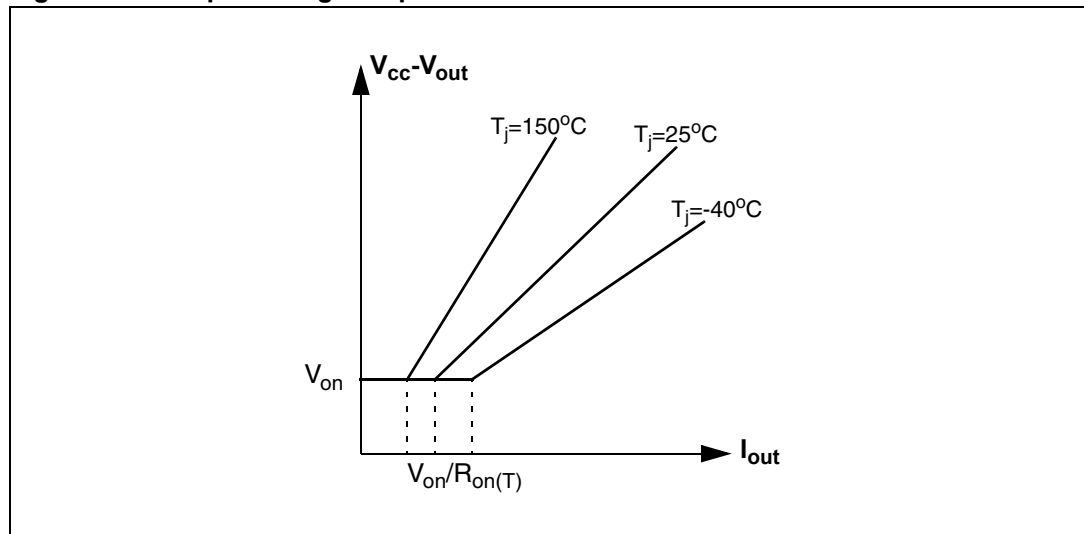


Figure 6. Switching characteristics

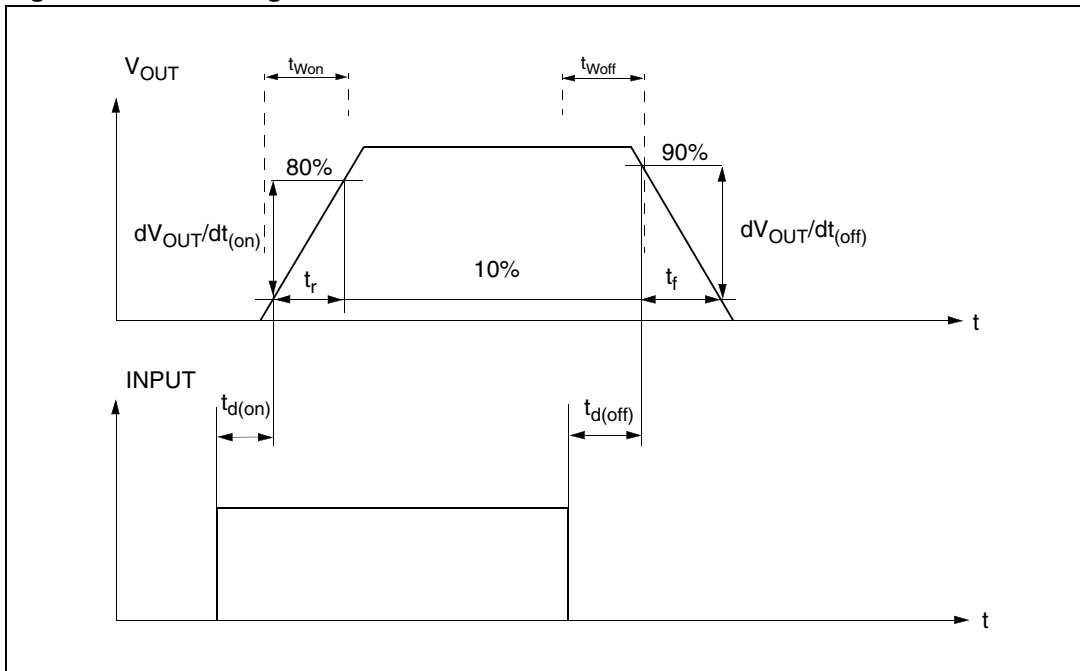


Table 11. Truth table

| Conditions | INPUTn | OUTPUTn | STATUSn ($V_{SD}=0V$) ⁽¹⁾ |
|---------------------------|--------|----------------------------------|--|
| Normal operation | L | L | H |
| | H | H | H |
| Over temperature | L | L | H |
| | H | L | L |
| Undervoltage | L | L | X |
| | H | L | X |
| Overload & short to GND | H | X | H |
| | H | (no power limitation) Cycling | L |
| | H | (power limitation) | L |
| Output voltage > V_{OL} | L | H | L ⁽²⁾ |
| | H | H | H |
| Output current < I_{OL} | L | L | H ⁽³⁾ |
| | H | H | L |

1. If the V_{SD} is high, the STATUS pin is in a high impedance.
2. The STATUS pin is low with a delay equal to t_{DSTKON} after INPUT falling edge.
3. The STATUS pin becomes high with a delay equal to t_{POL} after INPUT falling edge.

Table 12. Electrical transient requirements (part 1/3)

| ISO 7637-2: 2004(E) Test pulse | Test levels | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and impedance |
|--------------------------------------|-------------|--------|--------------------------------|-----------------------------------|--------|----------------------|
| | III | IV | | | | |
| 1 | -75 V | -100 V | 5000 pulses | 0.5 s | 5 s | 2 ms, 10 Ω |
| 2a | +37 V | +50 V | 5000 pulses | 0.2 s | 5 s | 50 μs, 2 Ω |
| 3a | -100 V | -150 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 3b | +75 V | +100 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 4 | -6 V | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b ⁽¹⁾ | +65 V | +87 V | 1 pulse | | | 400 ms, 2 Ω |

1. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 2/3)

| ISO 7637-2: 2004(E) test pulse | Test level results ⁽¹⁾ | |
|--------------------------------------|-----------------------------------|----|
| | III | IV |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b | C | C |
| 4 | C | C |
| 5b ⁽²⁾ | C | C |

1. The above test levels must be considered referred to Vcc= 13.5 V except for pulse 5b.

2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

2.4 Waveforms

Figure 7. Normal operation

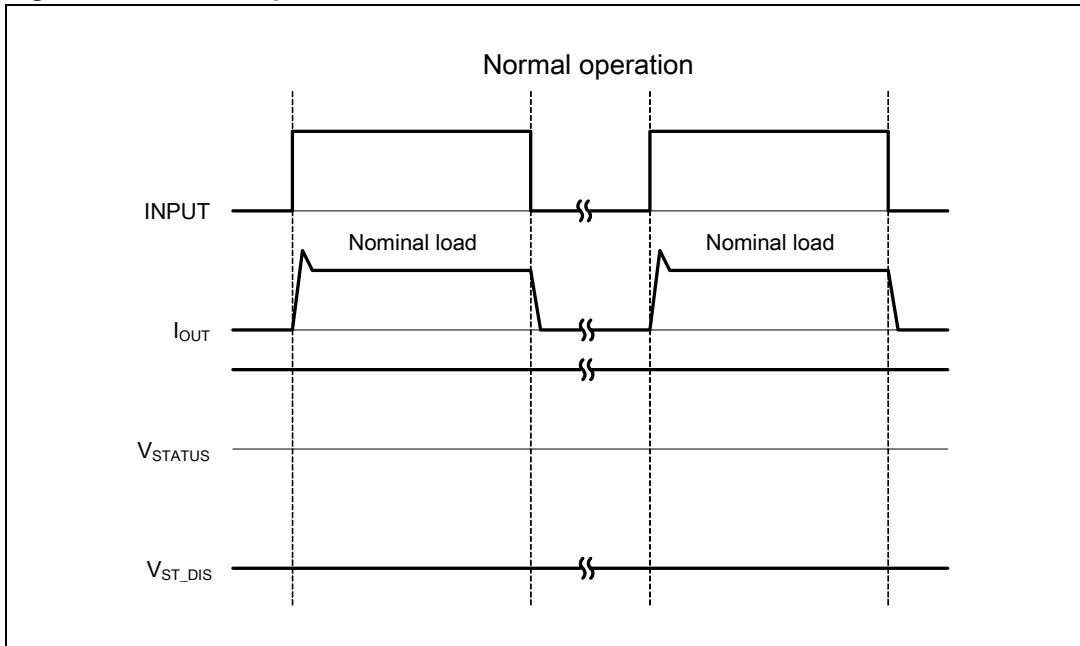


Figure 8. Undervoltage shutdown

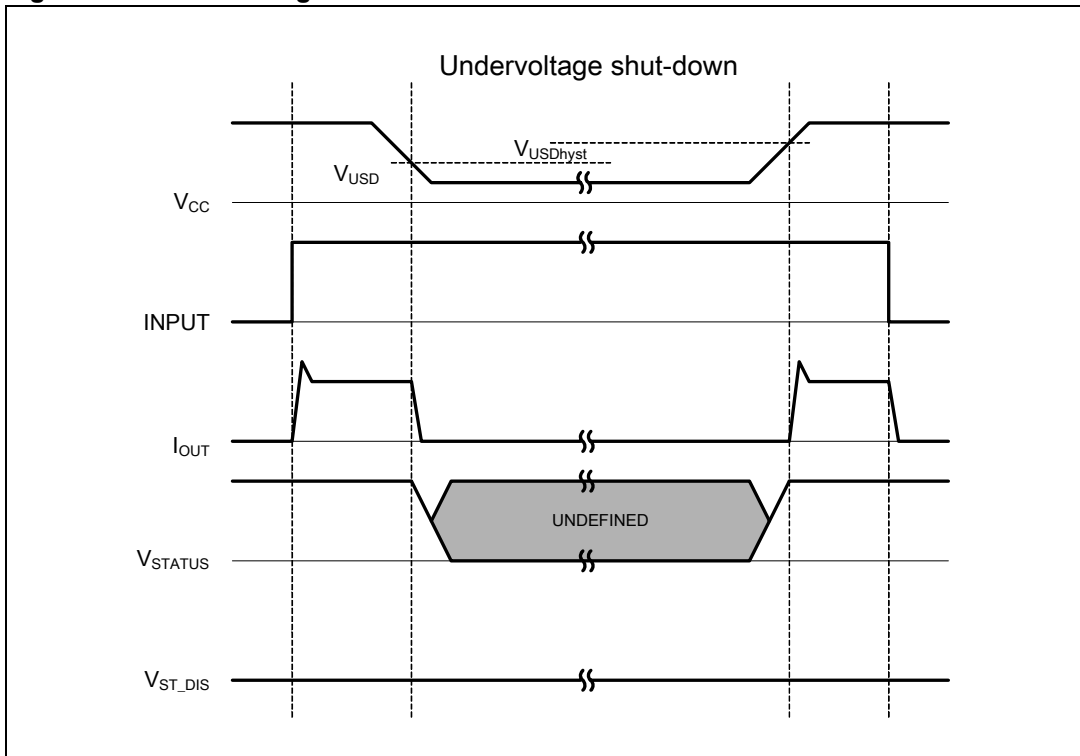


Figure 9. Overload or short to GND

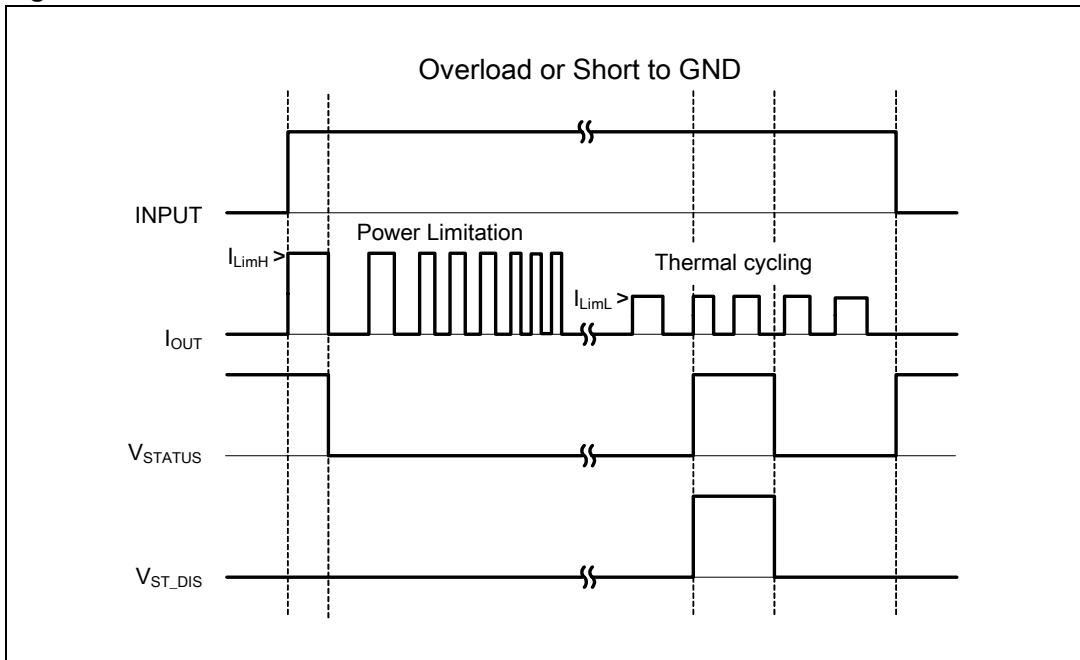


Figure 10. Intermittent overload

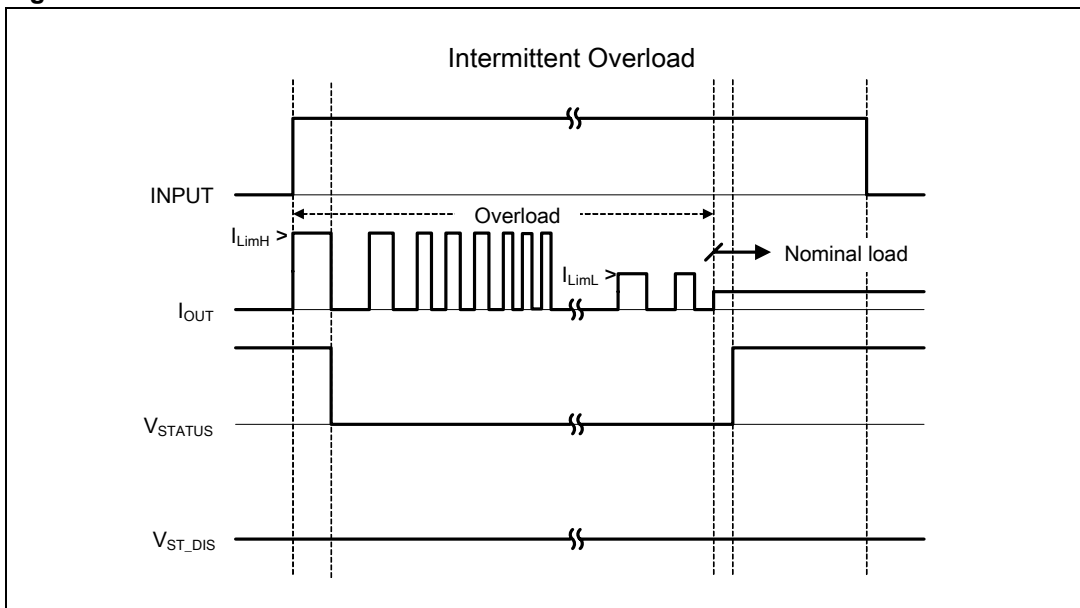


Figure 11. Open-load with external pull-up

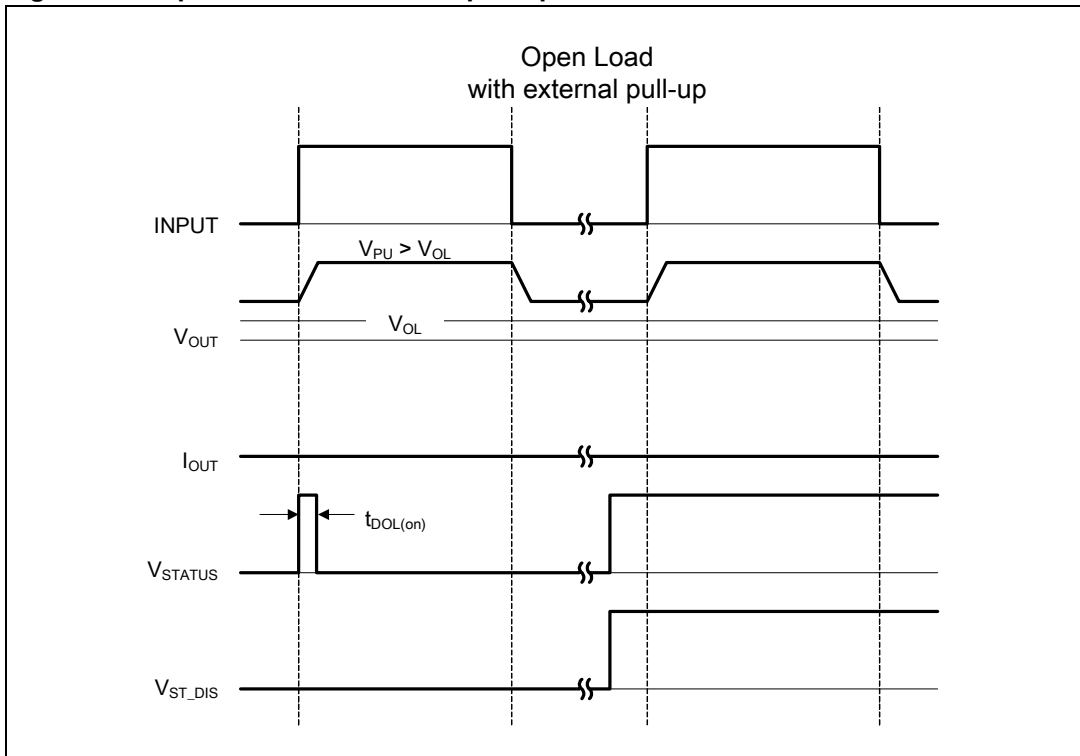


Figure 12. Open-load without external pull-up

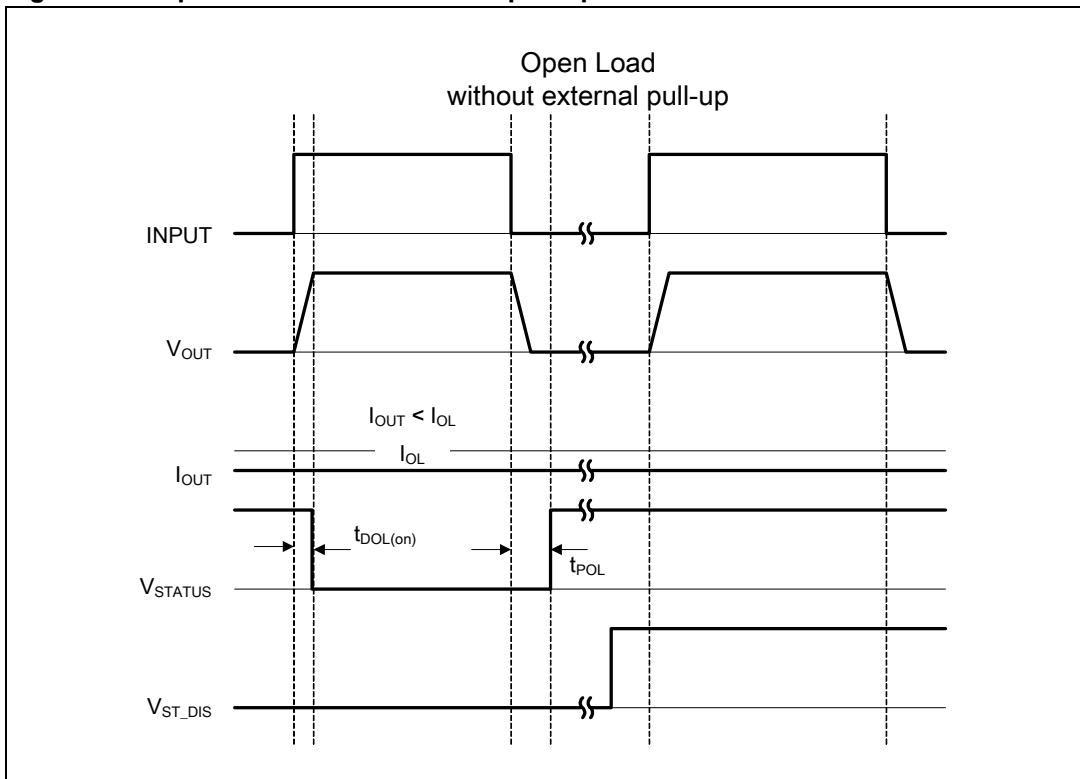


Figure 13. Short to V_{CC}

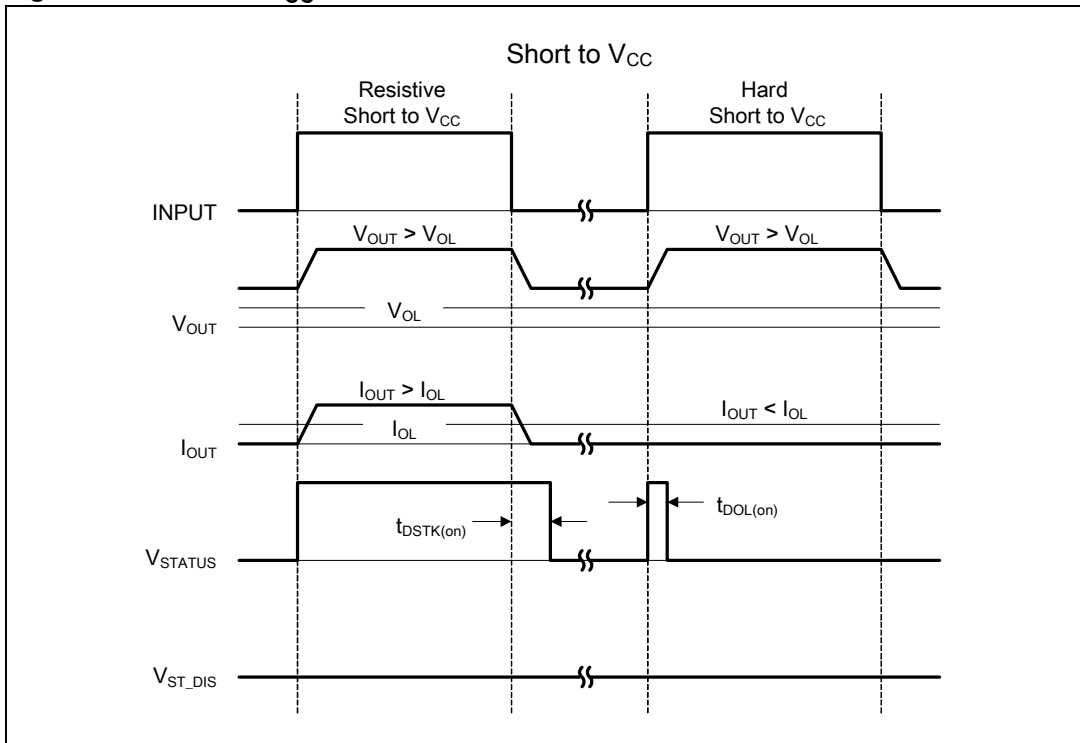
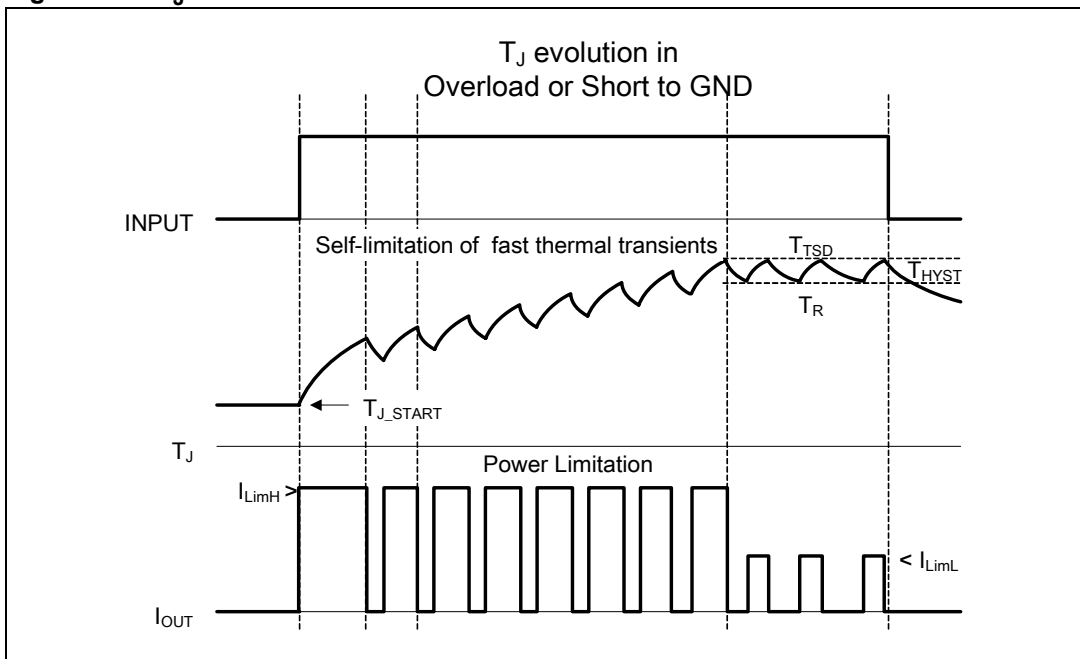


Figure 14. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 15. Off-state output current

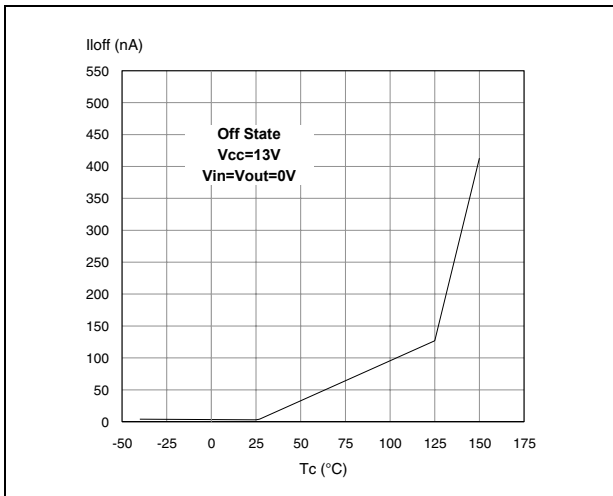


Figure 16. High level input current

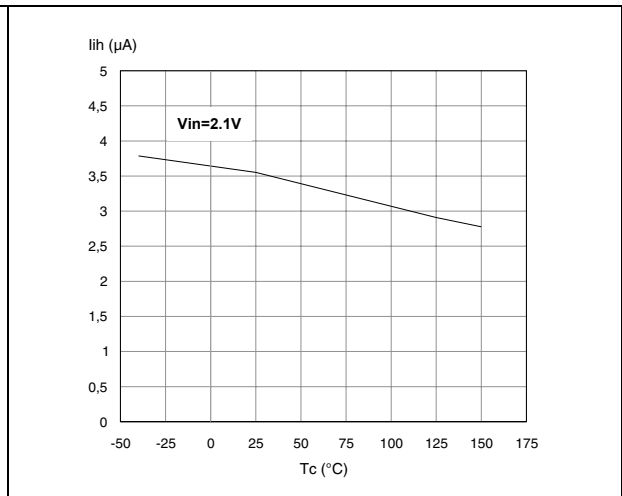


Figure 17. Input clamp voltage

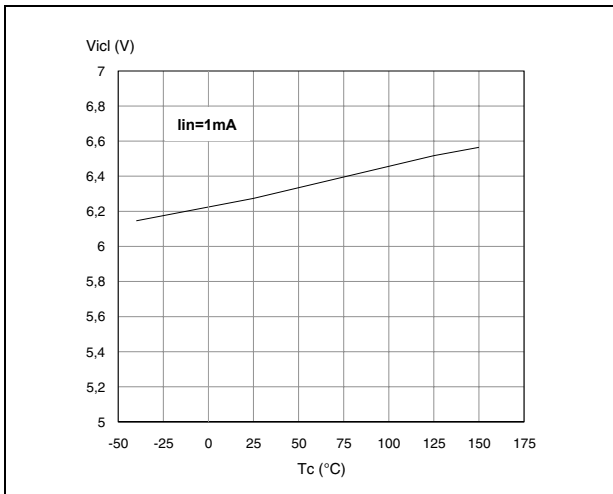


Figure 18. Input high level voltage

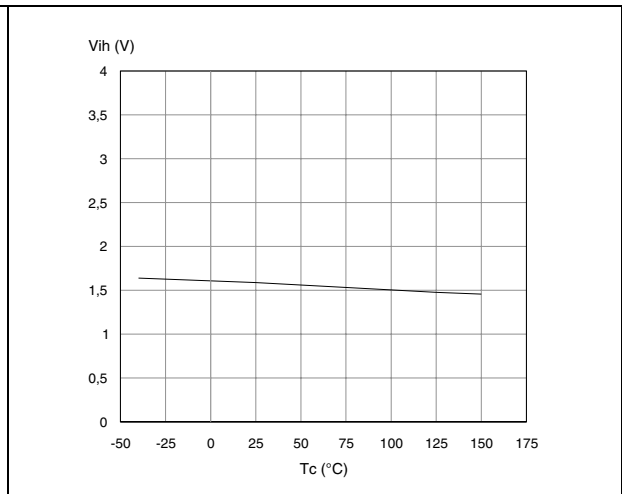


Figure 19. Input low level voltage

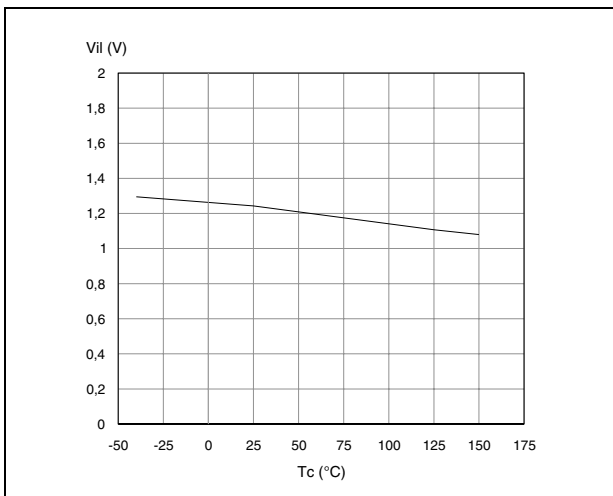


Figure 20. Low level STAT_DIS current

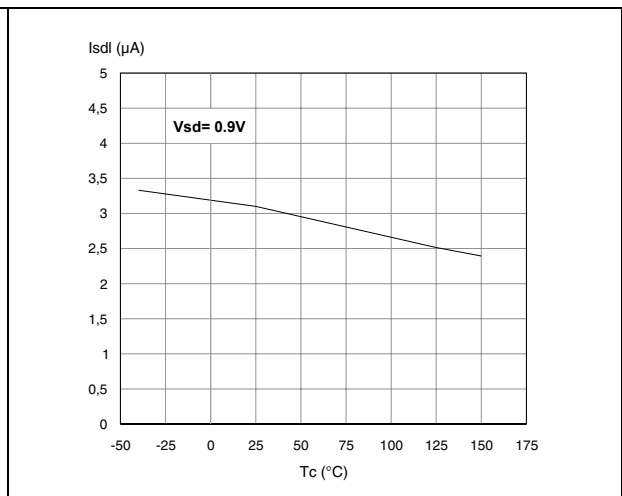


Figure 21. On-state resistance vs T_{case}

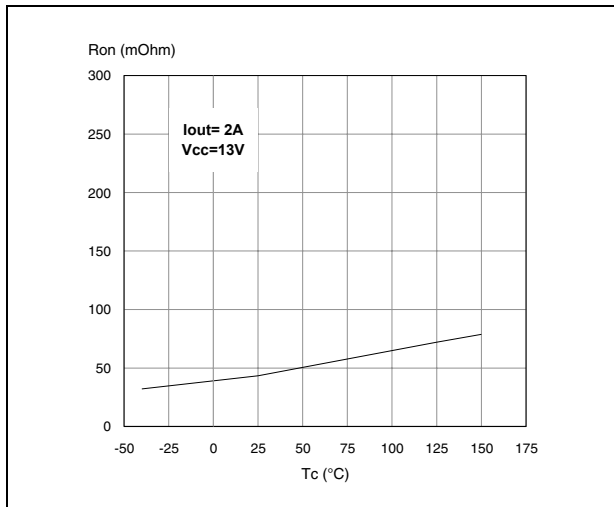


Figure 22. High level STAT_DIS current

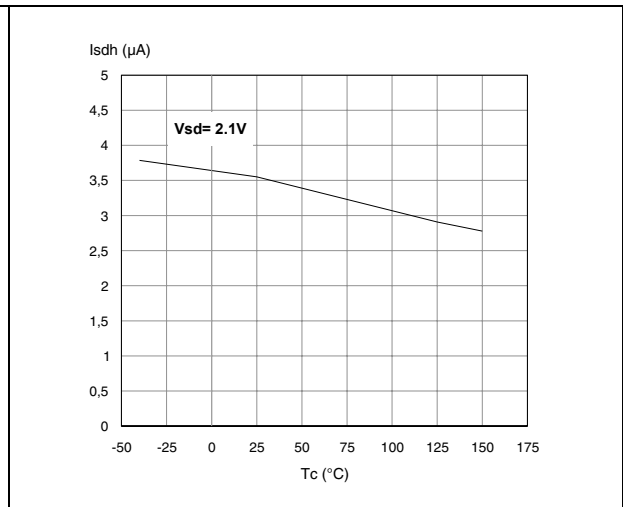


Figure 23. On-state resistance vs V_{CC}

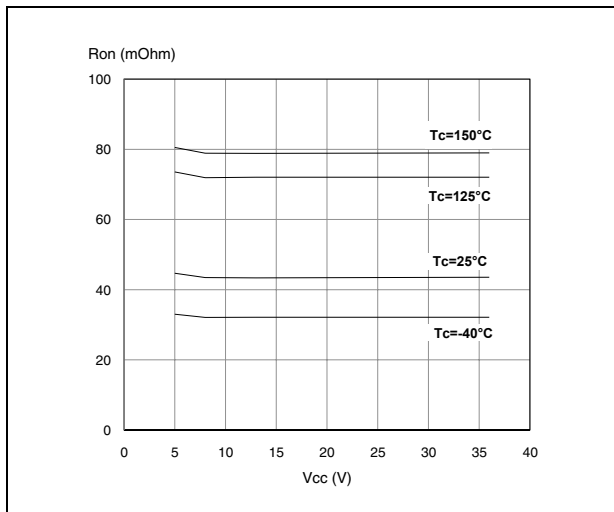


Figure 24. Low level input current

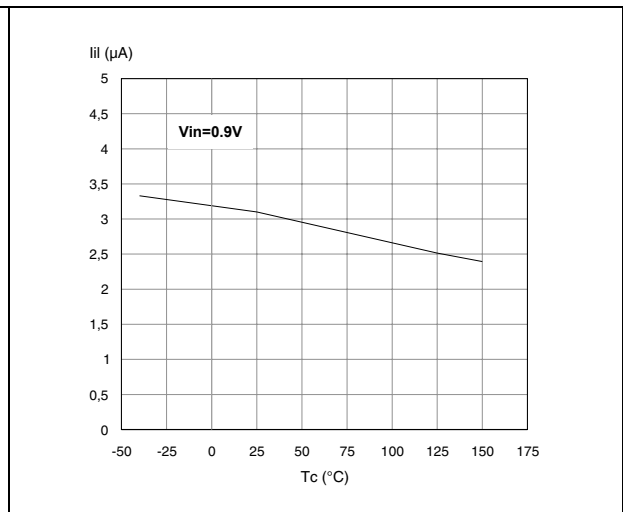


Figure 25. I_{LIM} vs T_{case}

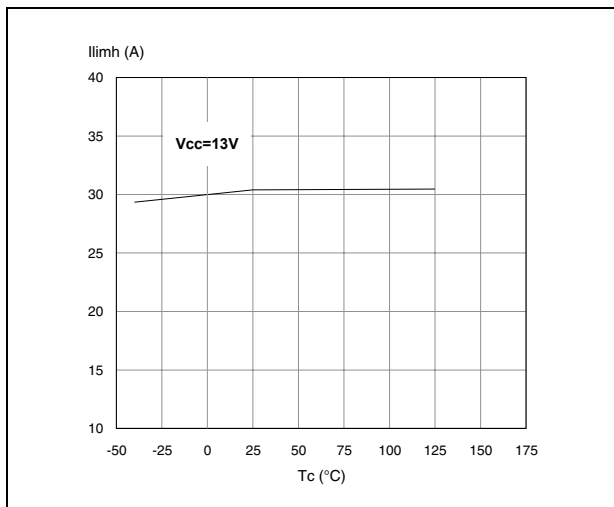


Figure 26. Turn-on voltage slope

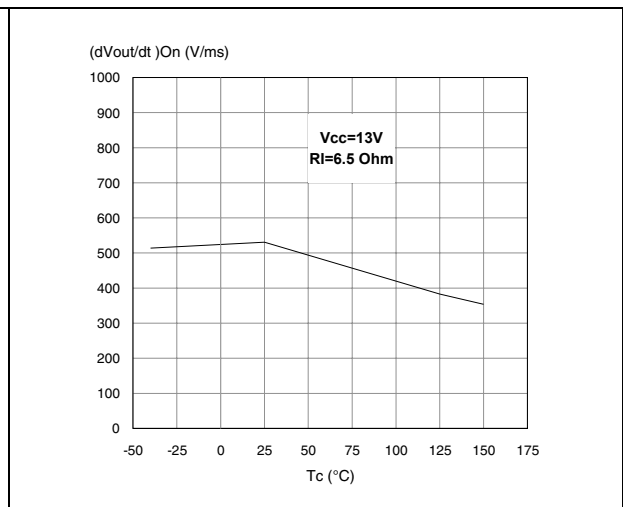


Figure 27. Undervoltage shutdown

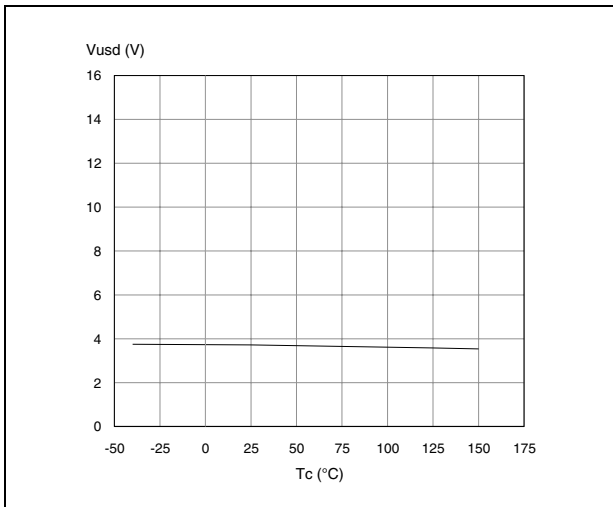


Figure 28. Turn-off voltage slope

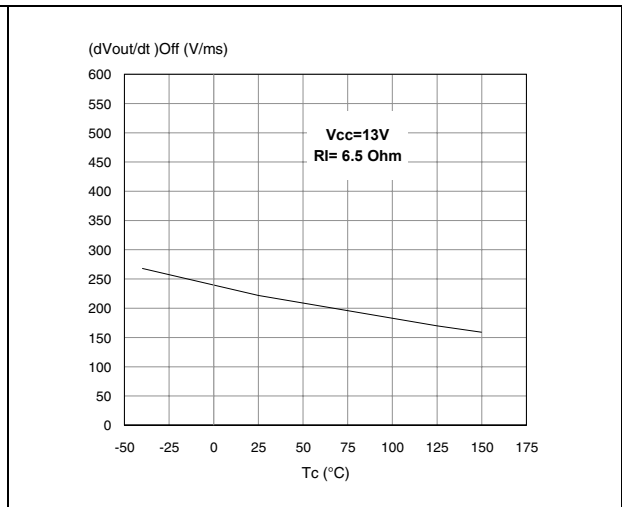


Figure 29. STAT_DIS clamp voltage

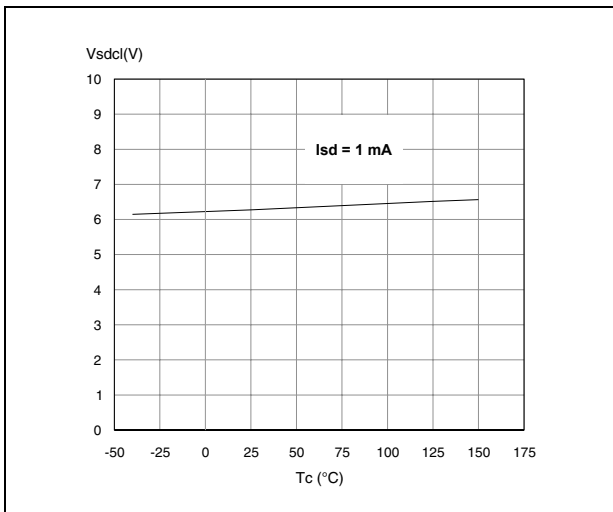


Figure 30. High level STAT_DIS voltage

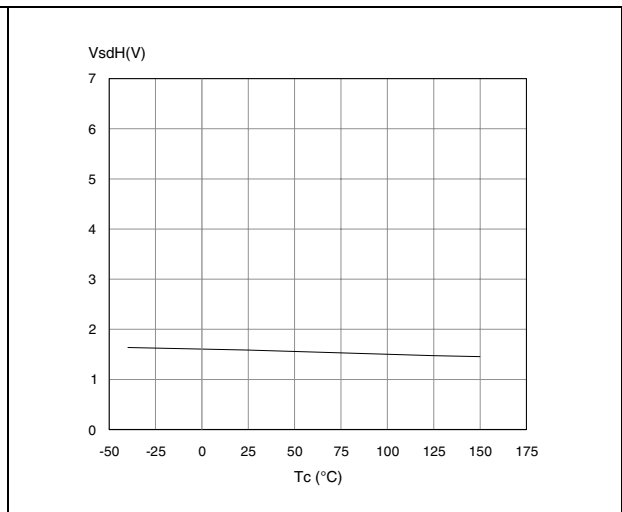
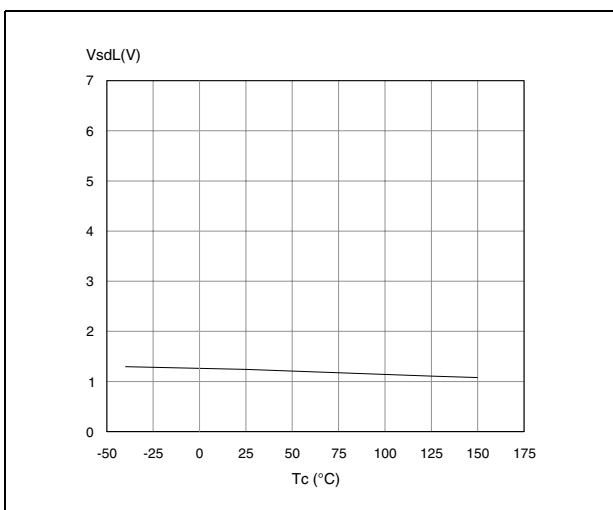
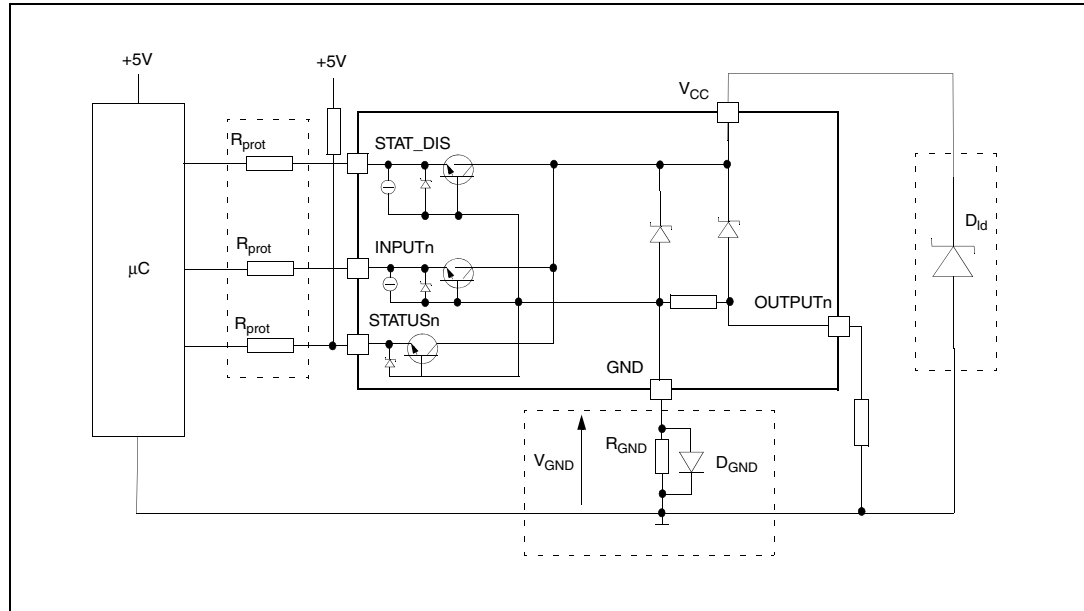


Figure 31. Low level STAT_DIS voltage



3 Application information

Figure 32. Application schematic⁽¹⁾



1. Channels 2, 3 and 4 have the same internal circuit as channel 1.

3.1 Gnd protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

$$1) R_{GND} \leq 600\text{mV} / (I_{S(on)max})$$

$$2) R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC} < 0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended R_{prot} value is $10k\Omega$.

3.4 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1) no false open-load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition

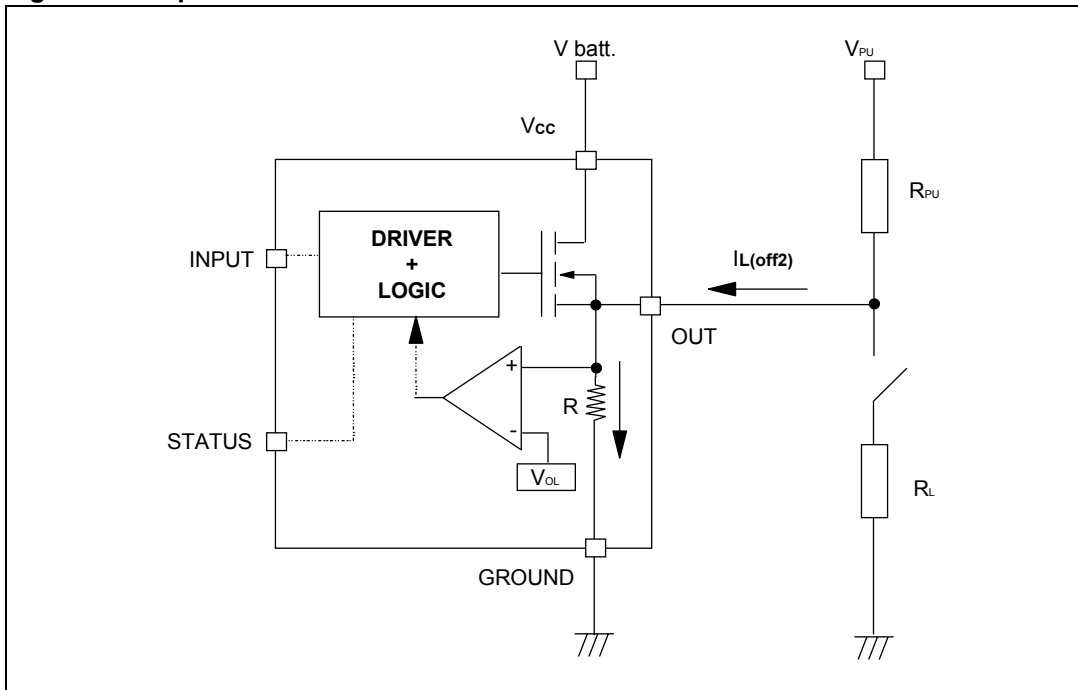
$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$$

2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

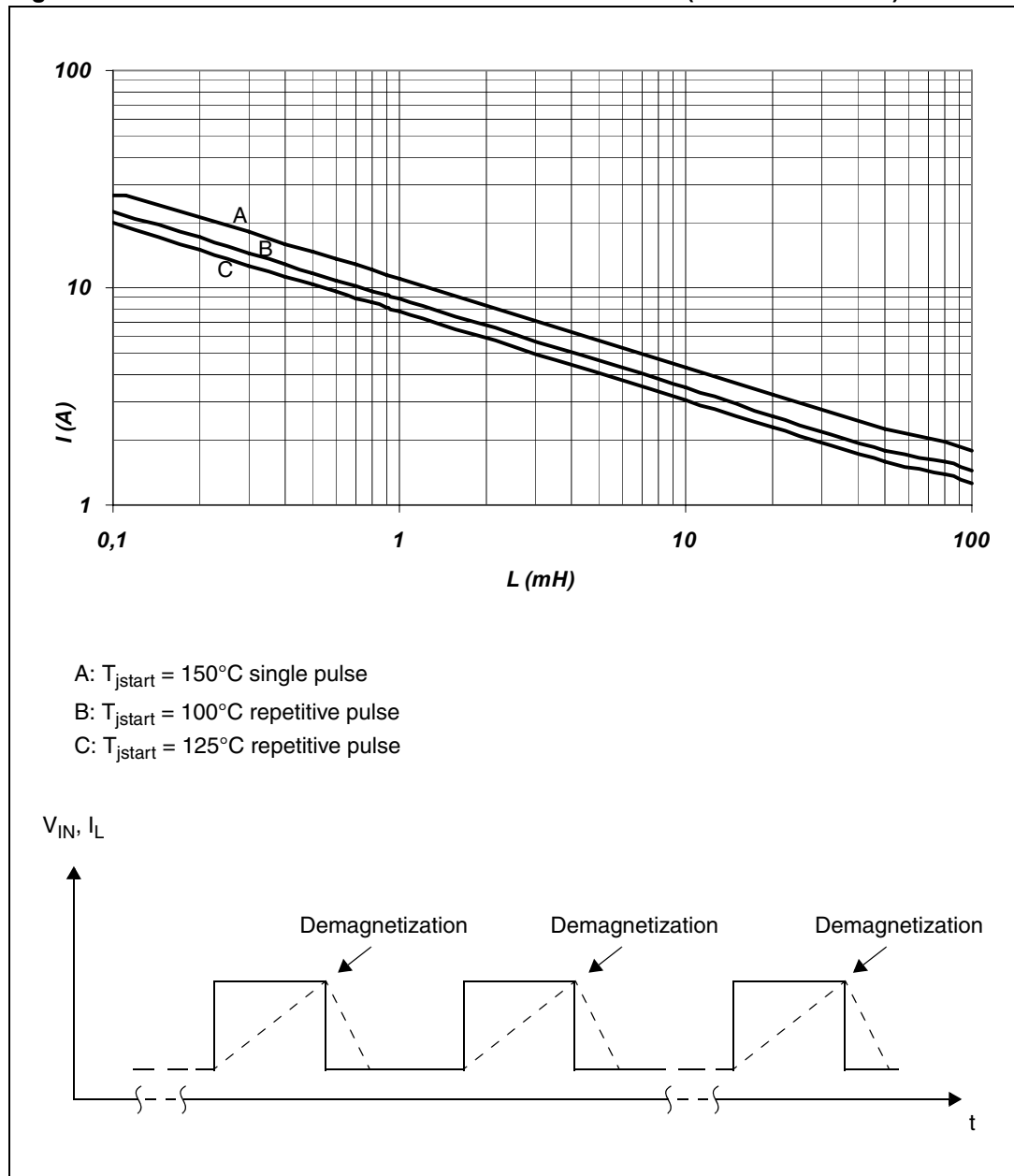
The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 33. Open-load detection in off-state



3.5 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 34. Maximum turn-off current versus inductance (for each channel)⁽¹⁾

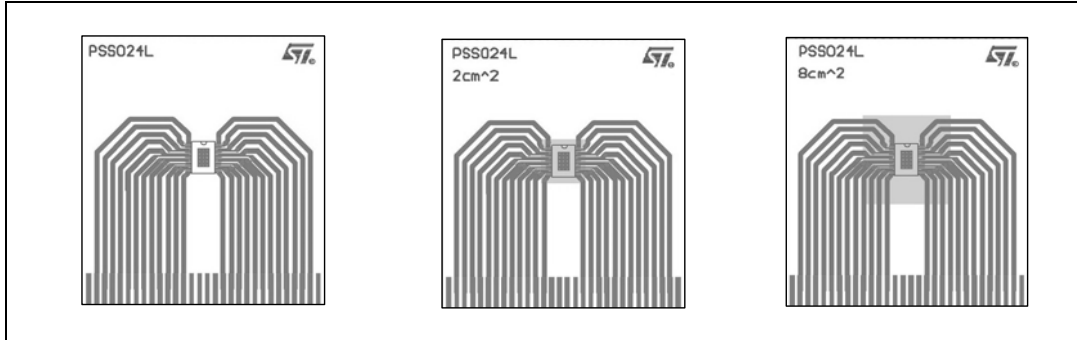


1. Values are generated with $R_L = 0\Omega$.
 In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μm (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

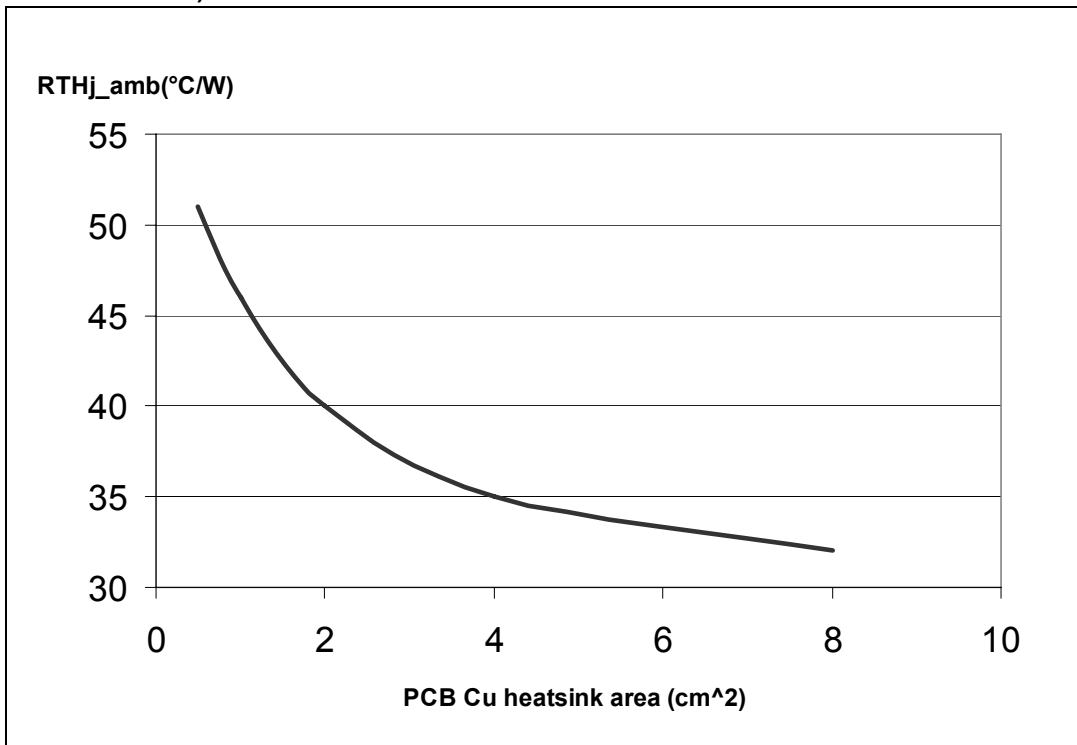


Figure 37. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

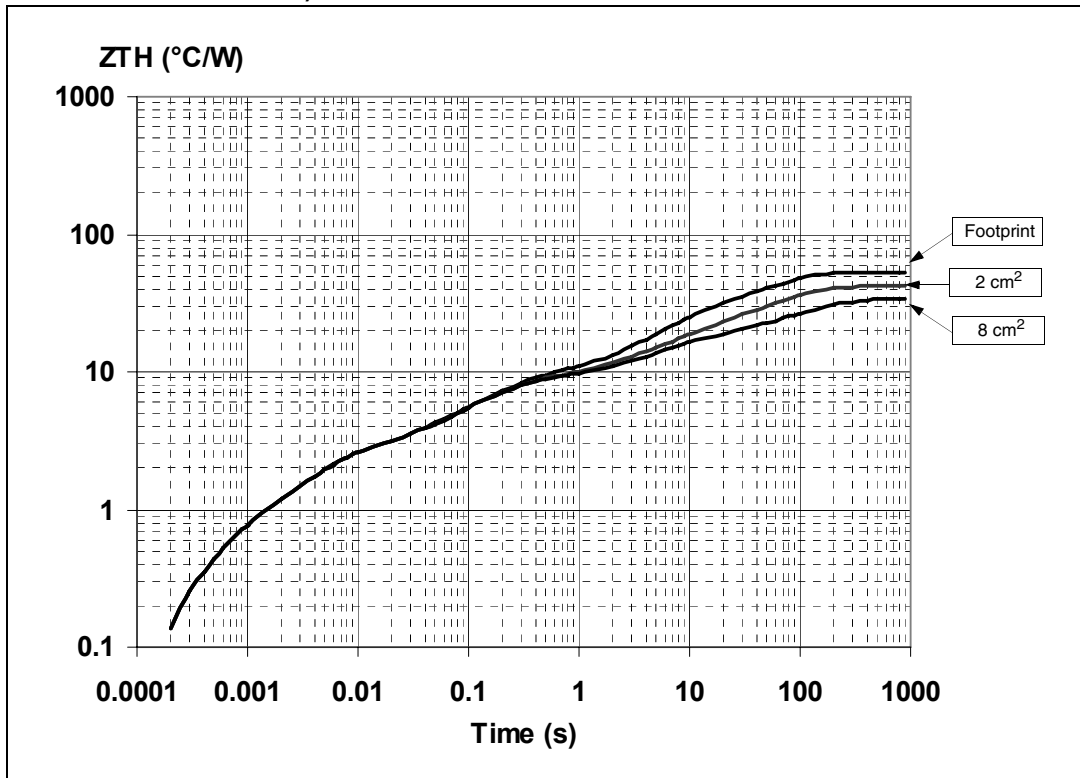
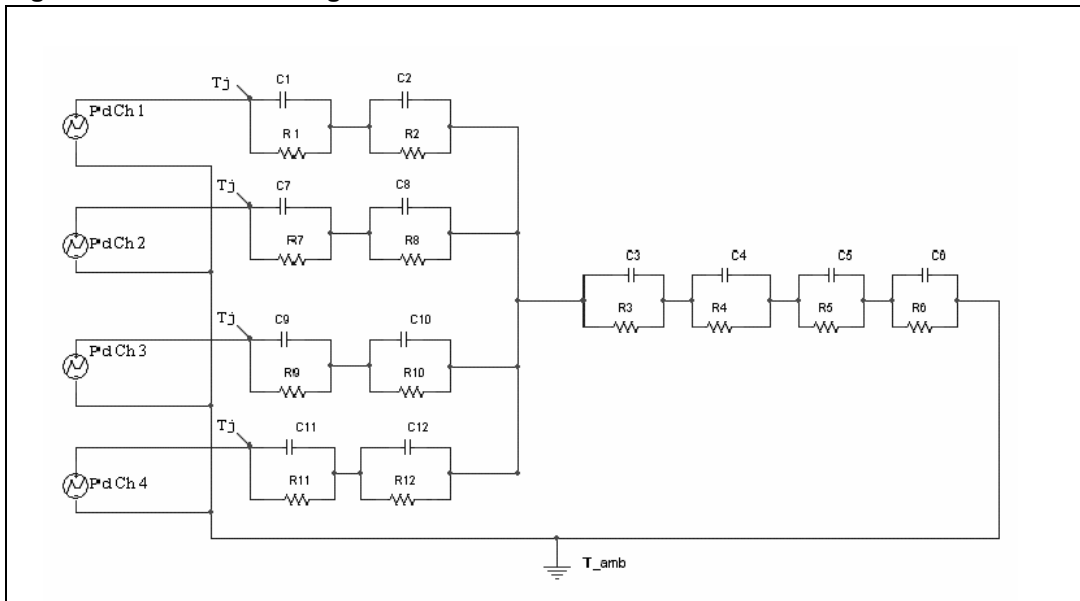


Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-24⁽¹⁾



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameter

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|----|----|
| R1 = R7 = R9 = R11 (°C/W) | 0.4 | | |
| R2 = R8 = R10 = R12 (°C/W) | 2 | | |
| R3 (°C/W) | 6 | | |
| R4 (°C/W) | 7.7 | | |
| R5 (°C/W) | 9 | 9 | 8 |
| R6 (°C/W) | 28 | 17 | 10 |
| C1 = C7 = C9 = C11 (W.s/°C) | 0.001 | | |
| C2 = C8 = C10 = C12 (W.s/°C) | 0.0022 | | |
| C3 (W.s/°C) | 0.025 | | |
| C4 (W.s/°C) | 0.75 | | |
| C5 (W.s/°C) | 1 | 4 | 9 |
| C6 (W.s/°C) | 2.2 | 5 | 17 |

5 Package information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 39. PowerSSO-24 package dimensions

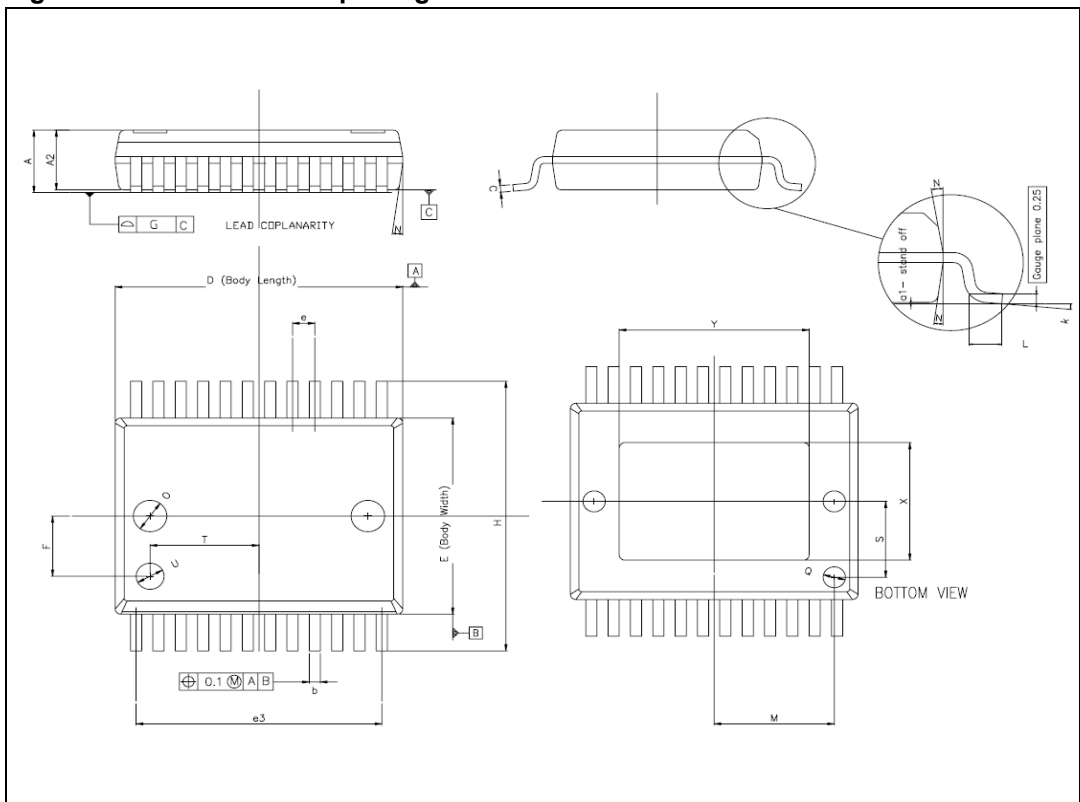


Table 16. PowerSSO-24™ mechanical data

| Symbol | Millimeters | | |
|--------|-------------|------|-------|
| | Min | Typ | Max |
| A | | | 2.45 |
| A2 | 2.15 | | 2.35 |
| a1 | 0 | | 0.1 |
| b | 0.33 | | 0.51 |
| c | 0.23 | | 0.32 |
| D | 10.10 | | 10.50 |
| E | 7.4 | | 7.6 |
| e | | 0.8 | |
| e3 | | 8.8 | |
| F | | 2.3 | |
| G | | | 0.1 |
| H | 10.1 | | 10.5 |
| h | | | 0.4 |
| k | 0° | | 8° |
| L | 0.55 | | 0.85 |
| O | | 1.2 | |
| Q | | 0.8 | |
| S | | 2.9 | |
| T | | 3.65 | |
| U | | 1.0 | |
| N | | | 10° |
| X | 4.1 | | 4.7 |
| Y | 6.5 | | 7.1 |

6 Packing information

6.1 PowerSSO-24 package packing information

Figure 40. PowerSSO-24 tube shipment (no suffix)

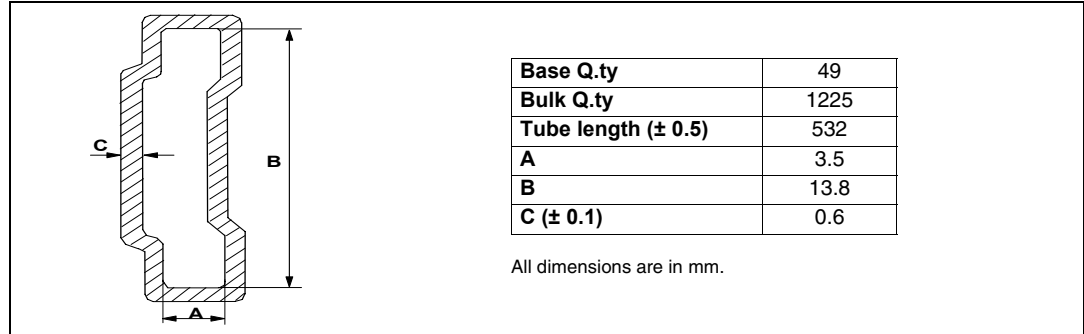
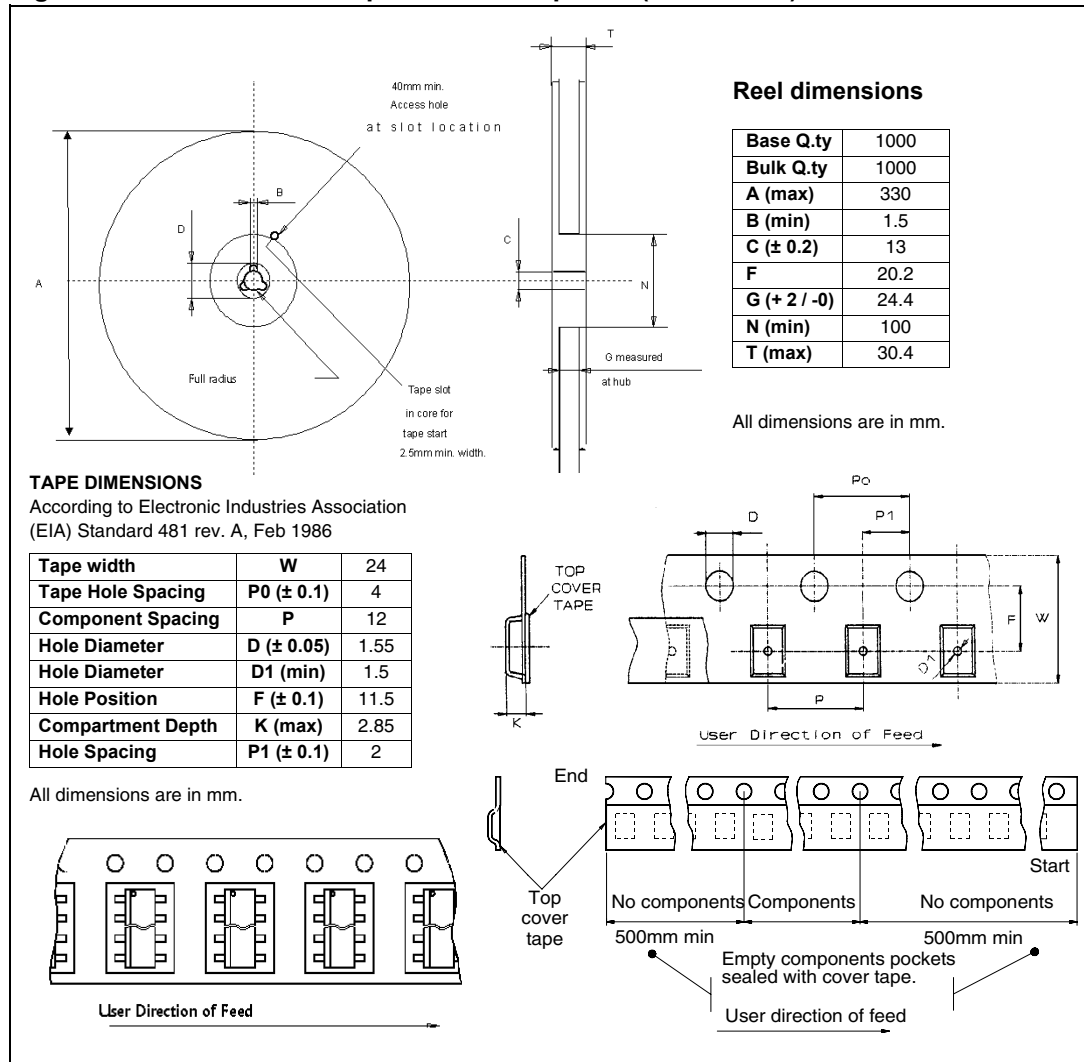


Figure 41. PowerSSO-24 tape and reel shipment (suffix "TR")



7 Order codes

Table 17. Device summary

| Package | Order codes | |
|-------------|-------------|---------------|
| | Tube | Tape and reel |
| PowerSSO-24 | VNQ5E050K-E | VNQ5E050KTR-E |

8 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| July-2006 | 1 | Initial release |
| May-2007 | 2 | Document rewritten, restructured and put in corporate technical literature template. Operative Vcc range changed from 36 V to 28 V. Tables 6, 12 updated. |
| 04-Feb-2008 | 3 | Document restructured. Changed <i>Description</i> on cover page. <i>Table 9: Open-load detection (8V<Vcc<18V)</i> : added td_vol parameter. Changed <i>Section 2.4: Waveforms</i> . Added <i>Section 2.5: Electrical characteristics curves</i> . |
| 22-Jun-2009 | 4 | <i>Table 16: PowerSSO-24 mechanical data</i> : – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows |
| 22-Jul-2009 | 5 | Updated <i>Figure 39: PowerSSO-24 package dimensions</i> . Updated <i>Table 16: PowerSSO-24 mechanical data</i> : – Deleted G1 row – Added O, Q, S, T and U rows |

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