SGLS004 – D2744, APRIL 1986

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

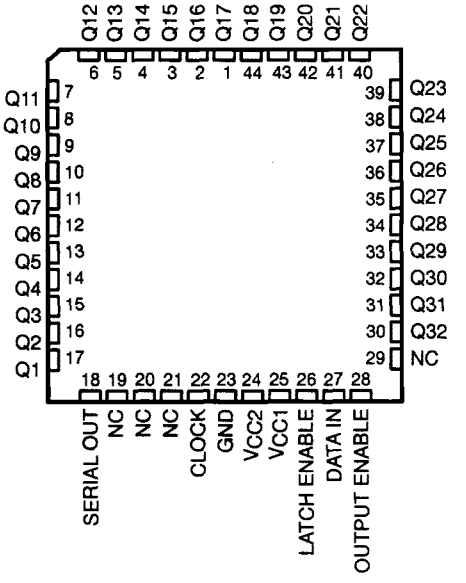
description

The SN55553 and SN55554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence is reversed from the SN55553 for ease in printed-circuit-board layout.

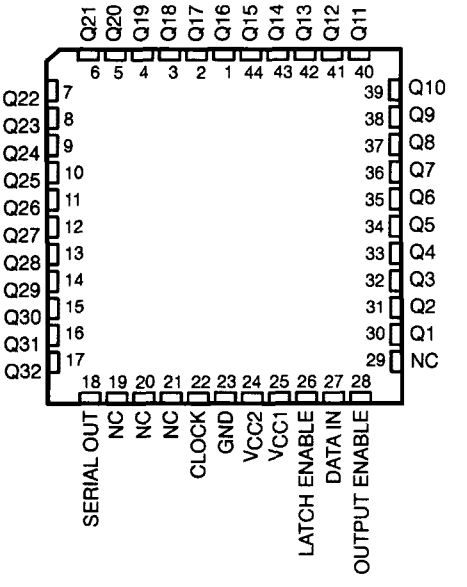
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55553 . . . FD PACKAGE
(TOP VIEW)



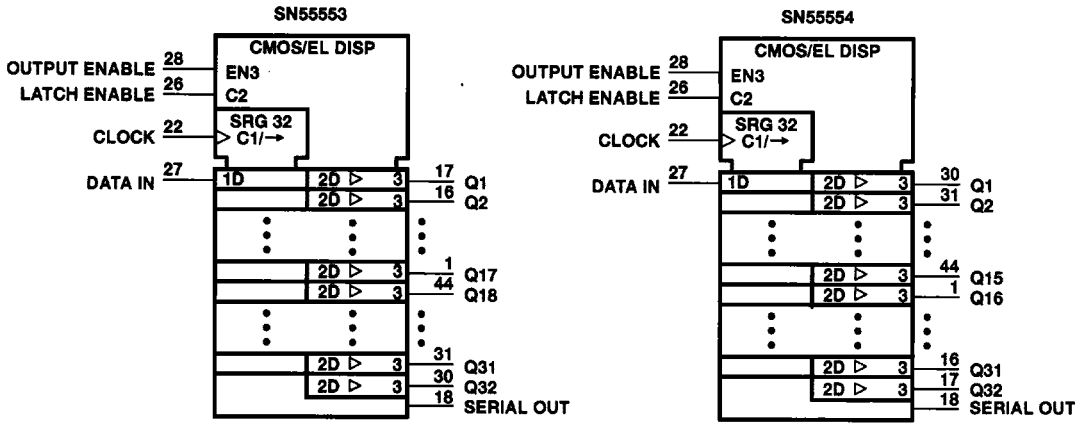
SN55554 . . . FD PACKAGE
(TOP VIEW)



NC – No internal connection

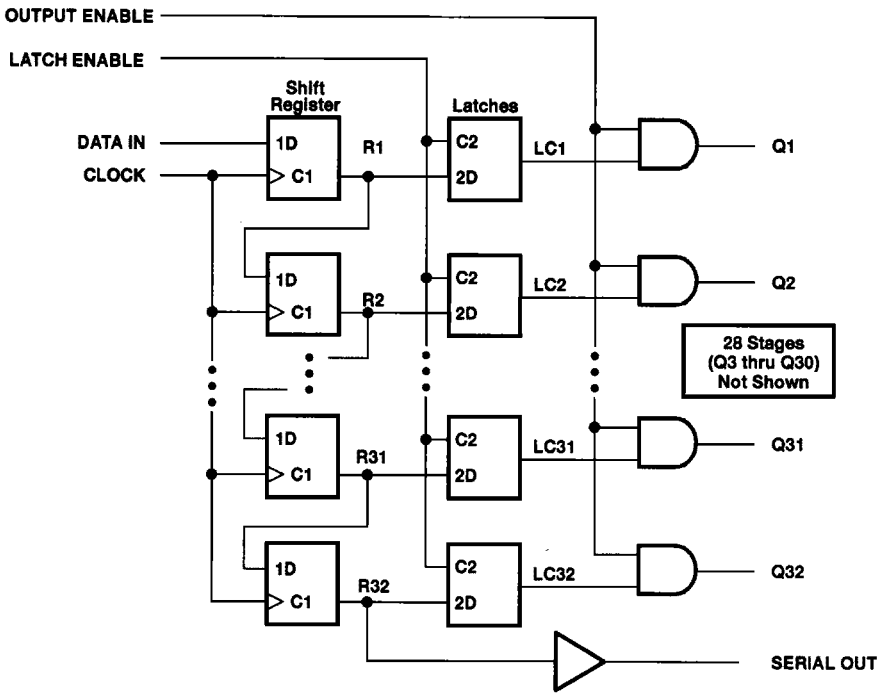
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

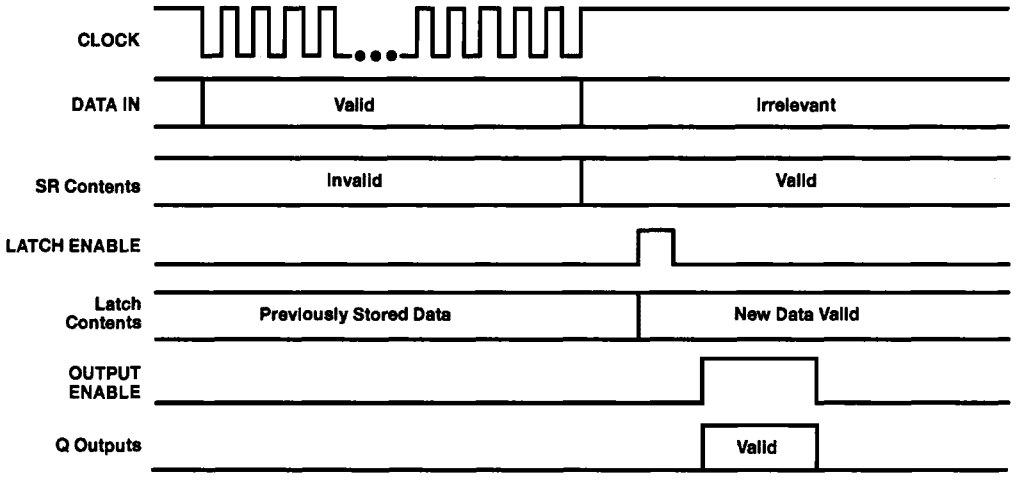
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q22
Load	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R32	Determined by
	No↑	X	X	No change		R32	OUTPUT ENABLE
Latch	X	L	X	As determined above	Stored data	R32	Determined by
	X	H	X		New data	R32	OUTPUT ENABLE
Output Enable	X	X	L	As determined above	Determined by LATCH ENABLE‡	R32	All L
	X	X	H			R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

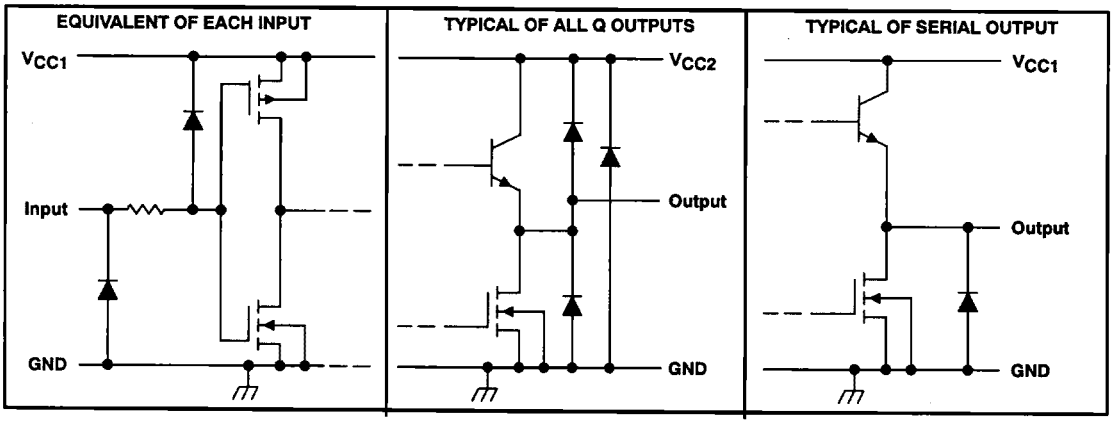
† R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 18 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1} + 0.3 V
Ground current ..... 700 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1825 mW
Minimum operating free-air temperature ..... −55°C
Operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	0		60	V
High-level input voltage, V_{IH}	0.75 V_{CC}		V_{CC} +0.3	V
Low-level input voltage, V_{IL}	−0.3		0.25V_{CC}	V
High-level output current, I_{OH}	−15			mA
Low-level output current, I_{OL}	15			mA
Output clamp current, I_{OK}			±20	mA
Clock frequency, f_{clock}, T_A = 25°C	0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$, T_A = 25°C	80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$, T_A = 25°C	80			ns
Setup time before CLOCK ↑, t_{su}, T_A = 25°C	20			ns
Hold time after CLOCK ↑, t_h, T_A = 25°C	110			ns
Operating free-air temperature, T_A	−55			°C
Operating case temperature, T_C			125	

electrical characteristics over recommended operating temperature range, V_{CC2} = 12 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	55		V
		SERIAL OUT	I_O = −100 µA	10		
V_{OL}	Low-level output voltage	Q outputs	I_O = 15 mA		10	V
		SERIAL OUT	I_O = 100 µA		1.5	
I_{IH}	High-level input current (see Note 3)		V_I = 12 V		5	µA
I_{IL}	Low-level input current (see Note 3)		V_I = 0		−5	µA
I_{CC1}	Supply current from V_{CC1}				7	mA
I_{CC2}	Supply current from V_{CC2}		Outputs high		20	mA
			Outputs low		2	

NOTE 3: I_{IH} and I_{IL} parameters are independent of V_{CC2} and need not be 60 V for this test.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{DLH}	Delay time, CLOCK↑ to SERIAL OUT↑	C_L = 45 pF to GND,	See Figures 1 and 2		200	ns
t_{DHL}	Delay time, CLOCK↑ to SERIAL OUT↓				200	ns
t_{DLH}	Delay time, LE to Q output↑	C_L = 45 pF to GND,	See Figures 1 and 3		1000	ns
t_{DHL}	Delay time, LE to Q output↓				500	µs

PARAMETER MEASUREMENT INFORMATION

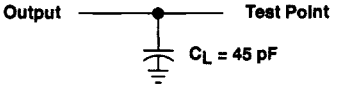


Figure 1. Load Circuit

PARAMETER MEASUREMENT INFORMATION

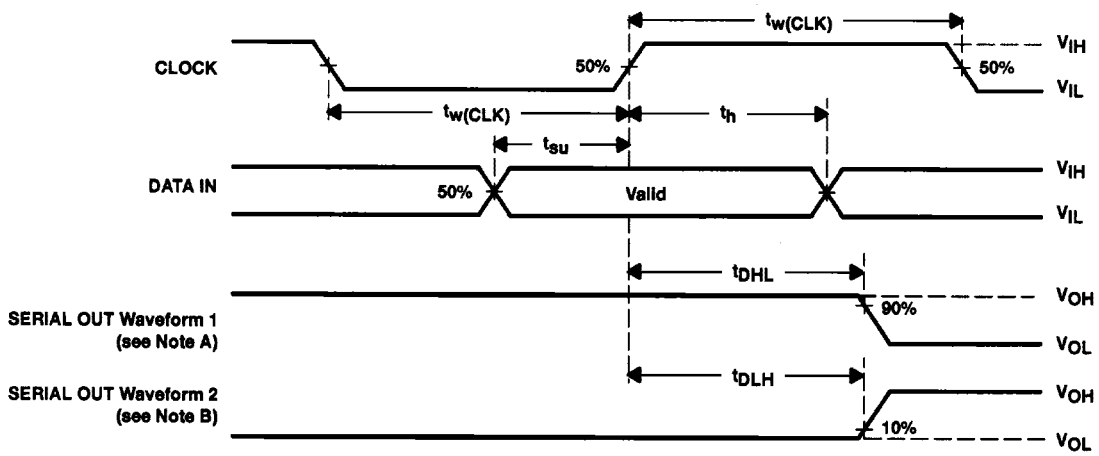


Figure 2. Voltage Waveforms for SERIAL OUT

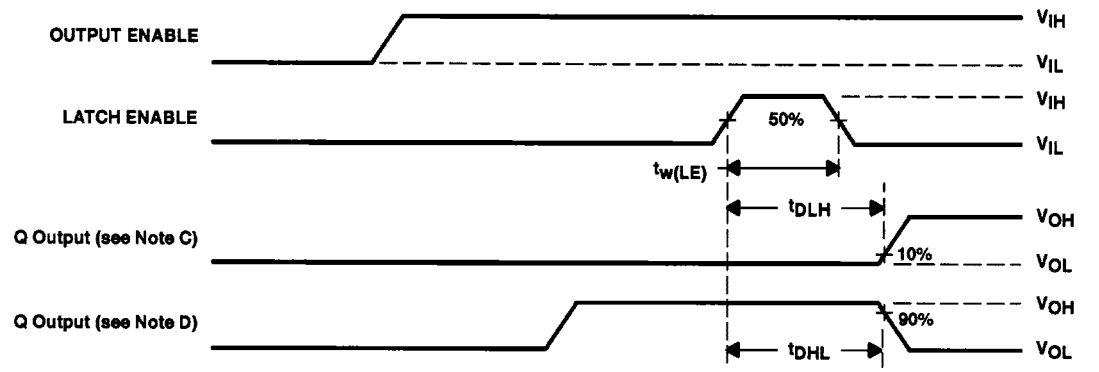


Figure 3. Voltage Waveforms for Q Outputs

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure t_{DLH}, initially a low is stored in the latch and a high is stored in the shift register.
D. To measure t_{DHL}, initially a high is stored in the latch and a low is stored in the shift register.