# SIEMENS

## Power Factor Controller (PFC)
**IC for High Power Factor and Active Harmonic Filtering**

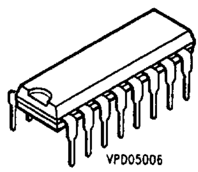
## TDA 4815; TDA 4818; TDA 4819

**Advance Information**

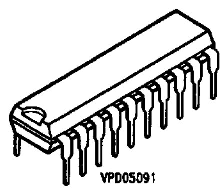
**Bipolar IC**

### Features

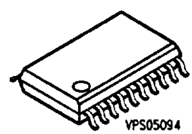
- Power factor approaching 1
- For wide-range power supplies
- Continuous mode with fixed frequency (TDA 4815, TDA 4819)
- Discontinuous mode with variable frequency (TDA 4818)
- 0.5 A driver for SIPMOS
- 300 kHz switching frequency
- Feed-forward control
- Complete protective functions



**P-DIP-16**



**P-DIP-20-1**



**P-DSO-20-1**

| Type | Ordering Code | Package |
|---|---|---|
| ▼ TDA 4815 | Q67000-A8323 | P-DIP-20-1 |
| ▼ TDA 4815 G | Q67000-A8324 | P-DSO-20-1 (SMD) |
| ▼ TDA 4818 | Q67000-A8325 | P-DIP-20-1 |
| ▼ TDA 4819 | Q67000-A8326 | P-DIP-16 |

▼ = New type

The TDA 4815, 4818, 4819 family of integrated circuits permits power-factor correction and voltage regulation over a wide range. These devices are designed for preregulators in switched-mode power supplies (SMPS). TDA 4815 and TDA 4819 produce sinusoidal line current generated by trapezoidal shaped current (continuous mode) through the primary inductor. This type of control is particularly suitable for preregulators with a fixed switching frequency and changing load conditions.

For constant loads and free-running frequency TDA 4818 provides control for triangular shaped current (discontinuous mode). All devices drive SIPMOS transistors directly and feature a multiplier, a pulse-width modulator, two control amplifiers, a reference voltage of 2.5 V plus overvoltage and overcurrent comparators. TDA 4815 additionally features feed-forward control to compensate for known interference such as input-voltage ripple.

TDA 4819 is an economy version of TDA 4815 in a P-DIP-16 package.

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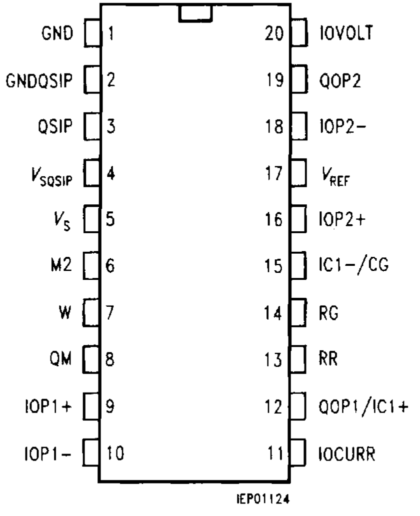
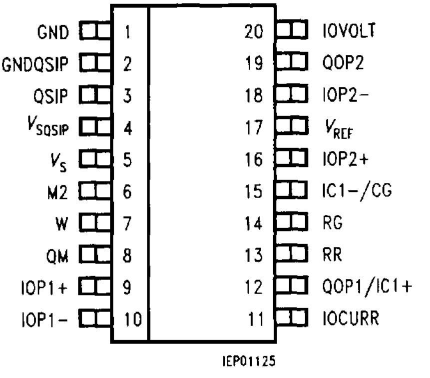
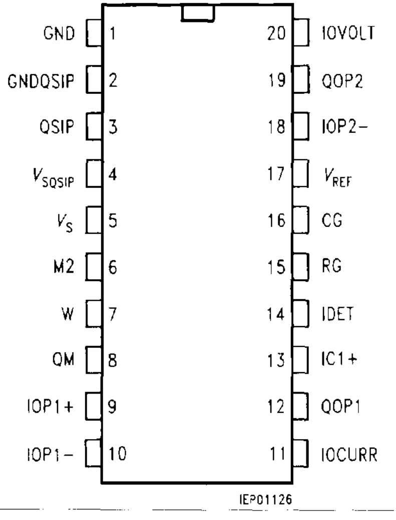
TDA 4815



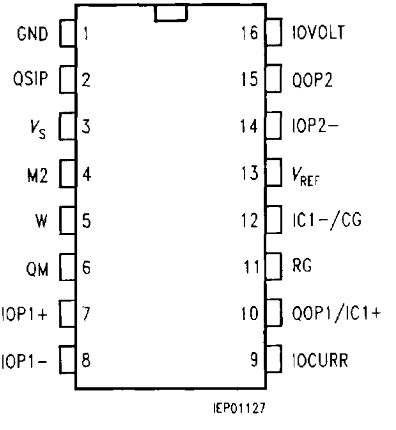

TDA 4815 G




TDA 4818



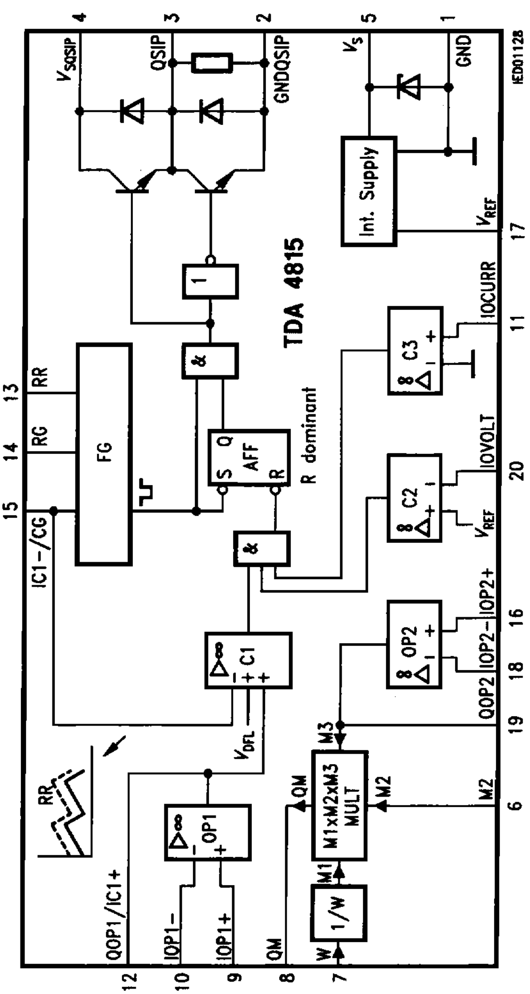

TDA 4819



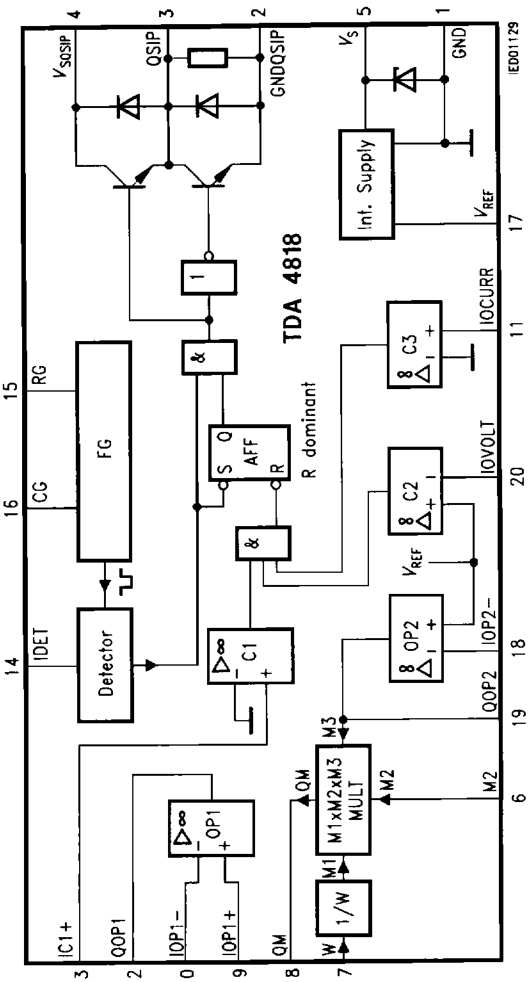

**Pin Configuration**
(top view)

## Pin Definitions and Functions

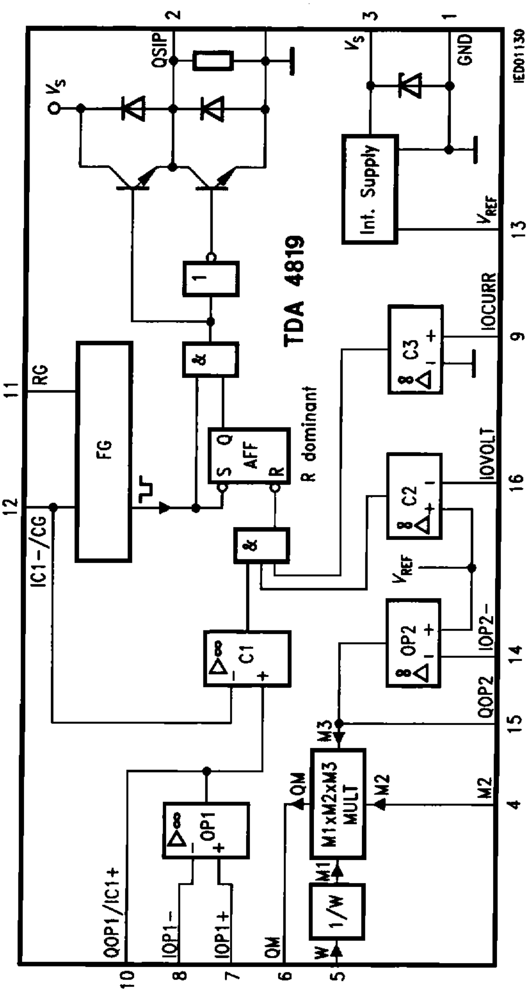
| Symbol | Function |
|---|---|
| GND | Ground |
| GNDQSIP | Ground, SIPMOS driver |
| QSIP | SIPMOS driver output |
| $V_{SQSIP}$ | Supply voltage, SIPMOS driver |
| $V_S$ | Supply voltage |
| M2 | Multiplier input |
| W | Wide voltage range input |
| QM | Multiplier output |
| IOP + | Non-inverting input op-amp1 |
| IOP – | Inverting input op-amp 1 |
| IOCURR | Overcurrent sense input |
| QOP1 | Output op-amp 1 |
| IC1 + | Non-inverting input current comparator 1 |
| RR | Ramp generator resistor |
| RG | Frequency generator resistor |
| IC1 – | Inverting input current comparator 1 |
| CG | Frequency generator capacitor |
| $V_{REF}$ | Reference voltage |
| IOP2 + | Non-inverting input op-amp 2 |
| IOP2 – | Inverting input op-amp 2 |
| QOP2 | Output op-amp 2 |
| IOVOLT | Overvoltage sense input |
| IDET | Detector input |




**Block Diagram (TDA 4815)**




**Block Diagram (TDA 4818)**




**Block Diagram (TDA 4819)**

## Functional Description

### Voltage Supply

The IC does not switch from standby to full current consumption until the turn-ON threshold on $V_S$ is exceeded. Turn-OFF is controlled by hysteresis. The integrated Z-diode limits the voltage on $V_S$ when impressed current is fed.

### Operational Amplifier

Operational amplifier 1 (OP1) is a control amplifier and compares the current on the current-sensing resistor to the setpoint on the output of the multiplier. The duty factor that is momentarily necessary is then set via comparator C1 and the ramp generator.

Operational amplifier 2 (OP2) is also configured as a control amplifier. This compares the divided output voltage to the adjusted reference voltage $V_{REF}$, which is stable with temperature. The output voltage of OP2 produced in this way is multiplied in the triple multiplier by a sine-magnitude voltage. On the output of the multiplier a sine-magnitude current then appears that is variable in amplitude.

### Multiplier and 1/W

The multiplier (MULT) processes two, relatively slowly altering voltages (M1, M3) and a sine-magnitude voltage (M2). With the voltage on input M1 preregulation for wide-range AC voltage is produced via 1/W on the input of the SMPS. This takes the load from OP2. The output voltage of the SMPS is regulated to a constant value, independent of the load, with the voltage on input M3.

At its output the multiplier produces an impressed sine-magnitude current. The pulse width of the output signal on QSIP has to be altered so that the potential on the output of the multiplier is always kept on OV. This is managed by OP1, C1 and the ramp generator.

### Frequency Generator

The frequency generator (FG) produces a constant frequency for operation with trapezoidal current. The time of the falling edge on FG determines the minimum time for which output QSIP is reliably turned off.

The frequency generator produces on the capacitor CG also the ramp voltage for the pulse width modulation (PWM).

Using the TDA 4818 (with triangular current) the circuit has to be started and possibly restarted at regular intervals. This can be done externally by a lamp generator for instance. But a convenient solution is to use the internal frequency generator to retrigger it.

### Feed Forward Control (TDA 4815)

The TDA 4815 has the additional advantage of a feed forward control, i. e. via the input RR (pin 13) the PWM-ramp will be controlled dependent on the line input voltage. The current fed into pin 13 causes (via an internal current mirror) a parallel shift of the PWM-ramp voltage with the transfer ratio $V_{Shift} / I_{RR}$ and without changing the slope. This function controls the duty cycle to increase the dynamic of the current regulator.

The benefit is a better shape of the drawn line current especially at low operation frequencies.

The parallel shift of the PWM-ramp voltage has to be dimensioned this way: If the peak value of the input voltage reaches the output voltage, then $V_{Shift}$ has to correspond to the amplitude of the ramp voltage (typ. 1.5 V).

**Detector (TDA 4818)**



For operation with triangular current IDET is connected to the current-sensing choke. When input IDET is high, the SIPMOS driver is turned off. At the same time the flipflop (AFF) can be set. When IDET is low and there is no more current flowing in the choke, output QSIP is enabled. After the setpoint current has been reached in the choke, comparator C1 turns the output off again by resetting AFF. In this way the choke is always currentless when the SIPMOS transistor turns on and no gaps appear in the choke current.

**Comparators C2 and C3**

Comparator C2 turns off output QSIP when the output voltage of the SMPS is overvoltage. Comparator C3 turns off output QSIP when the SIPMOS transistor has source overcurrent. This guards the SMPS against overload during the turn-on operation or if there are abrupt changes in load.

**Output QSIP**

The output driver is designed as a push-pull stage. There is a resistor of 10 kΩ across QSIP and GND. This keeps the SIPMOS transistor turned off during standby mode.

Output QSIP is also connected via diodes to the supply $V_S$ and to GND.

When the supply of the SMPS is turned on, the diode to $V_S$ conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smoothing capacitor on $V_S$. The voltage on $V_S$ should not then exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode to GND clamps negative voltages on QSIP to – 0.7 V. Capacitive currents produced by voltage breakdown on the drain of the SIPMOS transistor can then flow away unhindered.

**Absolute Maximum Ratings**
$T_A$ = – 40 to 85 ˚C

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply voltage | $V_S$ | – 0.3 | $V_Z$ | V | $V_Z$ = Z-voltage |
| Supply voltage for SIPMOS driver | $V_{SQSIP}$ | – 0.3 | 17 | V | (**see Characteristics**) |
| Inputs IC1, IC2, IC3, W, IOP, M2, M3 | $V_n$ | – 0.3 | 17 | V | |
| IDET | $V_{IDET}$ | 1 | 4 | V | |
| | $I_{IDET}$ | – 5 | 5 | mA | $V_{IDET}$ > 4 V or < 1 V |
| Reference voltage | $V_{REF}$ | – 0.3 | 6 | V | |
| Outputs QOP | $V_{QOP}$ | – 0.3 | 6 | V | |
| QM | $V_{QM}$ | – 2 | 6 | V | |
| Z-current $V_S$-GND | $I_Z$ | 0 | 70 | mA | Observe $P_{max}$ |
| Driver output QSIP | $V_{QSIP}$ | – 0.3 | $V_{VSQSIP}$ | V | |
| QSIP clamping diodes | $I_{QSIP}$ | – 150 | 50 | mA | $V_{QSIP}$ > $V_{VSQSIP}$ or $V_{QSIP}$ < – 0.3 V |
| Inputs CG, RG, RR | $V_{CG, RG}$ | – 0.3 | 6 | V | |
| | $I_{RR}$ | 0 | 1 | mA | |
| Junction temperature | $T_j$ | | 150 | ˚C | |
| Storage temperature | $T_{stg}$ | – 65 | 125 | ˚C | |
| Thermal resistance system-air | | | | | |
| TDA 4819 | $R_{th SA}$ | | 70 | K/W | P-DIP-16 |
| TDA 4815, 4818 | $R_{th SA}$ | | 60 | K/W | P-DIP-20 |
| TDA 4815 G | $R_{th SA}$ | | 95 | K/W | P-DSO-20-1 |

**Operating Range**

| Parameter | Symbol | min. | max. | Unit | Remarks |
|---|---|---|---|---|---|
| Supply voltage | $V_S$ | $V_{SON}$ | $V_Z$ | V | 1) |
| Supply voltage QSIP | $V_{SQSIP}$ | | 17 | V | |
| Z-current | $I_Z$ | 0 | 50 | mA | Observe $P_{max}$ |
| Driver current | $I_{QSIP}$ | – 500 | 500 | mA | Observe $P_{max}$ |
| Switching frequency | $f_{FG}$ | 50 | 300000 | Hz | |
| Ambient temperature | $T_A$ | – 40 | 85 | ˚C | |
| QSIP clamping diodes | $I_{QSIP}$ | – 100 | 30 | mA | Observe $P_{max}$ |
| GNDQSIP | $V_{GNDQSIP}$ | – 0.3 | 0.5 | V | TDA 4815/4818 |

1) $V_{SON}$ means $V_{SH}$ has been exceeded but the supply voltage is still above $V_{SL}$. The device has switched from standby to active. For $V_{SH}$ and $V_{SL}$ values, **see Characteristics**. If 0 V < $V_S$ < $V_{SON}$, the device is on standby and output QSIP is low.

## Characteristics

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Current Consumption** | | | | | | |
| Without load on driver (QSIP) and $V_{REF}$: | | | | | | |
| QSIP low | $I_S$ | | | 0.7 | mA | $0\ V < V_S < V_{S\,ON}$ |
| | | | | 10 | mA | $V_{S\,ON}$ 1) $< V_S < V_Z$ |
| Load on QSIP with SIPMOS gate; | | | | | | |
| dynamic operation | $I_S$ | | 20 | | mA | $V_S = 12\ V$ |
| | | | | | | $f_{FG/DET} = 100\ kHz$; |
| | | | | | | load QSIP = 3 nF |
| **Hysteresis on $V_S$** | | | | | | |
| Turn-ON threshold for $V_S$ rising | $V_{SH}$ | | 10.5 | | V | |
| Turn-OFF threshold for $V_S$ falling | $V_{SL}$ | | 8.5 | | V | |
| **Comparators (C1, C2, C3)** | | | | | | |
| Input offset voltage C2, C3 | $V_{IO}$ 2) | – 10 | | 10 | mV | |
| Input offset voltage C1 | $V_{IO}$ 2) | | 50 | | mV | |
| (TDA 4815, 4819) | $V_{IO}$ 2) | | | | | |
| Input offset voltage C1 | $-I_I$ | | 100 | 2 | mV | |
| (TDA 4818) | | | | | | |
| Input current | | | | | µA | |
| Common-mode range | | | | | | |
| C1, C2, C3 | $V_{CM}$ | – 0.3 | | $V_{DFL}$ | V | See frequency generator |
| **Operational Amplifiers (OP1, OP2)** | | | | | | |
| Open-loop voltage again | $G_{VOL}$ | 60 | 80 | | dB | |
| Input offset voltage OP1 | $V_{IO}$ | 0 | | 12 | mV | $I_Q = 100\ \mu A$ |
| OP2 | $V_{IO}$ | – 6 | | 6 | mV | $I_Q = 100\ \mu A$ |
| Input current | $-I_I$ | | | 2 | µA | |
| Common-mode range | $V_{CM}$ | – 0.3 | | 4 | V | |
| Output current | $I_Q$ | – 2 | | 1 | mA | $1.5\ V < V_Q < 4.5\ V$ |
| Output voltage | $V_{QOP}$ | 0.8 | | 4 | V | |
| Gain-bandwith product | $f_T$ | | 2 | | MHz | |
| Transition phase | $p_T$ | | 90 | | deg | |

1) $V_{Son}$ means $V_{SH}$ has been exceeded but voltage is still > $V_{SL}$. The device has switched from standby to active.

2) $V_{IO} = V_+ - V_-$

## Characteristics (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Reference Voltage ($V_{REF}$)** | | | | | | |
| Voltage | $V_{REF}$ | 0 | 2.5 | | V | $0 < I_{REF} < 1$ mA |
| Load current | $-I_L$ | | | 3 | mA | |
| Voltage change | $\Delta V_{REF}$ | | 5 | | mV | $10 \text{ V} < V_S < V_Z$ |
| Voltage change | $\Delta V_{REF}$ | | 10 | | mV | $0 \text{ mA} < I_{REF} < 1$ mA |
| Temperature response | $\Delta V_{REF}/\Delta T$ | – 0.3 | | 0.3 | mV/K | |
| Accuracy | | – 1 | | 1 | % | $V_S = 12$ V; $I_{REF} = 1$ mA; $T_A = 25$ °C |
| **Output Driver (QSIP)** | | | | | | |
| H-output voltage | $V_{QSIPH}$ | 6 | | | V | $I_{QSIP} = -10$ mA |
| L-output voltage | $V_{QSIPL}$ | | | 1 | V | $I_{QSIP} = 10$ mA |
| Output current [1) ] | | | | | | |
| rising edge | $-I_{QSIP}$ | | 400 | | mA | $C_L = 3$ nF |
| falling edge | $I_{QSIP}$ | | 500 | | mA | $C_L = 3$ nF |
| **Z-Diode ($V_S$-GND)** | | | | | | |
| Z-voltage (observe $P_{max}$) | $V_Z$ | 15 | | 17 | V | $I_Z = 50$ mA |

1) Maximum current during rising or falling edge.

**Characteristics** (cont'd)

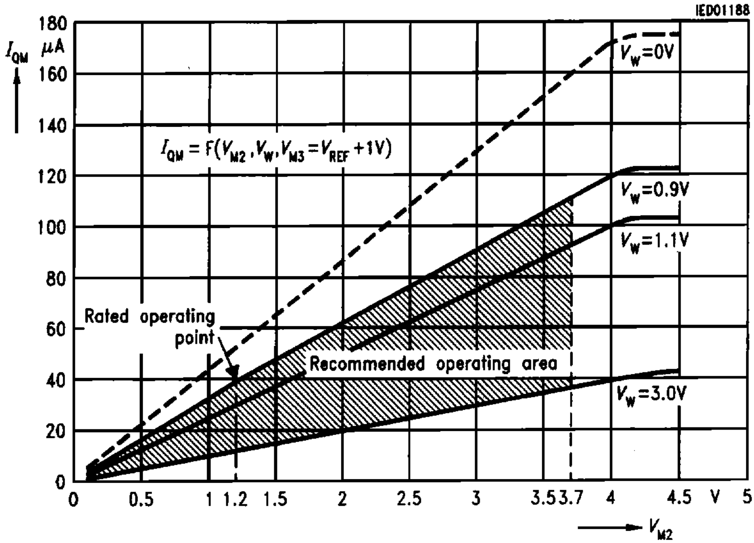
| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Multiplier (MULT) and 1/W** | | | | | | |
| Quadrant for input voltages | | | I | | qu | |
| Input voltage W | $V_W$ | 0.9 | | 3 | V | |
| Reference level for W | $V_{REF\ W}$ | | 0 | | V | |
| Input voltage M2 | $V_{M2}$ | 0 | | 3.7 | V | |
| Reference level for M2 | $V_{REF\ M2}$ | | 0 | | V | |
| Input voltage M3 | $V_{M3}$ | $V_{REF}$ | | $V_{QOP(max)}$ | V | |
| Reference level for M3 | $V_{REF\ M3}$ | | $V_{REF}$ | | V | |
| Input current W, M2, M3 | $-I_I$ | 0 | | 2 | µA | |
| Coefficient of output current | $k$ | | 30 | | µA/V | |
| Temperature response of coefficient | $\Delta k/\Delta(k_0 K)$ | | ± 0.1 | | %/K | |
| Multiplier output current at rated operating point (ROP) | $I_{QM(ROP)}$ | | 40 | | µA | Rated operating point: $V_{M2}$ = 1.2 V $V_W$ = 0.9 V $V_{M3} - V_{REF}$ = 1 V |

Calculation of output current: $I_{QM} = k \times \frac{V_M \times (V_{M3} - V_{REF})}{V_W}$

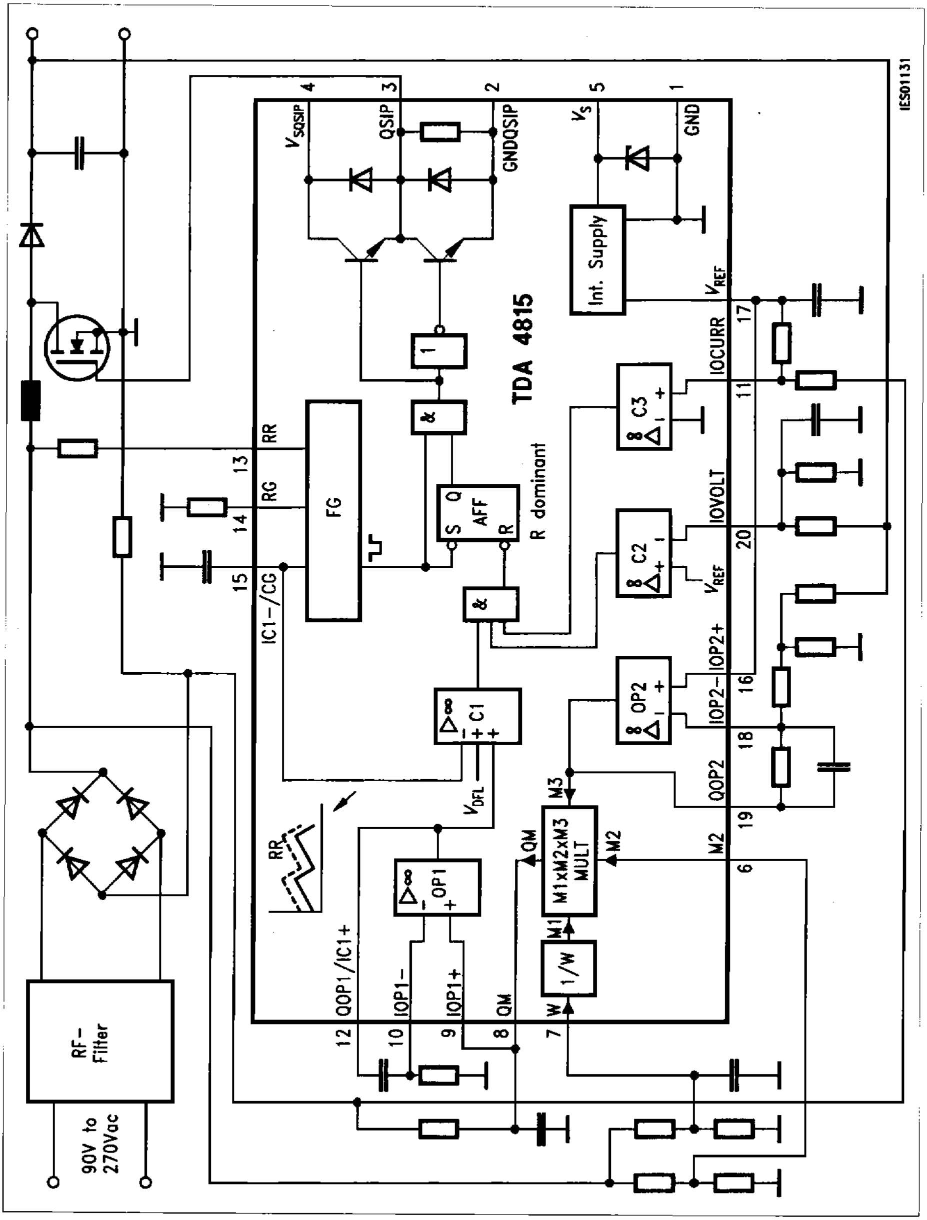
**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Delay Times (C1, C2, C3)** | | | | | | |
| Between input comp. and QSIP | $t$ [1] | | 200 | | ns | |
| **Frequency Generator** | | | | | | |
| Frequency range | $f$ | 0.05 | | 300 | kHz | |
| Frequency deviation | $\Delta f/f_O$ | | 1 | | % | $V_S = 12\ V \pm 20\ \%$ |
| Tolerance | $\Delta f/f_O$ | – 7 | | 7 | % | $C_G = 1$ nF; $f_O = 100$ kHz; $T_A = 25$ °C |
| Permissible charge current for $C_G$ = current on pin $R_G$ | $-I_{RG}$ | 0 | | 1 | mA | $I_{RG} = V_{REF/RG}$ |
| Discharge current on $C_G$ | $I_{dis}$ | | 3 | | mA | Set internally |
| Range of $C_G$ | $C_G$ | 0.05 | | 1000 | nF | |
| Minimum dead time | $t_D$ | | 300 | | ns | |
| Upper ramp voltage | $V_{Ru}$ | | 2.6 | | V | $I_{RR} = 0$ |
| Lower ramp voltage | $V_{Rl}$ | | 0.9 | | V | $I_{RR} = 0$ |
| Max. voltage on $C_G$ | $V_{CGH}$ | | 5.2 | | V | |
| Min. voltage on $C_G$ | $V_{CGL}$ | | 0.9 | | V | |
| Current on pin RR | $I_{RR}$ | 0 | | 300 | µA | $V_{RR}$ = appr. 1.7 V |
| Transfer ratio $V_{Shift}/I_{RR}$ | | | 25 | | mV/µA | $I_{RR} = 100$ µA |
| Duty factor limiting voltage on C1 | $V_{DFL}$ | | 3.5 | | V | |
| **Detector** | | | | | | |
| Upper switching voltage for voltage rising (H) | $V_{DETH}$ | | 2.6 | | V | |
| Lower switching voltage for voltage falling (L) | $V_{DETL}$ | | 2 | | V | |
| Input current | $-I_{DET}$ | | | 35 | µA | $V_{DETL} < V_{DET} < V_{DETH}$ |
| Clamping-diode current | $I_{DET}$ | – 3 | | 3 | mA | $V_{DET} > V_{DETH}$ or $V_{DET} < V_{DETL}$ |
| Switching hysteresis | $V_{DETHy}$ | | 0.6 | | V | |

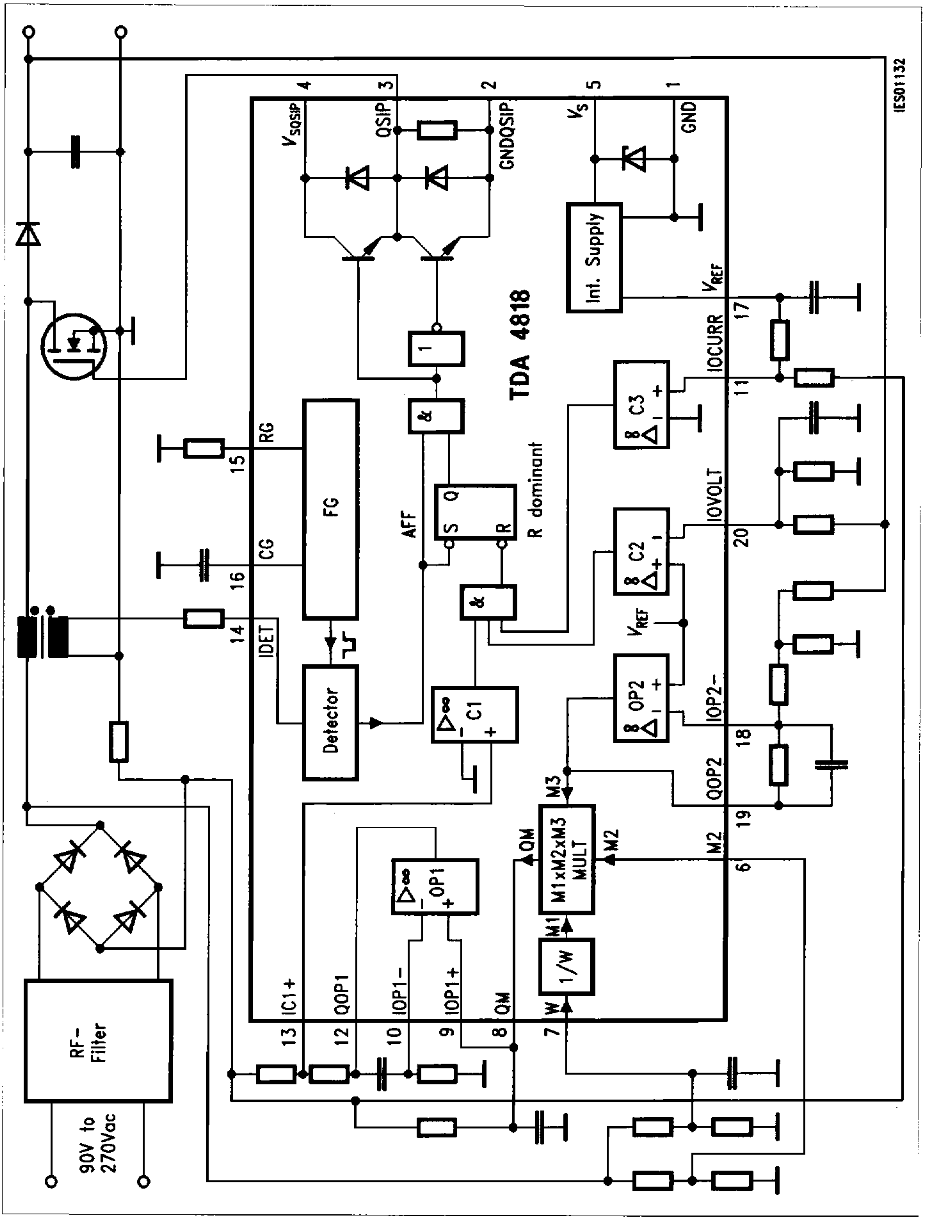
1) Step function on comparator input $\Delta V_{Comp}$ from – 100 mV to + 100 mV.



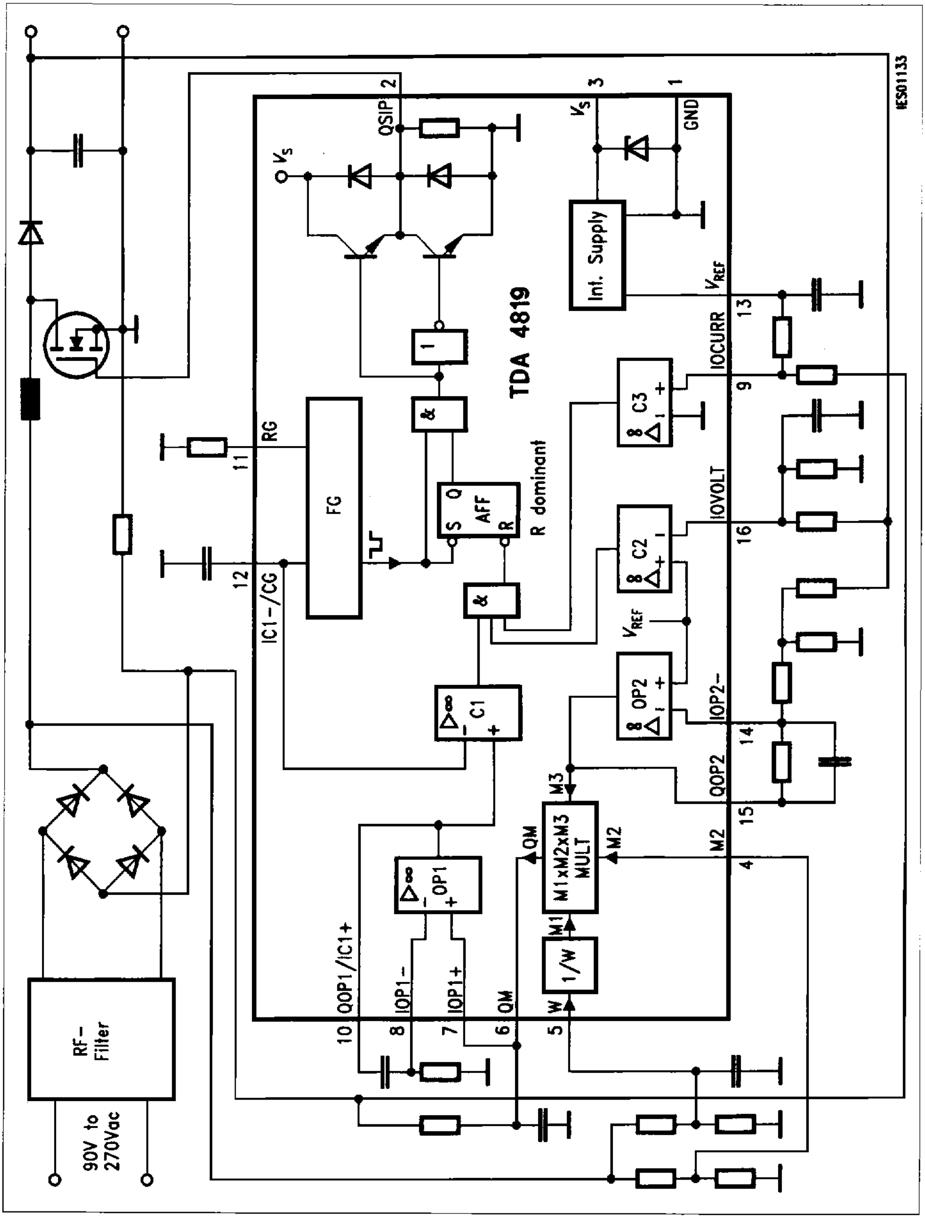

**Multiplier Transfer Characteristics**
$I_{QM} = f\,(V_{M2}, V_W, V_{M3} = V_{REF} + 1\text{ V})$




**Application Circuit 1 for Continuous Mode with TDA 4815**




**Application Circuit 2 for Discontinuous Mode with TDA 4818**




**Application Circuit 3 for Low-Cost Continuous Mode with TDA 4819**

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### Benefits of Preregulators with Power-Factor Controller in SMPS

- Power-factor correction increases the power available from the AC line by more than 35 % compared to conventional rectifier circuits. Circuit breakers and connectors become more reliable because of the lower peak currents.
- Wide-range power supplies are easier to implement for AC input voltages of 90 to 270 V without switch-over.
- Sinusoidal line current consumption and active harmonic filtering:
  Line harmonics are reduced to a minimum that the power factor is approaching 1 and all standards (IEC 555-2, EN 60555) are fulfilled.
- Stabilized DC output voltage:
  Preregulated DC output voltage provides optimal operating conditions for a subsequent converter.
- Reduced smoothing capacitance:
  For a given amplitude of the 100/120 Hz ripple voltage the smoothing capacitance can be reduced in comparison to a conventional rectifier circuit.
  Reduced choke size:
  Rectifier circuits capable of more than 200 W usually employ chokes to decrease the charging current ot the capacitor. These chokes are larger than those used in a preregulator with power-factor control.
- Higher efficiency:
  A preregulator does cause, some additional losses but these are more than compensated for by the cut in losses created by the rectifier configuration and the optimum operating conditions that are produced for a subsequent converter, even in the event of supply-voltage fluctuations.

### Summary of Effects of DC-Voltage Preregulation with Power Factor Control

| Parameter | Conventional Power Rectification | Power Rectification with Preregulator and Power-Factor Control |
|---|---|---|
| Mean DC supply voltage | 280 V | 340 V |
| Maximum DC supply voltage with line overvoltage | 350 V | 350 V |
| Minimum DC supply voltage with line undervoltage | 230 V | 330 V |
| Relative reverse voltage of diodes with line overvoltage | 1 | 0.7 |
| Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and line undervoltage | 1 | 2.06 |
| Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and rated supply voltage | 1 | 1.74 |
| Relative input capacitance with sustained ripple voltage | 1 | 0.3 to 0.5 |
| Power factor | 0.5 to 0.7 | 0.99 |

**Differences between Power-Factor Control Using Continuous Mode and Discontinuous Mode**

- Continuous Mode (TDA 4815, TDA 4819):
  This is best suited for medium and large power supplies with changing load conditions. The switching frequency is fixed, so the preregulator can synchronize the subsequent converter. A fast diode should be used to reduce switching losses.
- Discontinuous Mode (TDA 4818):
  This is best suited for small (≤ 200 W) power supplies with constant load conditions. The frequency is free-running and the ripple current of the supply slightly higher.