



Preliminary
STP1100BGA

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microSPARC™ -Ilep

DATA SHEET

SPARC v8 32-Bit Microprocessor With PCI/ DRAM Interfaces

DESCRIPTION

The microSPARC-Ilep 32-bit microprocessor is a highly integrated, high-performance microprocessor. Implementing the SPARC Architecture version 8 specification, it is ideally suited for low-cost uniprocessor embedded applications.

It is built with leading edge CMOS technology, with the core operating at a low voltage of 3.3V for optimized power consumption.

The microSPARC-Ilep includes on chip: integer unit (IU), floating-point unit (FPU), large separate instruction and data caches, a 32-entry version 8 reference MMU, programmable DRAM controller, PCI controller, PCI bus interface, a 16-entry IOMMU, flash memory interface support, interrupt controller, 2 timers, internal and boundary scan through JTAG interface, power management and clock generation capabilities.

The operating frequencies are 100 MHz.

Features

- Integrated 32-bit, 33 MHz PCI expansion bus controller
- Integrated 256 MByte DRAM controller
- Built-in 16 MByte flash memory controller
- SPARC high-performance RISC architecture
- Support for little and big endian byte ordering
- 8-window, 136-word register file
- 16 KByte instruction cache and 8 KByte data cache
- Built-in floating-point unit
- On-chip memory management unit
- Operating voltage of 3.3V with 5V compatible I/O
- Integrated power management circuitry
- IEEE 1149.1 (JTAG) boundary scan test bus

Benefits

- Connection to industry-standard expansion bus
- High-bandwidth memory controller to reduce latency
- Flash memory interface runs real-time operating systems that loads and runs code out of ROM
- Compatible with over 10,000 applications and existing development tools
- Handles with ease PCI devices designed for DOS machines, along with UNIX® applications
- Fast interrupt response, procedure calls, and program execution
- Decouples processor operation from slow external memory
- Supports concurrent execution of floating-point and integer instructions
- Support for sophisticated operating systems with memory protection and virtual addressing
- Low-power core reduces power consumption and supports industry-standard peripherals
- Consumes minimal power during standby
- Ease of manufacturing tests

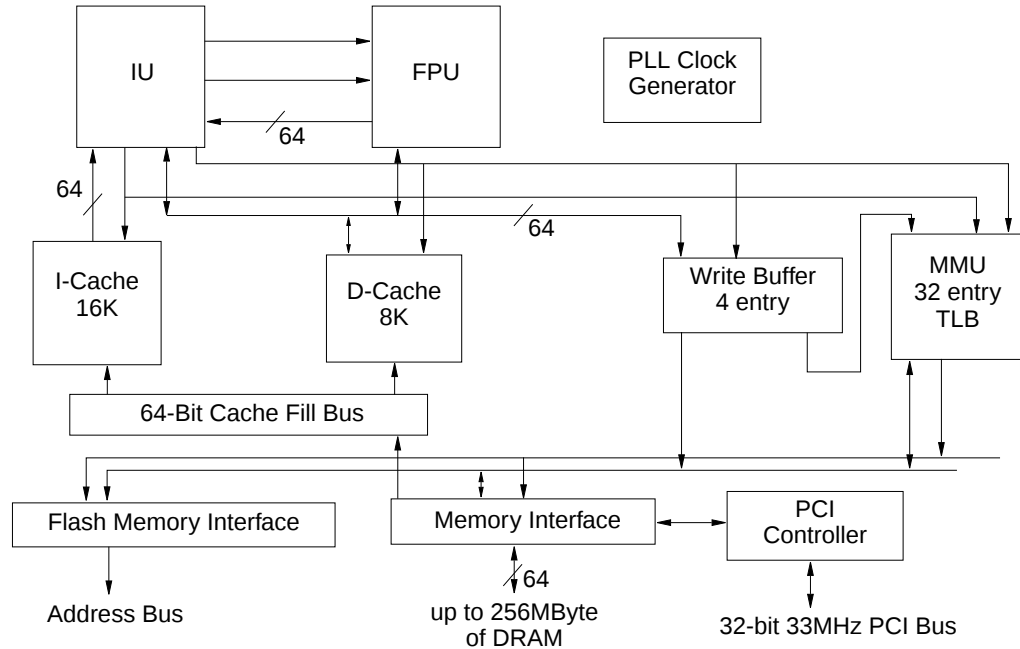


Figure 1. microSPARC-Ilep Block Diagram

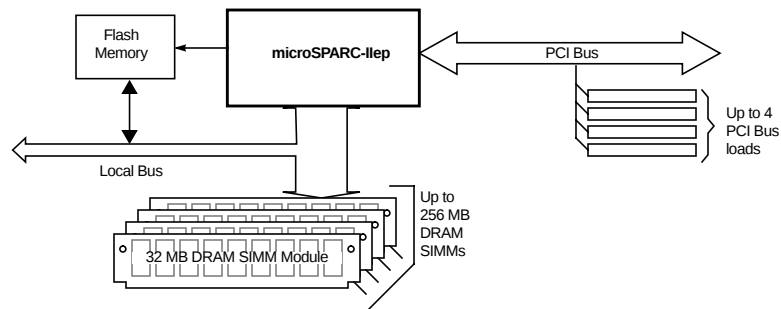


Figure 2. Typical microSPARC-Ilep System Block Diagram

TECHNICAL OVERVIEW

Integer Unit (IU)

The microSPARC-IIep integer unit executes SPARC integer instructions defined in the SPARC Architecture Manual version 8. The IU contains 136 registers supporting 8-window registers and 8-global registers. It has numerous high performance features include instruction prefetching, branch folding and 5-stage instruction pipeline. The IU supports little- and big-endian byte ordering of data.

Floating-Point Unit (FPU)

The floating-point unit executes all single- and double-precision floating-point instructions defined in the SPARC Architecture Manual version 8. The FPU traps on quad-precision instructions and transfers their execution to software. The FPU contains a floating-point core based on Meiko design, a fast-multiplier, a 3-instruction deep instruction queue, and 32 32-bit floating-point registers. The floating-point core and fast multiplier allow parallel execution of floating multiplication (FPMUL) and another floating-point instruction while the instruction queue support concurrent execution of floating-point and integer instruction.

Memory Management Unit (MMU)

The microSPARC-IIep memory management unit translates 32-bit virtual addresses to 31-bit physical address. It maps physical address into 8 different address spaces. The MMU provides functionalities specified in the SPARC version 8 Reference MMU and implements hardware table-walk. It implements a 32-entry fully-associative translation lookaside buffer (TLB) and provides memory protection for 256 contexts.

Instruction Cache

The instruction cache is a 16 KByte, direct-mapped, virtually-indexed, virtually-tagged cache. The instruction cache is organized as 512 lines of 32 bytes plus 32 tag bits. To reduce read-miss latency, the instruction cache supports cache refill in two 32-bit words, streaming and bypass.

Data Cache

The data cache is an 8-KByte, direct-mapped, virtually-indexed, virtually-tagged cache. Cache write policy supported is write-through with no write-allocate. The data cache is organized as 512 lines of 16 bytes plus 32 tag bits. The data cache provides zero-penalty data accesses for cache hits.

To reduce write latency, the data cache contains a 4-deep double-word store buffer. To reduce read-miss latency, the data cache supports cache refill in two 32-bit words, streaming and bypass.

DRAM Interface

The microSPARC-IIep DRAM interface supports industry standard fast-page mode DRAM and EDO DRAM that support fast-page mode. It supports 8 banks of memory up to a total of 256 MBytes of system memory. Each bank of memory can be consisted of 8 MBytes, 16 MBytes or 32 MBytes. The DRAM interface is programmable and support different memory speeds relative to the processor frequency.

The DRAM data bus is 64 bits wide with two parity bits, each covering 32-bits of data. The parity bits can be disabled.

The DRAM interface provides a programmable DRAM refresh controller that supports $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh.

PCI Bus Interface

The PCI bus interface complies with the industry standard PCI Local Bus Specification version 2.1. It provides a 32-bit 33MHz bus interface. Its features include endian conversion for different data byte ordering, PCI Host and Satellite mode, a dedicated 16-entry translation lookaside buffer (TLB) dedicated for I/O transactions, a PCI arbiter, and PCI clock, reset and interrupt handler. As a PCI Host, microSPARC-IIep performs PCI bus arbitration, PCI clock, reset and interrupt handling. As a PCI Satellite, microSPARC-IIep relinquishes the PCI Host functionalities to the external PCI Host.

Other features supported by the PCI Bus interface include:

- Programmed input/output (PIO) transactions between the microSPARC-IIep and external PCI devices.
- PCI Host or Satellite mode selected by input pins during power-up.
- Programmable configuration of external PCI devices (Type 0 and Type 1) while under PCI Host mode.
- Programmable configuration by external PCI Host while under PCI Satellite mode.
- Buffers with matching fill and drain rate allow extended burst transfers.
- Direct transactions between PCI masters and PCI slaves.
- Two PCI bus fairness access arbitration protocols: same-level round robin and three-level round robin.
- Direct virtual memory access (DVMA) transactions between PCI masters and the microSPARC-IIep slave memory interface (referred to as PCI DVMA) using the software-controlled IOTLB to generate physical DRAM addresses.
- Booting from the PCI Bus from address selected by user.
- While under standby mode to reduce power consumption, the PCI interface consumes minimal power to support clock generation and wake-up when interrupted.
- Two 32-bit timers or one 32-bit timer and one 64-bit counter available.
- Interrupt handler supports up to eight programmable interrupt input/output lines.

Flash Memory Interface

Using an industry-standard programming algorithm, the microSPARC-IIep flash memory interface is compatible with 28FxxxXX flash memory devices. The interface has a programmable latency to allow flash memory access time of up to 45 processor clocks. After power-up, the default latency of the interface is 45 processor clocks. It can then be programmed to have an access latency from 6 to 45 processor clocks in increments of 3 processor clocks.

The flash memory interface supports up to 16MBytes of data. It supports both 32-bit and 8-bit data accesses as selected by a boot-mode select input pin. microSPARC-IIep is pin-selectable to boot from the flash memory interface or the PCI address space.

JTAG Test Bus Interface

The microSPARC-IIep provides a five-wire test access port (TAP) interface to support boundary scan and clock control. This interface is compatible with IEEE 1149.1 specification, *IEEE Standard Test Access Port and Boundary Scan Architecture*. This allows efficient access to any single chip in a scan daisy-chain without board-level multiplexing.

TAP Controller

The TAP controller is a synchronous finite state machine (FSM) which controls the sequence of operations of the JTAG test circuitry, in response to changes on the JTAG bus. The TAP controller is asynchronous with respect to the system clocks, and can therefore be used to control the clock control logic.

The TAP FSM implements the state (16 states) diagram as detailed in the IEEE 1149.1 specification.

Power Management

microSPARC-IIep can detect system inactivity, and place itself in a standby mode to reduce power consumption. While in standby mode, the processor consumes minimal power. However, the PCI interface remains active and any PCI activity will wake up the processor.

SIGNAL DESCRIPTIONS [1]

PCI Signals

Signal	Type	Note	Description
PCI_CLK[3:0]	Out	2.	Clock output pin. Under PCI Host mode, provide clock to other PCI devices. Under PCI Satellite mode, signal is unconnected.
PCI_RST#	I/O	2.	Reset. Under PCI Host mode, provides RESET to other PCI devices. Under PCI Satellite mode, signal is input.
AD[31:0]	I/O	2.	Address and Data pins (multiplexed).
CBE[3:0]#	I/O	2.	Bus Command and Byte Enables pins (multiplexed).
PAR	I/O	2.	Parity. Even parity across AD[31:0] and CBE[3:0]#.
FRAME#	I/O	2.	Frame. Driven by current master to indicate beginning and duration of an access.
IRDY#	I/O	2.	Initiator Ready. Driven by bus master to complete the current data phase of the transaction.
TRDY#	I/O	2.	Target Ready. Driven by target to complete the current data phase of the transaction.
STOP#	I/O	2.	Stop. Request from current target to stop the current transaction.
DEVSEL#	I/O	2.	Device Select. Driven by device that has decoded its address as a target.
PERR#	I/O	2.	Parity Error.
SERR#	I/O	6.	System Error. Generates a level 15 interrupt (open drain drivers)

1. These notes apply to the pin description tables in this section:

Note 1: Pin uses clipping reference VDD3.

Note 2: Pin uses clipping reference VDD2.

Note 3: Pin has low power driver and may require an external buffer to provide sufficient drive.

Note 4: Pin is 5 Volt tolerant and internally biased to VSS1 when not connected.

Note 5: Pin is 5 Volt tolerant and internally biased to VDD1 when not connected.

Note 6: Bidirectional open-drain driver, requires external pull up and uses clipping reference VDD2.

Note 7: Pin is 5 Volt tolerant.

Note 8: The EXT_CLK1 pin may not be driven above 5.0 volts. If this signal is driven with a PCI bus driver, it must be clamped externally to 5.0 volts.

PCI Signals (Continued)

Signal	Type	Note	Description
PCI_INT_L[7:0] (IRL_L[3:0])	I/O	6.	Interrupt Requests. Sent to the microSPARC-Ilep interrupt controller. If the PCI internal interrupt controller is disabled, interrupt requests can be triggered by software and sent to an external interrupt controller. For PCI, the interrupt signals should be connected as following: INTH#: PCI_INT_L[7] INTD#: PCI_INT_L[3] INTG#: PCI_INT_L[6] INTC#: PCI_INT_L[2] INTF#: PCI_INT_L[5] INTB#: PCI_INT_L[1] INTE#: PCI_INT_L[4] INTA#: PCI_INT_L[0] If PCI_INT_L[7:4] are used in a 5 volt PCI bus, the inputs have the potential of driving to greater than 5 volts and external clamping diodes to 5 volts are required (PCI_INT_L[3:0] are internally clipped to VDD2). If the PCI internal interrupt controller is disabled, PCI_INT_L[3:0] can be used to function as the SPARC interrupt request lines (IRL[3:0]) as defined in SPARC version 8.
PCI_REQ[3:0]#	In	2.	Bus Request. In PCI Host mode, microSPARC-Ilep internal PCI bus arbiter receives REQ# from other PCI masters. In PCI Satellite mode, PCI_REQ#[0] functions as PCI Bus Grant signal (SAT_GNT_L) and PCI_REQ#[1] functions as PCI Initialization Device Select signal (IDSEL). The remaining PCI_REQ#[3:2] signals should be tied high.
PCI_GNT[3:0]#	Out	2.	Bus Grant. In PCI Host mode, microSPARC-Ilep internal PCI bus arbiter sends GNT# to other PCI masters. In PCI Satellite mode, PCI_GNT#[0] functions as PCI Bus Request signal (SAT_REQ_L).

DRAM and Flash Memory Signals

Signal	Type	Note	Description
MEMDATA[63:0]	I/O	1.	64-bit bi-directional memory data bus accesses DRAM and flash memory. [31:0] or [7:0] are used dependent on width of flash memory interface.
MEMPAR[1:0]	I/O	1.	Bi-directional memory data parity pins for DRAM only. [0] is for MEMDATA[31:0] while [1] is for MEMDATA[63:32]. Parity is optional.
MEMADDR[11:0]	Out	3.	DRAM Address output pins. Require external buffering to provide the sufficient drive.
RAS_L[7:0]	Out	3.	DRAM Row Address Strobe. Eight separate RAS signals to support eight banks of DRAM. Require external buffering to provide sufficient drive.
CAS_L[3:0]	Out	3.	DRAM Column Address Strokes. Two pairs of CAS signals with each pair supporting four banks of DRAM. Require external buffering to provide sufficient drive.
MWE_L	Out	3.	DRAM Write Enable output pin. Require external buffering to provide sufficient drive.
MOE_L	Out	3.	DRAM Output Enable output pin. Require external buffering to provide sufficient drive.
SIMM32_SEL	In	4.	DRAM Double-Density SIMM and DIMM select. Disables dual-RAS mode under fast-page mode.
ROM_ADDR[23:0]	Out	3.	Flash memory Address bus (Byte address).

DRAM and Flash Memory Signals (Continued)

Signal	Type	Note	Description
ROM_CS_L	Out	3.	Flash memory Chip Select.
ROM_OE_L	Out	3.	Flash memory Output Enable.
ROM_WE_L	Out	3.	Flash memory Write Enable.

Clock and Timing Signals

Signal	Type	Note	Description
DIV_CTL[1:0]	In	4.	These two input pins set the multiplication factor for the EXT_CLK1 clock input pin to the internal processor clock and internal system clock as shown in <i>Table 2</i> .
SP_SEL[2:0]	In	4.	Memory Speed Select. Selects memory interface timing. Refer to <i>Table 3</i> for settings.
REF_CLOCK	Out	3.	Clock output at frequency of processor core. Used for testing and monitoring.
EXT_CLK1	In	8.	External Input Clock 1. While under PLL-bypass mode, an EXclusiveOR is performed on EXT_CLK1 and EXT_CLK2 to produce the processor clock. Otherwise, EXT_CLK1 is used to produce the processor clock using the Phase-Locked Loop.
EXT_CLK2 (MODE select)	In	4.	External Input Clock 2. While under PLL-bypass mode, an EXclusiveOR is performed on EXT_CLK1 and EXT_CLK2 to produce the processor clock. Otherwise, during power-up, EXT_CLK2 is used to select PCI Host or Satellite mode. Therefore, while PLL is not bypassed, if EXT_CLK2 is tied high, microSPARC-IIep functions in PCI Satellite mode. microSPARC-IIep functions in PCI Host mode by default.
PLL_BYP_L	In	5.	PLL-bypass mode select. When tied high during power-up, microSPARC-IIep output of Phase-Locked Loop is used to generate processor clock. When tied low during power-up, PLL-bypass mode is selected and the processor clock is generated using EXclusiveOR of EXT_CLK1 and EXT_CLK2.
PLL_RST	In	5.	Low until VDD1 > 2.0V and for 2 us or more when power-up.

JTAG Signals

Signal	Type	Note	Description
JTAG_CK	In	5.	Clock for boundary scan registers.
JTAG_MS	In	5.	Mode Select.
JTAG_TDI	In	5.	Test Data Input.
JTAG_TRST_L	In	4.	Test Reset.
JTAG_TDO	Out	3.	Test Data Output.

Miscellaneous Signals

Signal	Type	Note	Description
INPUT_RESET_L	In	4.	Power-up reset input pin.
BM_SEL[1:0]	In	4.	Boot Mode Select. 00 = 32-bit flash memory on local memory bus (cacheable after boot). 01 = 8-bit flash memory on local memory bus (cacheable after boot). 10 = PCI memory fetch from addresses f000.0000 - f0ff.ffff (non-cacheable). 11 = PCI memory fetch from addresses ffe.0000 - ffff.ffff (non-cacheable). After booting from PCI (BM_SEL[1:0] = 10 or 11) the Flash memory defaults to the 32-bit flash memory interface.
EXT_EVENT_L	In	5.	Input pin that can be used to stop internal clocks based on an external trigger.
INT_EVENT_L	Out	3.	Output pin that can be used to trigger external events based on an internal trigger.
IIDDTN	In	7.	Reserved for test Tie to VSS1 for normal operation.
TN	In	7.	Reserved for test. Tie to VDD1 for normal operation.
THERM_D	In	7.	Reserved for test. Tie to VSS1 for normal operation
SCAN_MODE	In	7.	Reserved for test. Tie to VSS1 for normal operation.
PROCMON	Out		Reserved for test. Do Not Connect.
VDD4, VSS4	In		PLL power/ground.
VDD2,VDD3	In		Reference power.
VDD1, VSS1	In		Core power/ground.

TIMING CONSIDERATIONS

TABLE 1: Timing Settings for DRAM Speeds ^[1]

Core Frequency	100 MHz	
PCI Frequency	25 MHz	33 MHz
60ns DRAM	DIV_CTL[1:0]=10 SP_SEL[2:0]=010	DIV_CTL[1:0]=01 SP_SEL[2:0]=010

1. See *Table 2* for DIV_CTL settings and *Table 3* for SP_SEL settings.

TABLE 2: Processor Interface Timing

DIV_CTL[1:0]	Multiply Factor of EXT_CLK1
01	x3
10	x4
11	x5
00	x6

TABLE 3: Memory Interface Timing

Signal	Description (SP_SEL[2:0] = 1xx reserved)	Number of Cycles ^[1]			
		SP_SEL[2:0] = 000	SP_SEL[2:0] = 001	SP_SEL[2:0] = 010	SP_SEL[2:0] = 011
t_ASC	Column address sent before $\overline{\text{CAS}}$	1	3	3	4
	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (refresh)	1.5	1.5	2.5	3.5
t_CAS	$\overline{\text{CAS}}$ active (read)	3	4	4	5
	$\overline{\text{CAS}}$ active (write)	2	3	3	3
t_CP	$\overline{\text{CAS}}$ precharge (read)	1	1	2	2
	$\overline{\text{CAS}}$ precharge (write)	2	3	3	3
t_DH, t_WCH, t_DH	Data, $\overline{\text{WE}}$, parity hold after $\overline{\text{CAS}}$	2	3	3	3
t_DS, t_WCS, t_DS	Data, $\overline{\text{WE}}$, parity sent before $\overline{\text{CAS}}$	1	2	2	2
t_RAS	$\overline{\text{RAS}}$ active (read)	7.5	8.5	9.5	11.5
	$\overline{\text{RAS}}$ active (write)	5.5	8.5	8.5	9.5
	$\overline{\text{RAS}}$ active (refresh)	6.5	6.5	6.5	8.5
t_RP	$\overline{\text{RAS}}$ precharge	3.5	3.5	4.5	5.5

1. The timing diagrams in *Figure 4* through *Figure 13* reflect a SP_SEL[2:0] of 010 for 100 MHz operation.

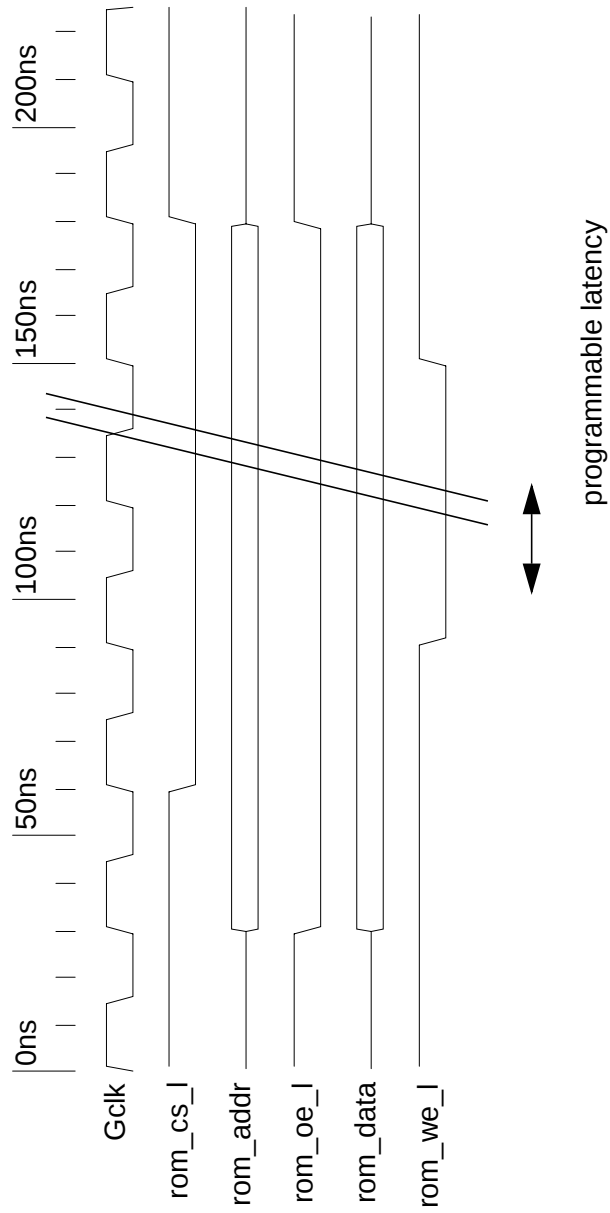


Figure 3. Flash Memory Interface

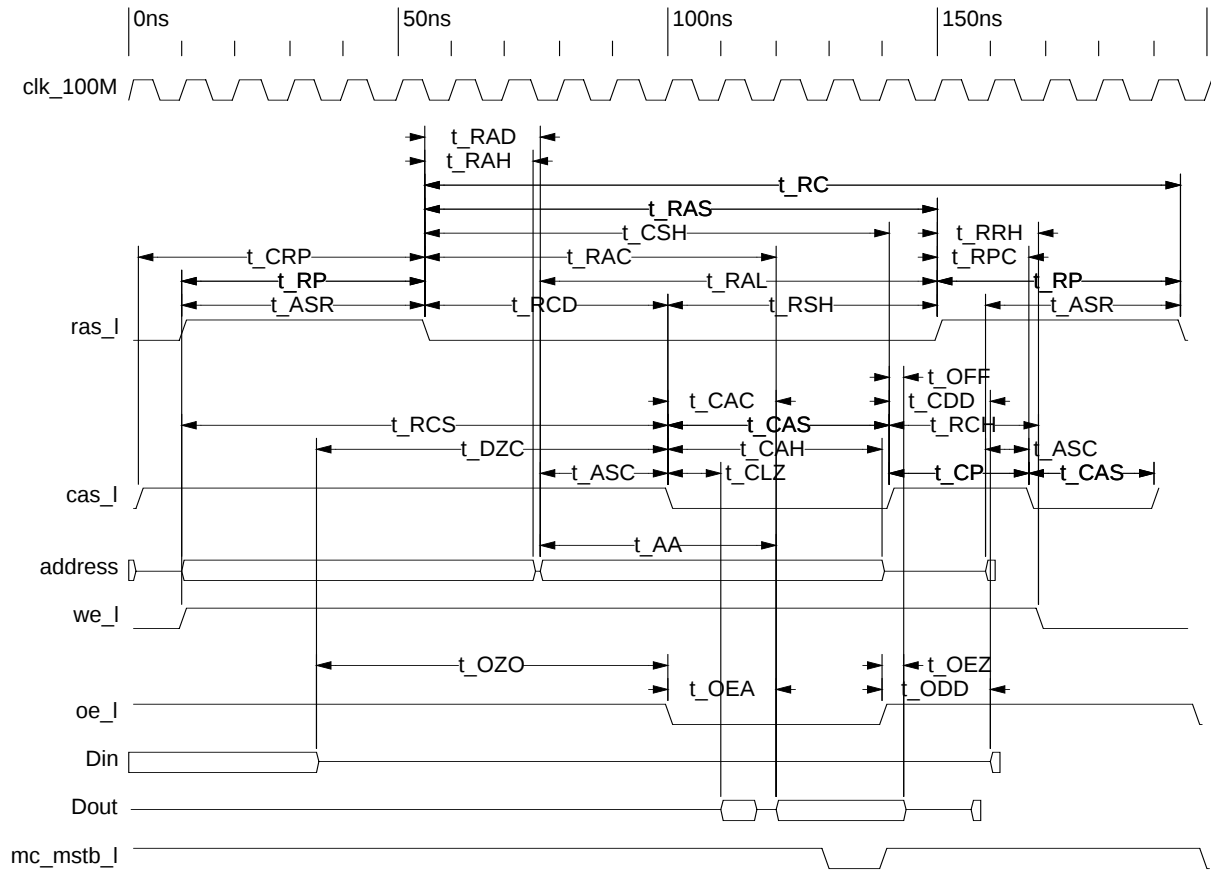


Figure 4. DRAM Read Cycle (100 MHz Clock)

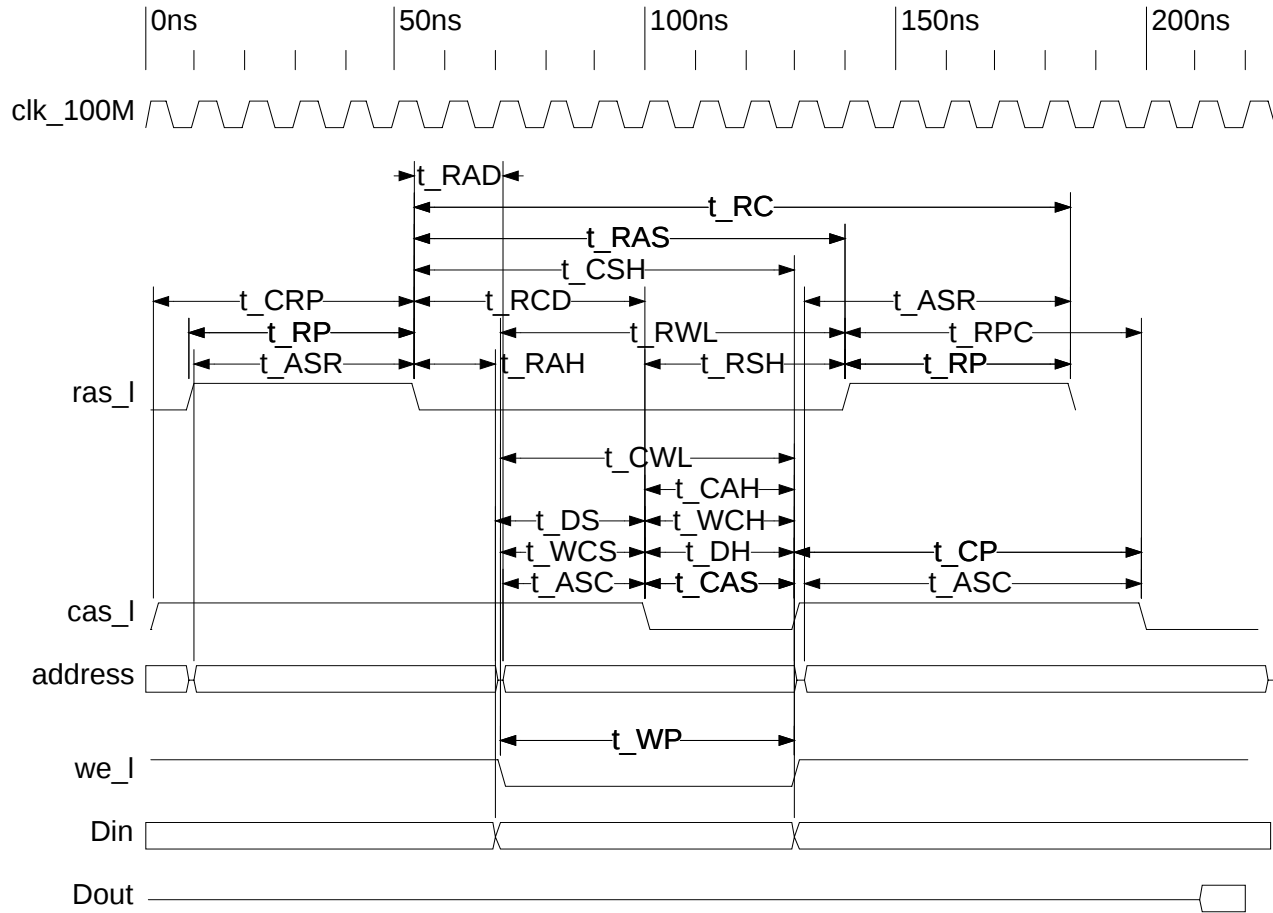


Figure 5. DRAM Write Cycle (100 MHz Clock)

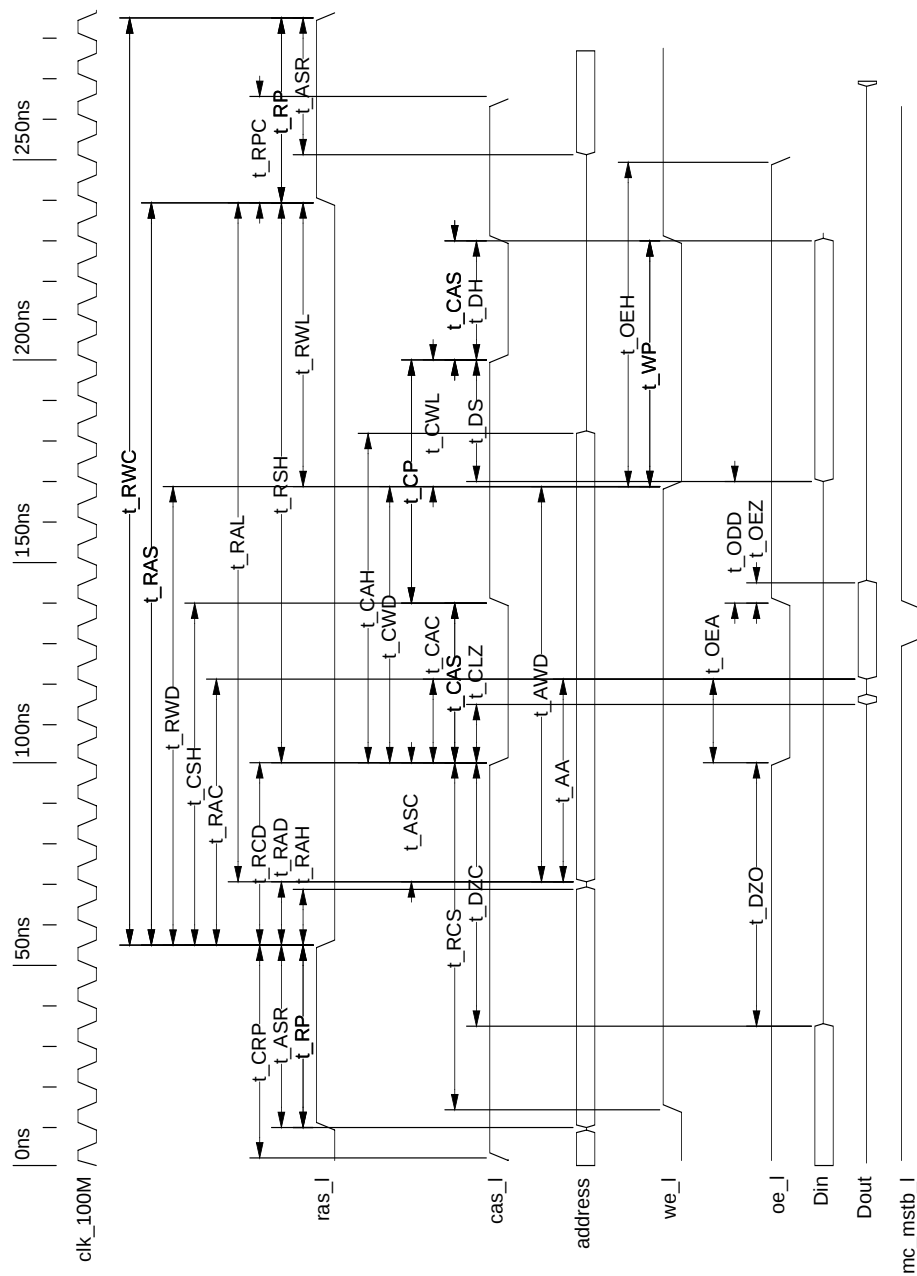
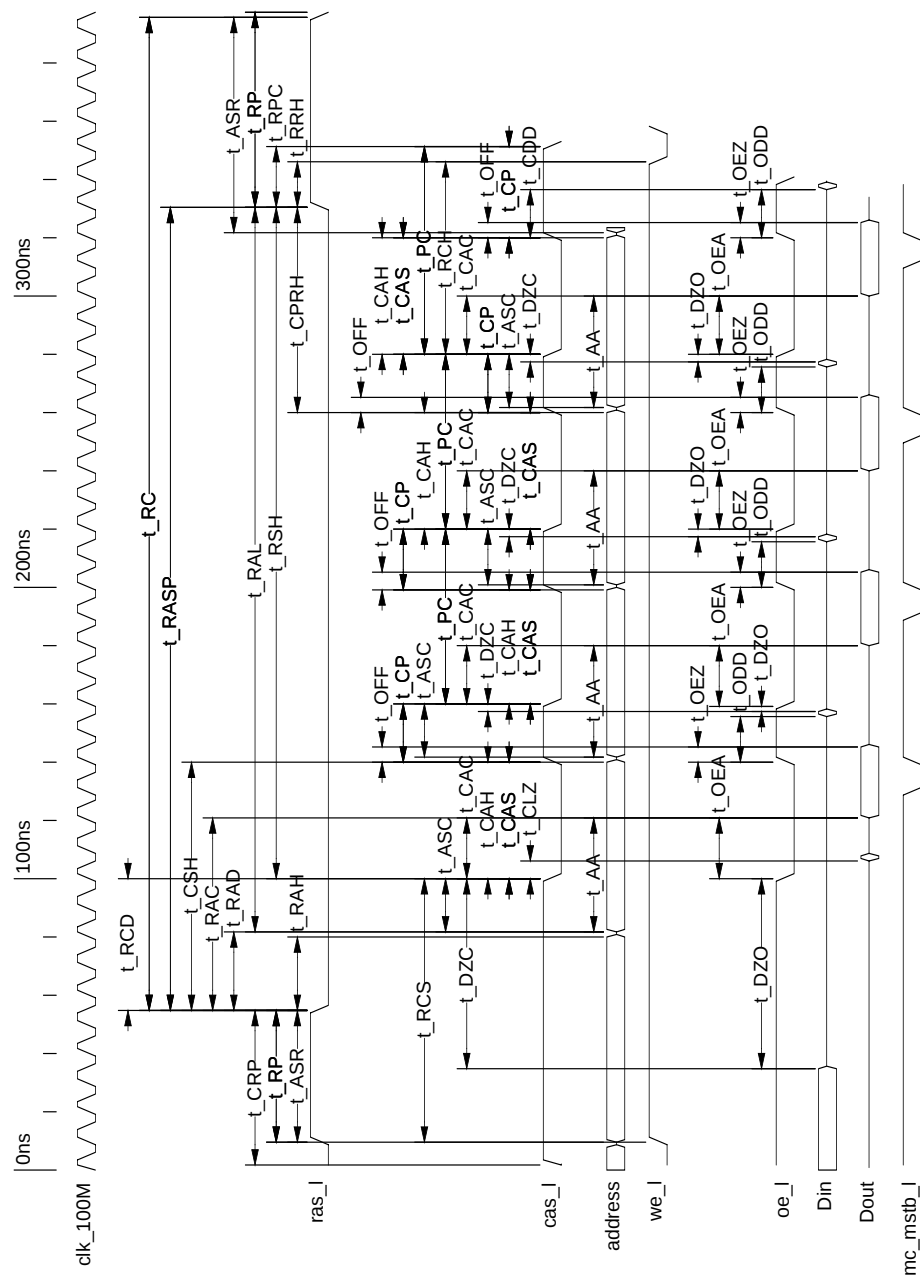


Figure 6. DRAM Read-Modify-Write Cycle (100 MHz Clock)



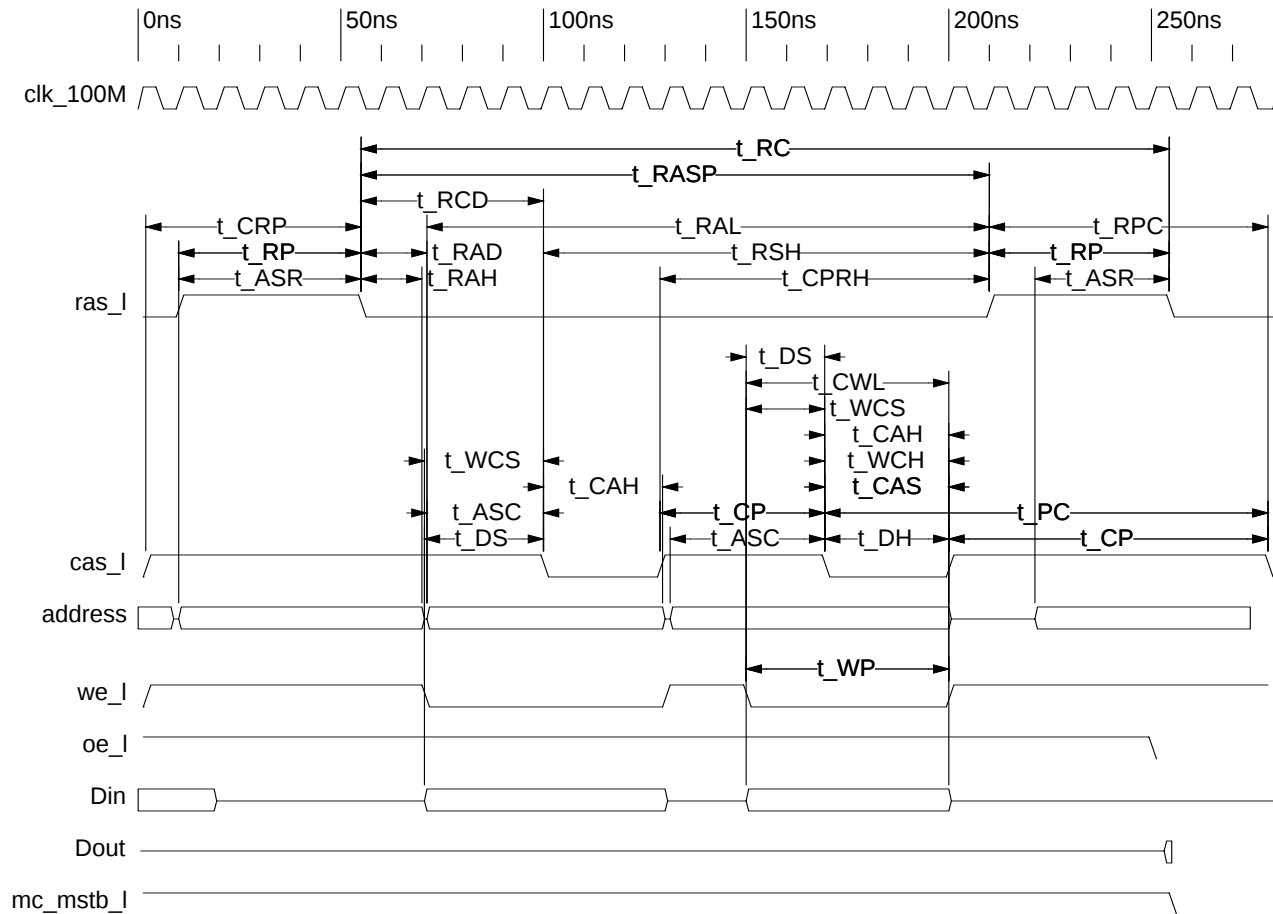


Figure 8. DRAM Page-Mode Write Cycle (100 MHz Clock)

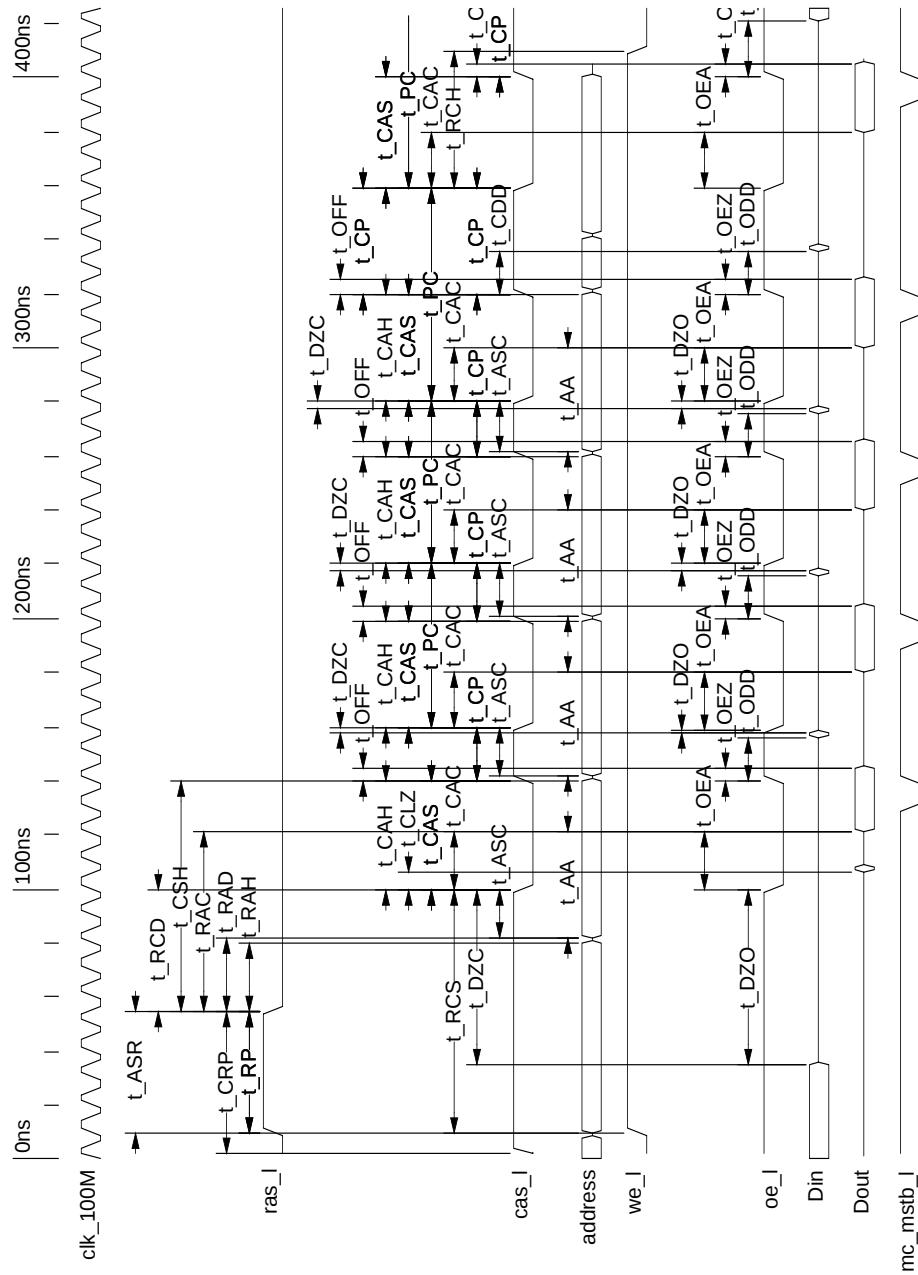


Figure 9. DRAM Read After a Page-Mode Read (100 MHz Clock)



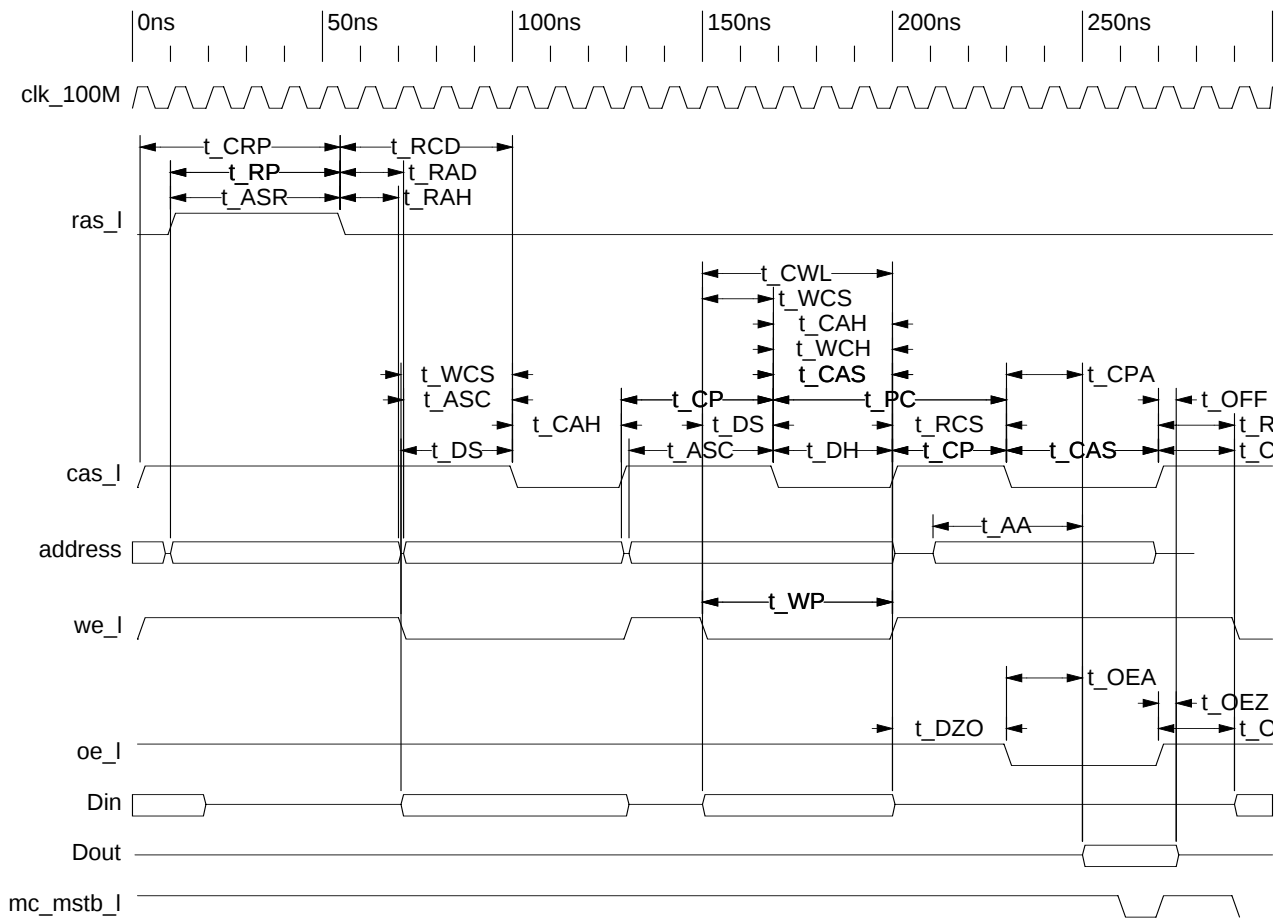


Figure 11. DRAM Read After a Page-Mode Write (100 MHz Clock)

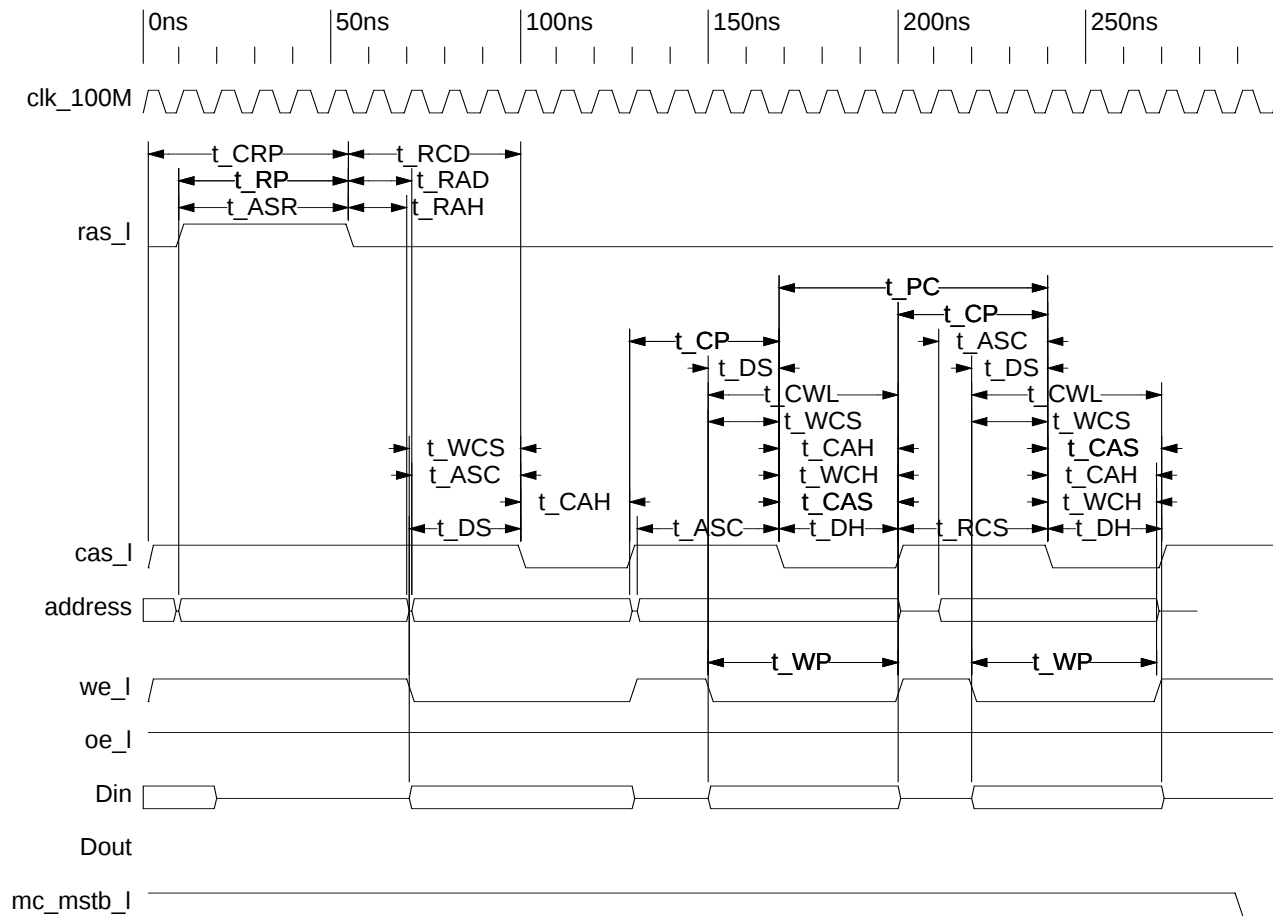


Figure 12. DRAM Write After a Page-Mode Write (100 MHz Clock)

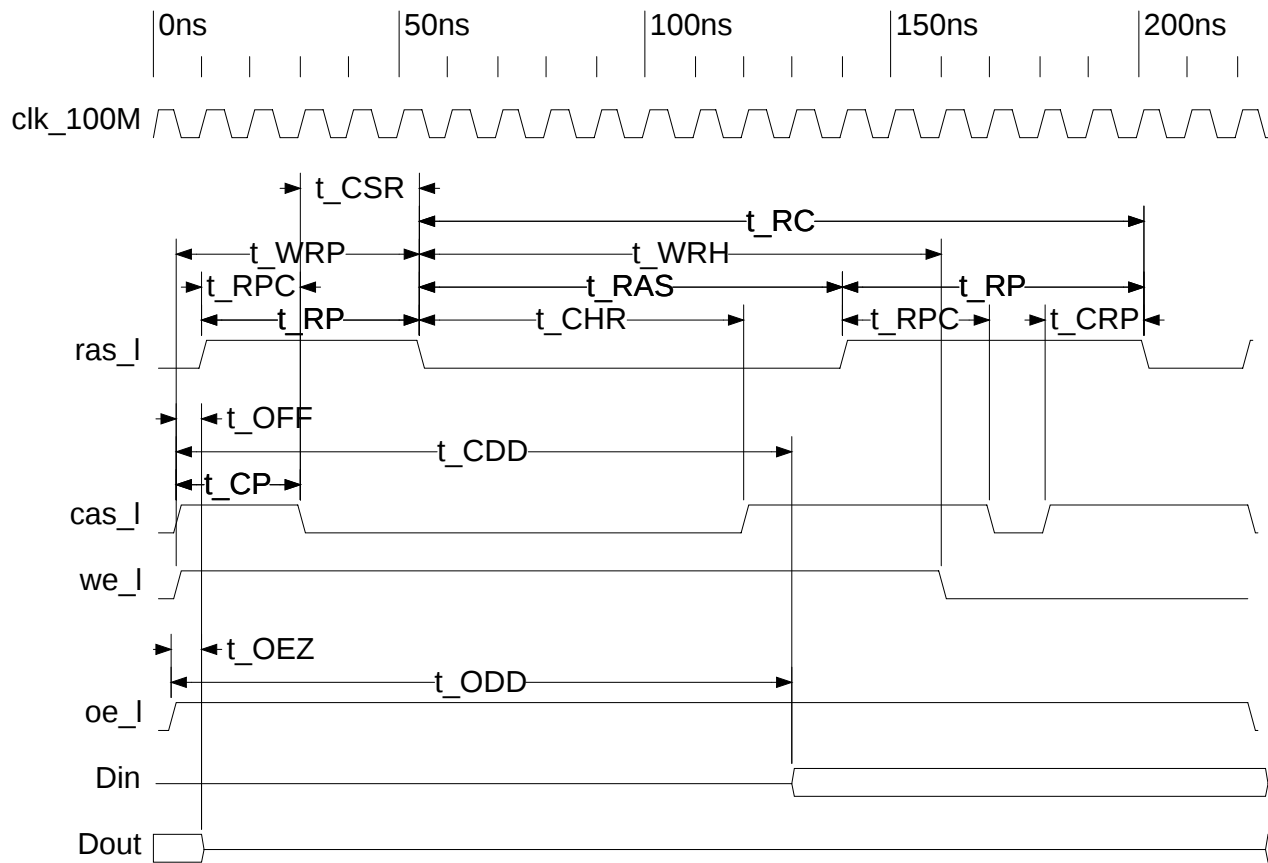


Figure 13. DRAM RAS-Before-CAS Refresh Cycle (100 MHz Clock)

ELECTRICAL SPECIFICATIONS ^[1]

Absolute Maximum Ratings ^[1]

Parameter	Symbol	Min	Max	Units
Supply voltage	V _{DD1}	-0.5	4	V
Reference Voltage	V _{DD2} , V _{DD3}			
PLL supply voltage	V _{DD4}			
Input voltage (any pin)	V _{IN}	-0.5		V
Input clamp current (any pin)	I _I	-20	20	mA
Operating junction temperature	T _J	0	105	C
Storage temperature	T _S	-40	125	C
Static discharge voltage		–	2000	V

1. Operation of the device at values in excess of those listed above may result in degradation or destruction of the device. Extended operation at the absolute maximum ratings may degrade the reliability of the product. All voltages are defined with respect to ground.

TABLE 4: Recommended Operating Conditions: ^[1]

Parameter		Symbol	100 MHz			Units
Core supply voltage		V _{DD1}	3.14	3.3	3.47	V
I/O reference voltage	PCI	V _{DD2}		3.3/5.0		V
	MEMDATA	V _{DD3}		3.3/5.0		V
PLL voltage	supply	V _{DD4}	3.14	3.3	3.47	V
	ground	V _{SS4}	-0.2	0	0.2	V
Ground		V _{SS1}	-0.2	0	0.2	V
DC I/O voltage	PCI		0	–	V _{DD2}	V
	MEMDATA		0	–	V _{DD3}	V
Operating case temperature		T _C	0	–	80	C

1. The microSPARC-IIep is designed with TTL compatible I/O.

Note: The following AC and DC characteristics are preliminary and for reference only.

1. These electrical specification numbers are preliminary, and are shown for reference only and are subject to change.

TABLE 5: DC Characteristics ($V_{CC} = V_{DD2}$ or V_{DD3})

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage		2.0	—	$V_{CC} + 0.2$	V
V_{IL}	Input low voltage		-0.5	—	0.8	V
V_{OH}	Output high voltage	$I_{OH} = 4.0 \text{ mA}$, $V_{CC} = \text{Min}^{[1]}$	2.4	—	—	V
		$I_{OH} = 5.0 \text{ mA}$, $V_{CC} = \text{Min}^{[2]}$	2.4	—	—	V
		$I_{OH} = 8.0 \text{ mA}$, $V_{CC} = \text{Min}^{[3]}$	2.4	—	—	V
V_{OL}	Output low voltage	$I_{OL} = 4.0 \text{ mA}$, $V_{CC} = \text{Min}^{[1]}$	—	—	0.4	V
		$I_{OL} = 5.0 \text{ mA}$, $V_{CC} = \text{Min}^{[2]}$	—	—	0.4	V
		$I_{OL} = 8.0 \text{ mA}$, $V_{CC} = \text{Min}^{[3]}$	—	—	0.4	V
I_{IN}	Input current	$V_{IN} = V_{CC}$ or GND	-10	—	10	μA
		$V_{IN} = V_{CC}$ or GND	-500	—	10	μA
I_{OZ}	Output leakage current	$V_{OUT} = V_{CC}$ or GND, Outputs disabled	-10	—	10	μA
W_D	Power dissipation	V_{DD1} , V_{DD2} , $V_{DD3} = \text{max}$, $f = 100 \text{ MHz}$	—	—	4	W

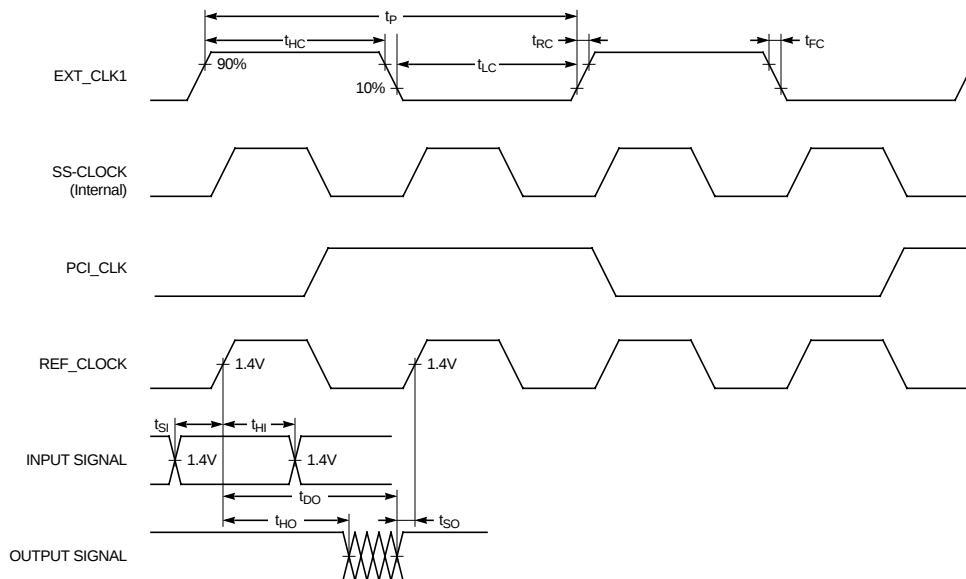
1. REF_CLOCK, JTAG_TDO, MEMADDR, RAS_L, CAS_L, MWE_L, MOE_L outputs only.

2. For each line of PCI_CLK output only.

3. MEMPAR, MEMDATA outputs only.

TABLE 6: Capacitance

Symbol	Parameter	Max	Units
C_{IN}	Input capacitance (Non-PCI pins)	15	pF
C_{OUT}	Output capacitance (Non-PCI pins)	10	pF
C_{BI}	Bidirectional capacitance (Non-PCI pins)	15	pF
C_{IN}	Input capacitance PCI pins	10	pF
C_{OUT}	Output capacitance PCI pins	10	pF
C_{BI}	Bidirectional capacitance PCI pins	10	pF



Parameter Definitions

- t_{SI} : Required setup time of a chip input referenced to a given (clock) edge.
- t_{HI} : Required hold time of a chip input referenced to a given (clock) edge.
- t_{DO} : Guaranteed propagation time of an output referenced to a given (clock) edge.
- t_{HO} : Guaranteed hold time of an output referenced to a given (clock) edge.
- t_{SO} : Guaranteed setup time of an output referenced to a next given (clock) edge.
- t_{HC} : Required clock high time.
- t_{LC} : Required clock low time.
- t_{RC} : Required clock rise time.
- t_{FC} : Required clock fall time.

Figure 14. Timing Waveforms

TABLE 7: AC Characteristics (Input Pins)

Pin Name	Symbol	Conditions	Reference Edge	100 MHz		Unit
				Min	Max	
JTAG_CK	t _{HC}	1 MHz - 10 MHz	asynch	25	—	ns
	t _{LC}		asynch	25	—	ns
	t _{RC}		asynch	—	10	ns
	t _{FC}		asynch	—	10	ns
JTAG_MS	t _{SI}		JTAG_CK+	10	—	ns
	t _{HI}		JTAG_CK+	0	—	ns
JTAG_TDI	t _{SI}		JTAG_CK+	10	—	ns
	t _{HI}		JTAG_CK+	0	—	ns
JTAG_TRST_L	t _{SI}	2 cycles	JTAG_CK+	10	—	ns
	t _{HI}		JTAG_CK+	0	—	ns
EXT_CLK1 ^[1]	t _p			30	—	ns
	t _{HC}				—	ns
	t _{LC}				—	ns
	t _{RC}			—		ns
	t _{FC}			—		ns
INPUT_RESET_L	t _{SI}	32 cycles and 1.1 ms for PCI	REF_CLOCK+	5	—	ns
	t _{HI}		REF_CLOCK+	1	—	ns
EXT_EVENT_L	t _{SI}		REF_CLOCK+	7		ns
	t _{HI}		REF_CLOCK+	1		ns

TABLE 7: AC Characteristics (Input Pins) (Continued)

Pin Name	Symbol	Conditions	Reference Edge	100 MHz		Unit
				Min	Max	
BM_SEL[1:0]	t _{SI}		REF_CLOCK+	5	—	ns
	t _{HI}		REF_CLOCK+	1	—	ns
PCI_INT_L[7:0]	t _{SI}	2 cycles	REF_CLOCK+	5	—	ns
(IRL[3:0])	t _{HI}		REF_CLOCK+	1	—	ns
PCI BDI's Refer to PCI Specification 2.1	t _{SI} t _{HI}					
AD[31:0]		10 pF	PCI_CLK+	7		ns
FRAME#		10 pF	PCI_CLK+	7		ns
TRDY#		10 pF	PCI_CLK+	7		ns
IRDY#		10 pF	PCI_CLK+	7		ns
STOP#		10 pF	PCI_CLK+	7		ns
DEVSEL#		10 pF	PCI_CLK+	7		ns
CBE[3:0]#		10 pF	PCI_CLK+	7		ns
PAR		10 pF	PCI_CLK+	7		ns
PERR#		10 pF	PCI_CLK+	7		ns
SERR#		10 pF	PCI_CLK+	7		ns
PCI Inputs ^[2] . Refer to PCI Specification 2.1	t _{SI} t _{HI}					
PCI_REQ_L[3:2]		10 pF	PCI_CLK+	12		ns
PCI_REQ_L[1]		10 pF	PCI_CLK+	10		ns
PCI_REQ_L[0]		10 pF	PCI_CLK+	10		ns

1. The EXT_CLK1 pin may not be driven above 5.0 volts. If this pin is driven with a PCI bus driver, it must be clamped to 5.0 volts.
2. PCI_REQ_L[0] is used to signal a grant (SAT_GNT_L) if an external arbiter is enabled. PCI_REQ_L[1] is used to signal IDSEL when operating in Satellite mode.

TABLE 8: AC Characteristics (Bidirectional and Output Pins)

Pin Name	Symbol	Conditions	Reference Edge	100 MHz		Unit
				Min	Max	
MEMDATA[31:0] ^[1]	t _{DO}	132 pF	REF_CLOCK+	—	10	ns
	t _{HO}	132 pF	REF_CLOCK+	0	—	ns
	t _{SI}		REF_CLOCK+	6	—	ns
	t _{HI}		REF_CLOCK+	0	—	ns
MEMDATA[63:32] ^[2]	t _{DO}	120 pF	REF_CLOCK+	—	10	ns
	t _{HO}	120 pF	REF_CLOCK+	0	—	ns
	t _{SI}		REF_CLOCK+	6	—	ns
	t _{HI}		REF_CLOCK+	0	—	ns
MEMPAR[1:0] ^[1]	t _{DO}	156 pF	REF_CLOCK+	—	10	ns
	t _{HO}	156 pF	REF_CLOCK+	0	—	ns
	t _{SI}		REF_CLOCK+	6	—	ns
	t _{HI}		REF_CLOCK+	0	—	ns
ROM_ADDR[23:0]	t _{DO}	35 pF	REF_CLOCK+	-	20	ns
	t _{HO}	35 pF	REF_CLOCK+	-	-	ns
ROM_OE_L	t _{DO}	35 pF	REF_CLOCK+	-	20	ns
	t _{HO}	35 pF	REF_CLOCK+	-	-	ns
ROM_WE_L	t _{DO}	35 pF	REF_CLOCK+	-	20	ns
	t _{HO}	35 pF	REF_CLOCK+	-	-	ns
ROM_CS_L	t _{DO}	35 pF	REF_CLOCK+	-	20	ns
	t _{HO}	35 pF	REF_CLOCK+	-	-	ns
MEMADDR[11:0]	t _{DO}	28 pF	REF_CLOCK+	-	10	ns
	t _{HO}	28 pF	REF_CLOCK+	-	-	ns
RAS_L[7:0]+	t _{DO}	35 pF	REF_CLOCK+	-	10	ns
	t _{HO}	35 pF	REF_CLOCK+	0	-	ns
RAS_L[7:0]-	t _{DO}	35 pF	REF_CLOCK-	-	10	ns
	t _{HO}	35 pF	REF_CLOCK-	0	-	ns
CAS_L[3:0]	t _{DO}	55 pF	REF_CLOCK+	-	10	ns
	t _{HO}	55 pF	REF_CLOCK+	2	-	ns
MWE_L	t _{DO}	28 pF	REF_CLOCK+	-	10	ns
	t _{HO}	28 pF	REF_CLOCK+	0	-	ns
MOE_L	t _{DO}	28 pF	REF_CLOCK+	-	10	ns
	t _{HO}	28 pF	REF_CLOCK+	0	-	ns
INT_EVENT_L	t _{DO}	35 pF	REF_CLOCK+	-	10	ns
	t _{HO}	35 pF	REF_CLOCK+	0	-	ns

TABLE 8: AC Characteristics (Bidirectional and Output Pins) (Continued)

Pin Name	Symbol	Conditions	Reference Edge	100 MHz		Unit
				Min	Max	
JTAG_TDO	t _{DO}	80 pF	JTAG_CLK+	-	30	ns
	t _{HO}	80 pF	JTAG_CLK+	0	-	ns
REF_CLOCK	t _{DO}	35 pF	-	-	-	ns
	t _{HO}	35 pF	-	-	-	ns
<i>PCI BDI's: Refer to PCI Specification Rev 2.1</i>						
AD[31:0]		50 pF	PCI_CLK+	2	11	ns
FRAME#		50 pF	PCI_CLK+	2	11	ns
TRDY#		50 pF	PCI_CLK+	2	11	ns
IRDY#		50 pF	PCI_CLK+	2	11	ns
STOP#		50 pF	PCI_CLK+	2	11	ns
DEVSEL#		50 pF	PCI_CLK+	2	11	ns
CBE[3:0]#		50 pF	PCI_CLK+	2	11	ns
PAR		50 pF	PCI_CLK+	2	11	ns
PERR#		50 pF	PCI_CLK+	2	11	ns
SERR#		50 pF	PCI_CLK+	2	11	ns
<i>PCI Outputs: Refer to PCI Specification Rev 2.1</i>						
PCI_GNT[3:0]# [3]		50 pF	PCI_CLK+	2	12	ns
PCI_CLK[3:0]		50 pF	-	-	-	-
PCI_RST#		50 pF	PCI_CLK+	2	12	ns

1. DRAM interface pins tested with V_{DD3} 5.0V 5%.

2. DRAM interface pins tested with V_{DD3} 5.0V 5%.

3. PCI_GNT[0] is used to signal a host request to an external arbiter if enabled.

PIN ASSIGNMENTS ^[1]

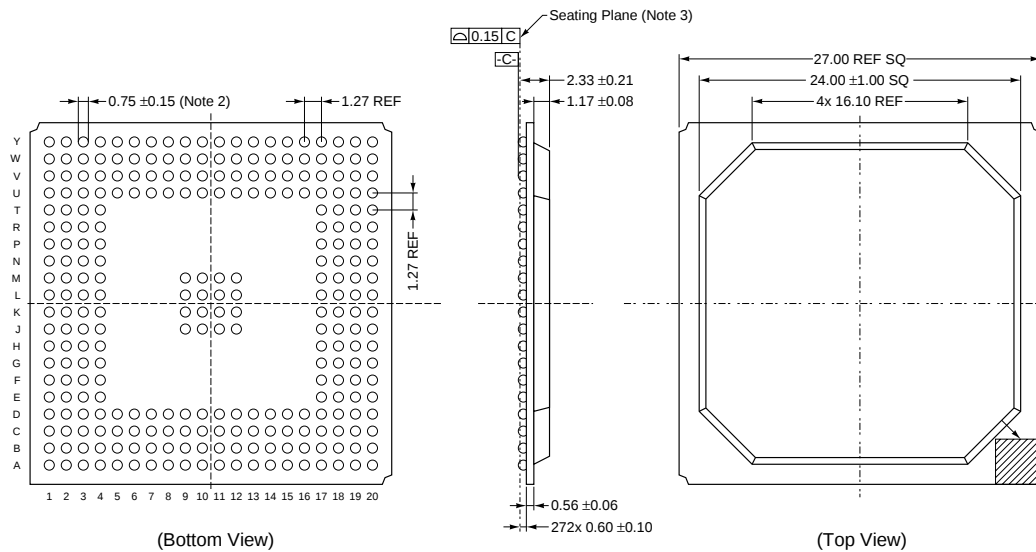
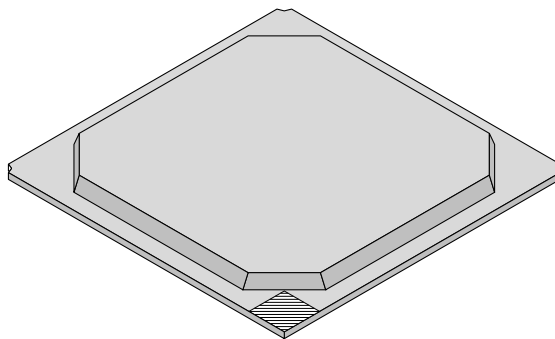
272 Pin Plastic Ball Grid Array (PBGA) Pin Assignment

SIGNAL NAME	BALL	SIGNAL NAME	BALL	SIGNAL NAME	BALL	SIGNAL NAME	BALL	SIGNAL NAME	BALL	SIGNAL NAME	BALL
AD[0]	B1	MEMDATA[17]	D16	BM_SEL[0]	V8	RAS_L[6]	J19	ROM_ADDR[22]	T17	VSS1	A1
AD[1]	D2	MEMDATA[18]	A18	BM_SEL[1]	W8	RAS_L[7]	J18	ROM_ADDR[23]	V20	VSS1	D4
AD[2]	D3	MEMDATA[19]	A17	CBE[0]#	V3	PAR	Y2	ROM_CS_L	T19	VSS1	D8
AD[3]	E4	MEMDATA[20]	C16	CBE[1]#	W2	PCI_CLK0	T4	ROM_OE_L	U20	VSS1	D13
AD[4]	C1	MEMDATA[21]	B16	CBE[2]#	Y1	PCI_CLK1	V2	ROM_WE_L	T18	VSS1	D17
AD[5]	D1	MEMDATA[22]	A16	CBE[3]#	W3	PCI_CLK2	W1	SERR#	U5	VSS1	H4
AD[6]	E2	MEMDATA[23]	C15	PCI_INT_L[4]	W12	PCI_CLK3	V6	SIMM32_SEL	H18	VSS1	H17
AD[7]	E1	MEMDATA[24]	B15	PCI_INT_L[5]	V12	PCI_GNT[0]#	R2	SP_SEL[0]	U11	VSS1	J9
AD[8]	F3	MEMDATA[25]	A15	DEVSEL#	P3	PCI_GNT[1]#	P4	SP_SEL[1]	V11	VSS1	J10
AD[9]	G4	MEMDATA[26]	C14	DIV_CTL[0]	Y14	PCI_GNT[2]#	R3	SP_SEL[2]	W11	VSS1	J11
AD[10]	F2	MEMDATA[27]	B14	DIV_CTL[1]	V13	PCI_GNT[3]#	T2	PCI_INT_L[6]	Y13	VSS1	J12
AD[11]	F1	MEMDATA[28]	A14	EXT_CLK1	W10	PCI_INT_L[0]	Y3	STOP#	R1	VSS1	K9
AD[12]	G3	MEMDATA[29]	C13	EXT_CLK2	Y9	PCI_INT_L[1]	Y4	THERM_D	G19	VSS1	K10
AD[13]	G2	MEMDATA[30]	B13	EXT_EVENT_L	V9	PCI_INT_L[2]	V5	TN	H20	VSS1	K11
AD[14]	H3	MEMDATA[31]	A13	FRAME#	N3	PCI_INT_L[3]	W5	TRDY#	P1	VSS1	K12
AD[15]	H2	MEMDATA[32]	C12	IIDD TN	H19	PCI_REQ[0]#	U1	PCI_INT_L[7]	V16	VSS1	L9
AD[16]	H1	MEMDATA[33]	B12	INPUT_RESET_L	W13	PCI_REQ[1]#	U2			VSS1	L10
AD[17]	J4	MEMDATA[34]	A12	INT_EVENT_L	Y12	PCI_REQ[2]#	T3			VSS1	L11
AD[18]	J3	MEMDATA[35]	B11	IRDY#	P2	PCI_REQ[3]#	V1	VDD2	C2	VSS1	L12
AD[19]	J2	MEMDATA[36]	C11	JTAG_CK	Y7	PCI_RST#	Y5	VDD2	E3	VSS1	M9
AD[20]	J1	MEMDATA[37]	A11	JTAG_MS	W7	PERR#	W4	VDD2	G1	VSS1	M10
AD[21]	K2	MEMDATA[38]	A10	JTAG_TDI	V7	PLL_BYP_L	W9	VDD2	K3	VSS1	M11
AD[22]	K1	MEMDATA[39]	B10	JTAG_TDO	W6	PLL_RST	V10	VDD2	M4	VSS1	M12
AD[23]	L1	MEMDATA[40]	D10	JTAG_TRST_L	Y6	PLL_VDD (VDD4)	Y10	VDD2	T1	VSS1	N4
AD[24]	L2	MEMDATA[41]	A9	SCAN_MODE	Y8	PLL_VSS (VSS4)	Y11	VDD2	U3	VSS1	N17
AD[25]	L3	MEMDATA[42]	B9	CAS_L[0]	M19	PROC MON	U9	VDD2	V4	VSS1	U4
AD[26]	L4	MEMDATA[43]	C9	CAS_L[1]	M20	REF_CLOCK	U12	VDD2	U7	VSS1	U8
AD[27]	M1	MEMDATA[44]	D9	CAS_L[2]	L19	ROM_ADDR[0]	W14			VSS1	U13
AD[28]	M2	MEMDATA[45]	A8	CAS_L[3]	L18	ROM_ADDR[1]	Y15			VSS1	U17
AD[29]	M3	MEMDATA[46]	B8	MEMADDR[0]	T20	ROM_ADDR[2]	V14				
AD[30]	N1	MEMDATA[47]	C8	MEMADDR[1]	R18	ROM_ADDR[3]	W15	VDD3	A4	VDD1	D6
AD[31]	N2	MEMDATA[48]	B7	MEMADDR[2]	P17	ROM_ADDR[4]	Y16	VDD3	A7	VDD1	D11
MEMDATA[0]	E20	MEMDATA[49]	A6	MEMADDR[3]	R19	ROM_ADDR[5]	U14	VDD3	B17	VDD1	D15
MEMDATA[1]	G17	MEMDATA[50]	C7	MEMADDR[4]	R20	ROM_ADDR[6]	V15	VDD3	C3	VDD1	F4
MEMDATA[2]	F18	MEMDATA[51]	B6	MEMADDR[5]	P18	ROM_ADDR[7]	W16	VDD3	C10	VDD1	F17
MEMDATA[3]	E19	MEMDATA[52]	A5	MEMADDR[6]	P19	ROM_ADDR[8]	Y17	VDD3	D12	VDD1	K4
MEMDATA[4]	D20	MEMDATA[53]	D7	MEMADDR[7]	P20	ROM_ADDR[9]	W17	VDD3	D14	VDD1	L17
MEMDATA[5]	E18	MEMDATA[54]	C6	MEMADDR[8]	N18	ROM_ADDR[10]	Y18	VDD3	E17	VDD1	R4
MEMDATA[6]	D19	MEMDATA[55]	B5	MEMADDR[9]	N19	ROM_ADDR[11]	U16	VDD3	F19	VDD1	R17
MEMDATA[7]	C20	MEMDATA[56]	C5	MEMADDR[10]	N20	ROM_ADDR[12]	V17			VDD1	U6
MEMDATA[8]	D18	MEMDATA[57]	B4	MEMADDR[11]	M17	ROM_ADDR[13]	W18			VDD1	U10
MEMDATA[9]	C19	MEMDATA[58]	A3	MOE_L	J17	ROM_ADDR[14]	Y19			VDD1	U15
MEMDATA[10]	B20	MEMDATA[59]	D5	MWE_L	M18	ROM_ADDR[15]	V18			VDD1	G20
MEMDATA[11]	C18	MEMDATA[60]	C4	RAS_L[0]	L20	ROM_ADDR[16]	W19				
MEMDATA[12]	B19	MEMDATA[61]	B3	RAS_L[1]	K20	ROM_ADDR[17]	Y20				
MEMDATA[13]	A20	MEMDATA[62]	B2	RAS_L[2]	K19	ROM_ADDR[18]	W20				
MEMDATA[14]	A19	MEMDATA[63]	A2	RAS_L[3]	K18	ROM_ADDR[19]	V19				
MEMDATA[15]	B18	MEMPAR[0]	F20	RAS_L[4]	K17	ROM_ADDR[20]	U19				
MEMDATA[16]	C17	MEMPAR[1]	G18	RAS_L[5]	J20	ROM_ADDR[21]	U18				

1. The STP1100BGA is JEDEC level III moisture sensitive and will be shipped dry packed. JEDEC standards should apply to handling.

PACKAGE DIMENSIONS

272-Pin BGA Package



- Notes: 1. Dimensions in mm.
2. Measured at maximum solder ball diameter parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

ORDERING INFORMATION

Part Number	Speeds	Description
STP1100BGA-100	100 MHz	SPARC v8 32-bit microprocessor with PCI/DRAM interfaces.

Document Part Number: 802-7327-05

Preliminary
STP1100BGA



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