

4V Drive Nch + Pch MOSFET

SH8M41

● Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8M41		○

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	80	-80	V
Gate-source voltage	V_{GSS}	20	-20	V
Drain current	Continuous	I_D	± 3.4	A
	Pulsed	I_{DP}^{*1}	± 13.6	A
Source current (Body Diode)	Continuous	I_S	-1.6	A
	Pulsed	I_{SP}^{*1}	-10.4	A
Power dissipation	P_D^{*2}	2		W / TOTAL
Channel temperature	Tch	150		°C
Range of storage temperature	Tstg	-55 to +150		°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

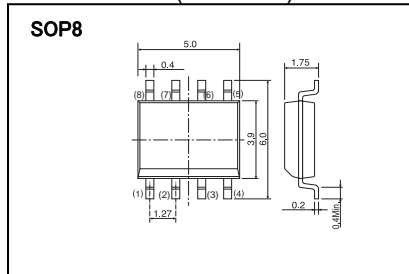
*2 Mounted on a ceramic board.

● Thermal resistance

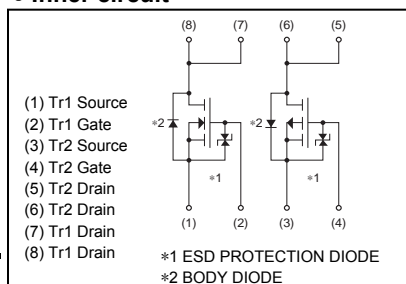
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	62.5	°C / W

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	10	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=80V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	90	130	m Ω	$I_D=3.4A, V_{GS}=10V$
		-	110	150		$I_D=3.4A, V_{GS}=4.5V$
		-	120	160		$I_D=3.4A, V_{GS}=4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	3	-	-	S	$V_{DS}=10V, I_D=3.4A$
Input capacitance	C_{iss}	-	600	-	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	-	100	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	40	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	12	-	ns	$I_D=1.7A, V_{D\bar{B}}=40V$
Rise time	t_r^*	-	15	-	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}^*$	-	40	-	ns	$R_L=24\Omega$
Fall time	t_f^*	-	12	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	6.6	9.2	nC	$I_D=3.4A$
Gate-source charge	Q_{gs}^*	-	1.8	-	nC	$V_{D\bar{B}}=40V$
Gate-drain charge	Q_{gd}^*	-	2.2	-	nC	$V_{GS}=5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_S=6.4A, V_{GS}=0V$

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	-10	μA	$V_{GS} = -20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-80	-	-	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}		-	-1	μA	$V_{DS} = -80V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	165	240	m Ω	$I_D = -2.6A, V_{GS} = -10V$
		-	220	300		$I_D = -1.3A, V_{GS} = -4.5V$
		-	230	310		$I_D = -1.3A, V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	2	-	-	S	$I_D = -2.6A, V_{DS} = -10V$
Input capacitance	C_{iss}	-	1000	-	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	-	90	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	40	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	14	-	ns	$I_D = -1.3A, V_{DS} = -40V$
Rise time	t_r^*	-	12	-	ns	$V_{GS} = -10V$
Turn-off delay time	$t_{d(off)}^*$	-	60	-	ns	$R_L = 31\Omega$
Fall time	t_f^*	-	20	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	-	8.2	11.5	nC	$I_D = -2.6A$
Gate-source charge	Q_{gs}^*	-	2.5	-	nC	$V_{DD} = -40V$
Gate-drain charge	Q_{gd}^*	-	2.5	-	nC	$V_{GS} = -5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_S = -1.6A, V_{GS} = 0V$

*Pulsed

● Electrical characteristic curves <Tr1(Nch)>

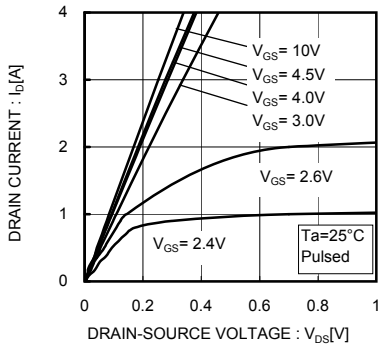


Fig.1 Typical Output Characteristics (I)

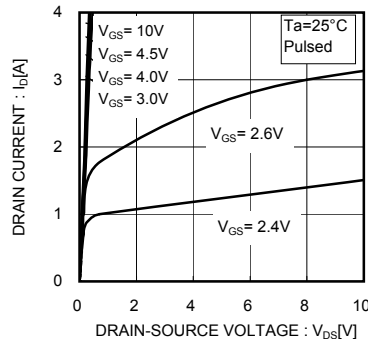


Fig.2 Typical Output Characteristics (II)

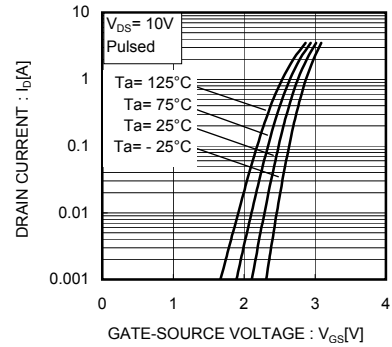


Fig.3 Typical Transfer Characteristics

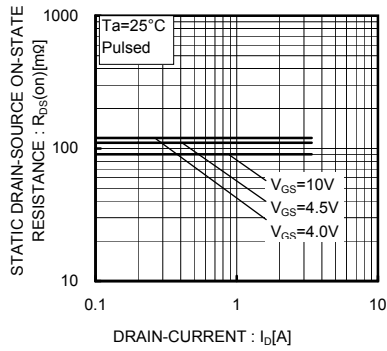


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

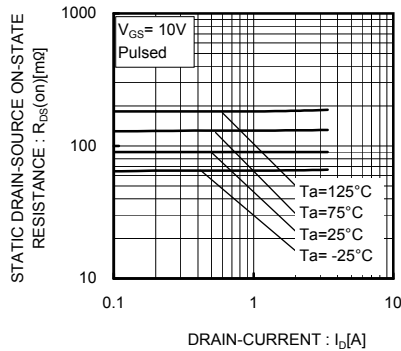


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

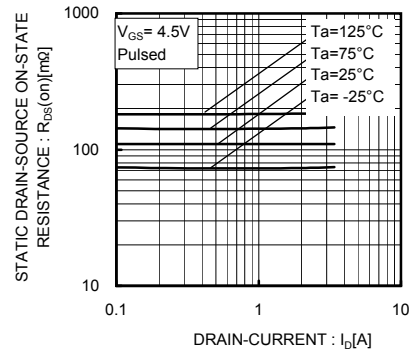


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(I)

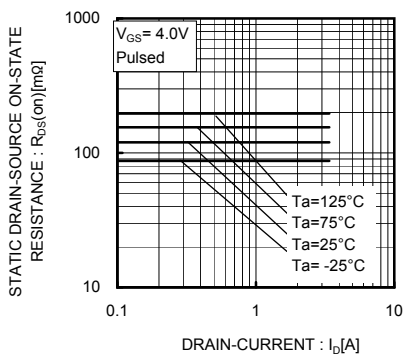


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(III)

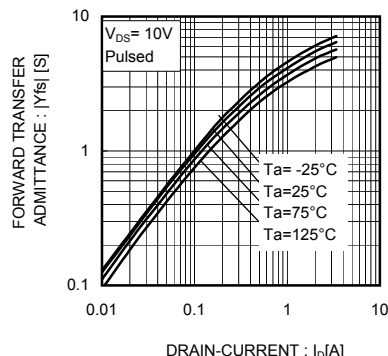


Fig.8 Forward Transfer Admittance vs. Drain Current

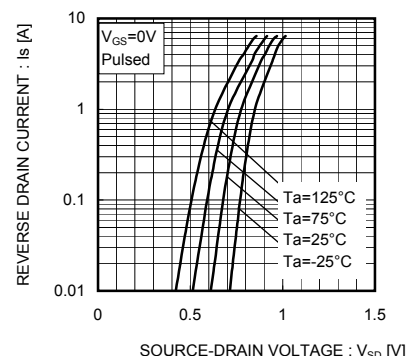


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

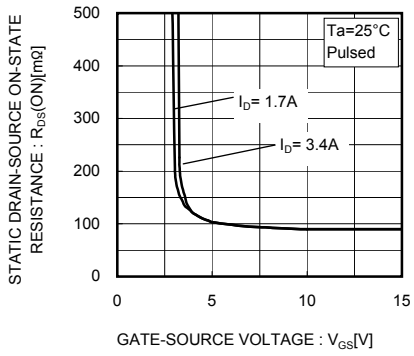


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

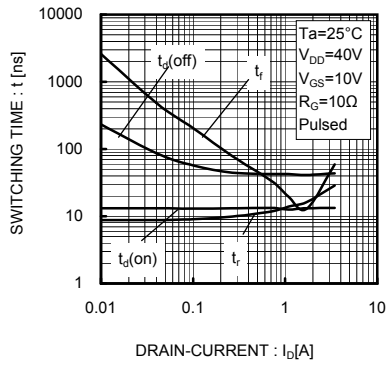


Fig.11 Switching Characteristics

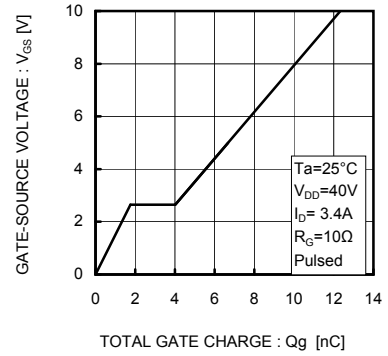


Fig.12 Dynamic Input Characteristics

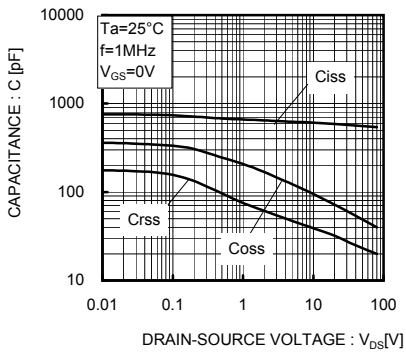


Fig.13 Typical Capacitance vs. Drain-Source Voltage

● Electrical characteristic curves <Tr2(Pch)>

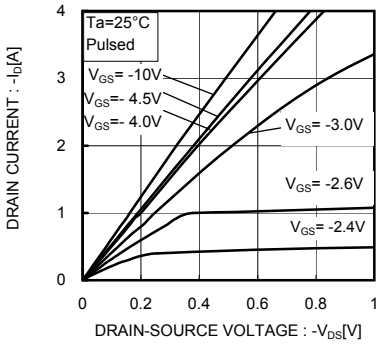


Fig.1 Typical Output Characteristics(I)

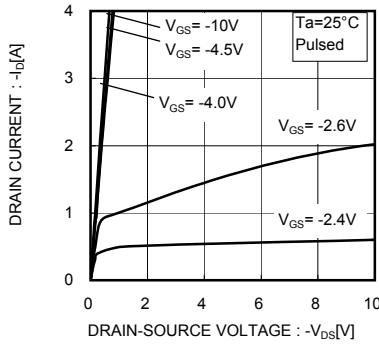


Fig.2 Typical Output Characteristics(II)

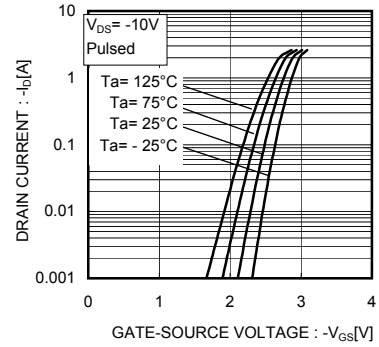


Fig.3 Typical Transfer Characteristics

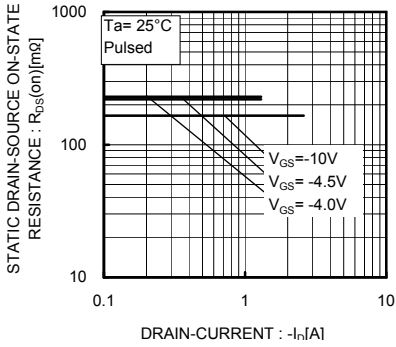


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

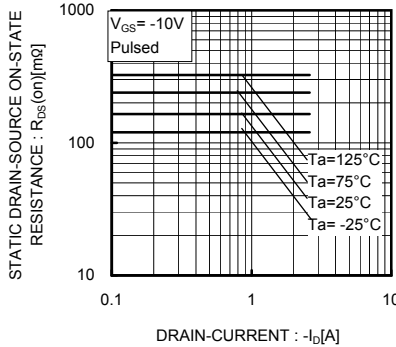


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(I)

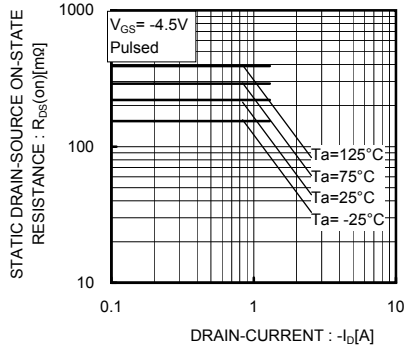


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(II)

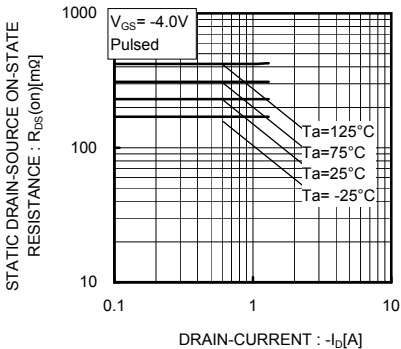


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(III)

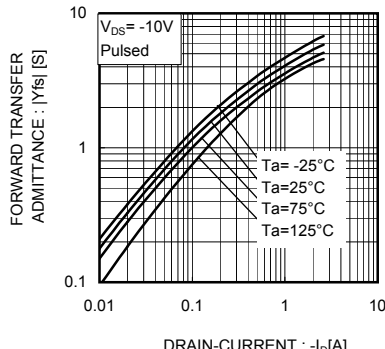


Fig.8 Forward Transfer Admittance vs. Drain Current

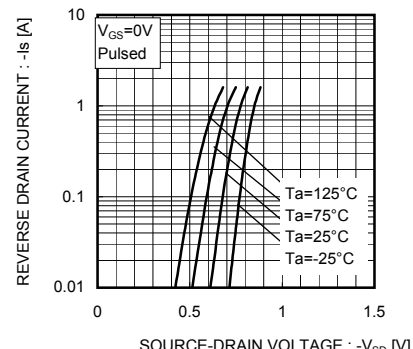


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

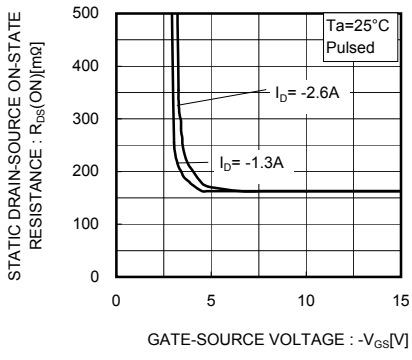


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

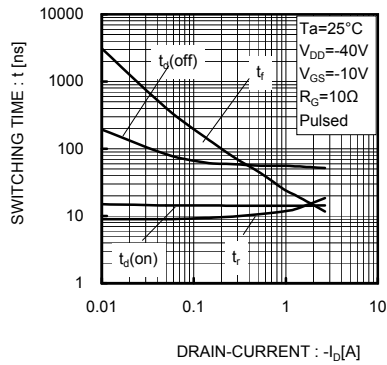


Fig.11 Switching Characteristics

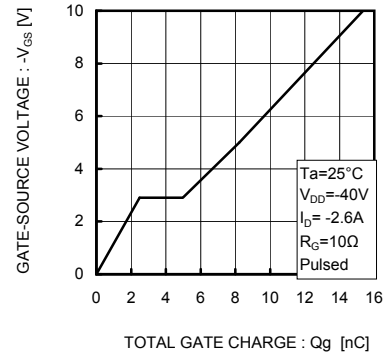


Fig.12 Dynamic Input Characteristics

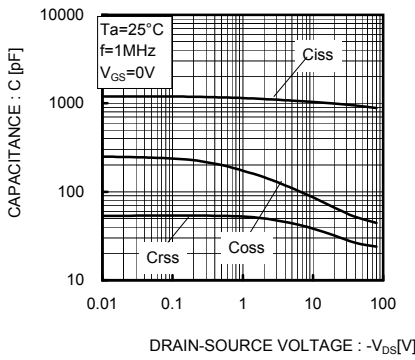


Fig.13 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

<Tr1(Nch)>

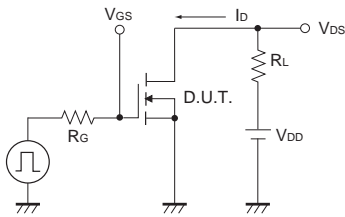


Fig.1-1 Switching time measurement circuit

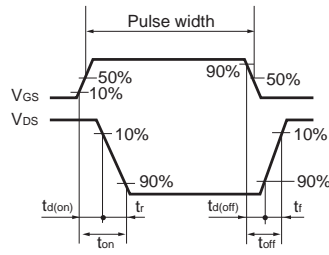


Fig.1-2 Switching waveforms

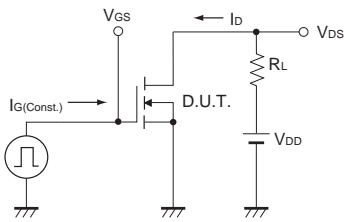


Fig.2-1 Gate charge measurement circuit

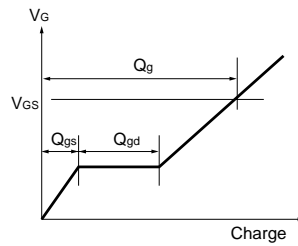


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

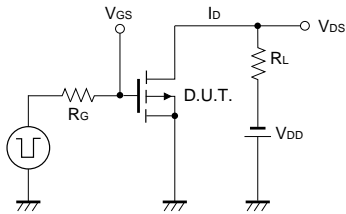


Fig. 3-1 Switching Time Measurement Circuit

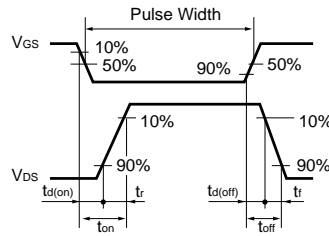


Fig. 3-2 Switching Waveforms

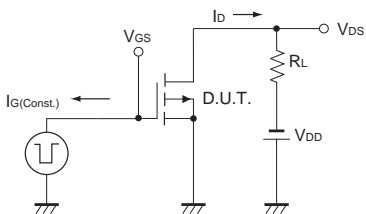


Fig. 4-1 Gate charge measurement circuit

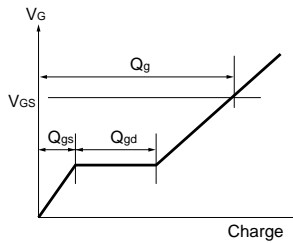


Fig. 4-2 Gate Charge Waveform

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