High-Integration SAB 80188/80188-1 8-Bit Microprocessor

SAB 80188 8 MHz

- Integrated feature set
  - enhanced SAB 8088-2 CPU
  - clock generator
  - 2 independent high-speed DMA channels
  - programmable interrupt controller
  - 3 programmable 16-bit timers
  - programmable memory and peripheral chip-select logic
  - programmable wait state generator
  - local bus controller
- High-performance processor
  - twice the performance of the standard SAB 8088 at 8 MHz
  - 2 Mbyte/s bus bandwidth interface at 8 MHz

SAB 80188-1 10 MHz

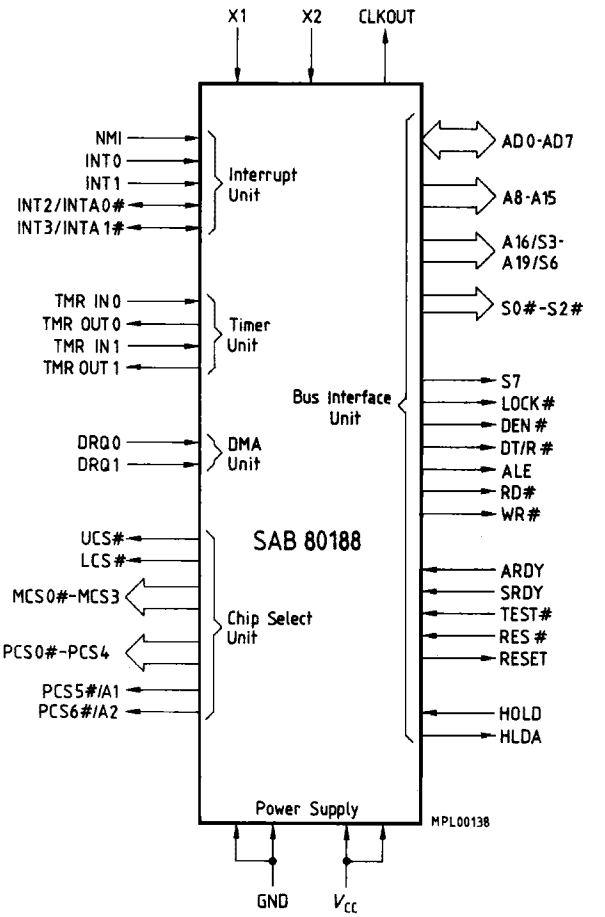
- Direct addressing capability to 1 Mbyte of memory
- Completely object-code compatible with all existing SAB 8086/8088 software
  - 10 new instruction types
- Optional numerical processor extension
- Compatible with the bus support components SAB 8282A/8283A/8286A/8287A and SAB 8288A/8289
- Compatible with industry standard 80188 processor
- Available in 10 MHz (SAB 80188-1) and 8 MHz (SAB 80188) versions

The SAB 80188 is a highly integrated 8-bit microprocessor implemented in +5V advanced Siemens MYMOS technology. It effectively combines 15 to 20 of the most common SAB 8088 system components onto one chip. The 8 MHz SAB 80188 provides twice the throughput of the standard 5 MHz SAB 8088. The SAB 80188 is upward-compatible with SAB 8086 and SAB 8088 software, and adds 10 new instruction types to the existing set. The SAB 80188 comes in a 68-pin packages and requires single +5V power supply.

Pin Names

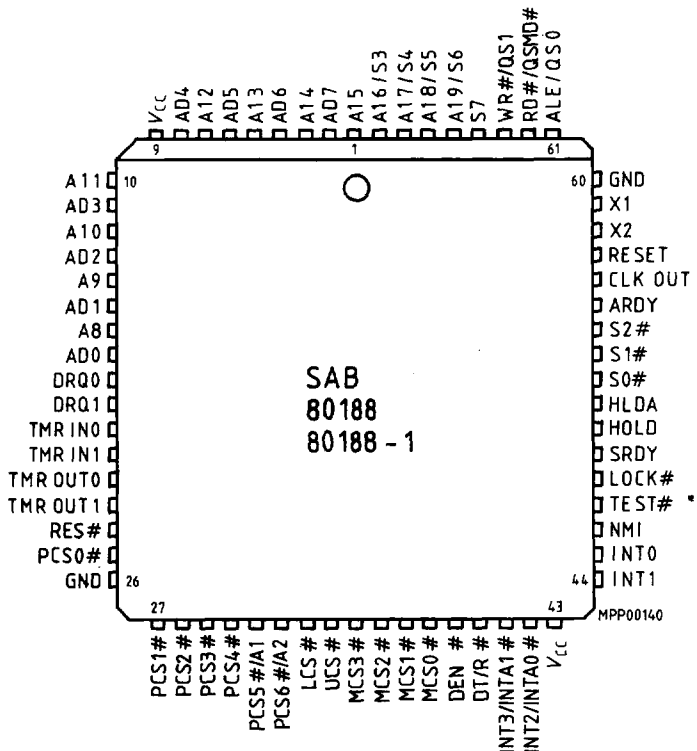
AD0–AD7	Address/Data Bus
A8–A15	Address Bus
A16/S3–A19/S6	Address Bus/Status Lines
S0–S2	Status Lines
S7	Status Line
$\overline{\text{LOCK}}$	Bus Lock
$\overline{\text{DEN}}$	Data Enable
DT/$\overline{\text{R}}$	Data Transmit/Receive
ALE/QS0	Address Latch Enable/Queue Status
$\overline{\text{RD}}$/QSMD	Read Strobe/Queue Status Mode
$\overline{\text{WR}}$/QS1	Write Strobe/Queue Status
ARDY	Asynchronous Ready
SRDY	Synchronous Ready
$\overline{\text{TEST}}$	Test Line
$\overline{\text{RES}}$	Reset Input
RESET	Reset Output
HOLD	Hold Request
HLDA	Hold Acknowledge
NMI	Non-Maskable Interrupt
INT0, INT1	Interrupt Request
INT2/INTA0	Interrupt Request/Acknowledge
INT3/INTA1	Interrupt Request/Acknowledge
TMR IN0/TMR OUT0	Timer 0 Input/Output
TMR IN1/TMR OUT1	Timer 1 Input/Output
DRQ0, DRQ1	Data Request
$\overline{\text{UCS}}$, $\overline{\text{LCS}}$	Upper/Lower Chip Select
$\overline{\text{MCS0}}$–$\overline{\text{MCS3}}$	Memory Chip Select
$\overline{\text{PCS0}}$–$\overline{\text{PCS4}}$	Peripheral Chip Select
$\overline{\text{PCS5}}$/A1, $\overline{\text{PCS6}}$/A2	Peripheral Chip Select/Address
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

Logic Symbol



Pin Configuration

Leaded Chip Carrier Package (top view)



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Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD7–AD0	2, 4, 6, 8, 11,13,15,17	I/O	**ADDRESS/DATA BUS (0 TO 7)** These signals constitute the time-multiplexed memory or I/O address (T1) and data (T2, T3, TW, and T4) bus. The bus is active high.
A15–A8	1, 3, 5, 7 10,12,14,16	O	**ADDRESS BUS (8 TO 15)** Contains valid address from T1 to T4. The bus is active high.
DRQ0 DRQ1	18 19	I I	**DMA REQUEST** Is driven high by an external device when it desires that a DMA channel (channel 0 or 1) performs a transfer. These signals are active high, level-triggered, and internally synchronized.
TMR IN 0, TMR IN 1	20 21	I I	**TIMER INPUTS** Are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active high (or low-to-high transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	**TIMER OUTPUTS** Are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
$\overline{RES}$	24	I	**$\overline{SYSTEM\ RESET}$** Causes the SAB 80188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the SAB 80188 clock. The SAB 80188 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned high. $\overline{RES}$ is required to be low for greater than 4 clock cycles and is internally synchronized. For proper initialization, the low-to-high transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the SAB 80188 will drive the status lines to an inactive level for one clock, and then tristate them.
$\overline{PCS0}$ $\overline{PCS1-4}$	25 27,28,29,30	O O	**$\overline{PERIPHERAL\ CHIP\ SELECT\ 0\ TO\ 4}$** These signals are active low when a reference is made to the defined peripheral area (64 Kbyte I/O space). These lines are not tristated during bus hold. The address ranges activating $\overline{PCS0-4}$ are software-programmable.
$\overline{PCS5}$/A1	31	O	**$\overline{PERIPHERAL\ CHIP\ SELECT\ 5}$ LATCHED A1** May be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active high.
$\overline{PCS6}$/A2	32	O	**$\overline{PERIPHERAL\ CHIP\ SELECT\ 6}$ LATCHED A2** May be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active high.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{LCS}$	33	O	**$\overline{LOWER\ MEMORY\ CHIP\ SELECT}$** Is active low whenever a memory reference is made to the defined lower portion (1 K to 256 K) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{LCS}$ is software-programmable.
$\overline{UCS}$	34	O	**$\overline{UPPER\ MEMORY\ CHIP\ SELECT}$** Is an active low output whenever a memory reference is made to the defined upper portion (1 K to 256 K block) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{UCS}$ is software-programmable.
$\overline{MCS0-3}$	38, 37, 36, 35	O	**MIDRANGE MEMORY CHIP SELECT 0 TO 3** These signals are active low when a memory reference is made to the defined midrange portion of memory (8 K to 512 K). These lines are not tristated during bus HOLD. The address ranges activating $\overline{MCS0-3}$ are software-programmable.
$\overline{DEN}$	39	O	**DATA ENABLE** Is provided as an SAB 8286A/8287A data bus transceiver output enable. $\overline{DEN}$ is active low during each memory and I/O access. $\overline{DEN}$ is high whenever DT/$\overline{R}$ changes its state.
DT/$\overline{R}$	40	O	**DATA TRANSMIT/$\overline{RECEIVE}$** Controls the direction of data flow through the external SAB 8286A/8287A data bus transceiver. When low data is transferred to the SAB 80188. When high the SAB 80188 places write data on the data bus.
INT0, INT1, INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45, 44 42 41	I I/O I/O	**MASKABLE INTERRUPT REQUEST** Can be requested by strobing one of these pins. When configured as inputs, these pins are active high. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active low interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
NMI	46	I	**NON-MASKABLE INTERRUPT** Is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from low to high initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
$\overline{TEST}$	47	I	**$\overline{TEST}$** Is examined by the WAIT instruction. If the $\overline{TEST}$ input is high when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes low, at which time execution will be resumed. If interrupts are enabled while the SAB 80188 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{LOCK}$	48	O	**$\overline{LOCK}$** This output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active low. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the $\overline{LOCK}$ prefix. It remains active until the completion of the instruction following the $\overline{LOCK}$ prefix. No pre-fetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active low, is driven high for one clock during reset, and then tristated.
SRDY	49	I	**SYNCHRONOUS READY** Must be synchronized externally to the SAB 80188. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active high. If this line is connected to V_{CC} no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied low.
HOLD HLDA	50 51	I O	**HOLD/HOLD ACKNOWLEDGE** Indicates that another bus master is requesting the local bus. The HOLD input is active high. HOLD may be asynchronous with respect to the SAB 80188 clock. The SAB 80188 will issue a HLDA (high) in response to a HOLD request at the end of T4 or T1. Simultaneous with issuing HLDA, the SAB 80188 will tristate the local bus and control lines. After HOLD is detected as being low, the SAB 80188 will lower HLDA. When the SAB 80188 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	52–54	O	**$\overline{BUS\ CYCLE\ STATUS}$** $\overline{S0}$ to $\overline{S2}$ are encoded to provide bus transaction information: SAB 80188 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins are tristated during "HOLD."
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
The status lines are driven high for one clock during reset, and then tristated until a bus cycle begins.

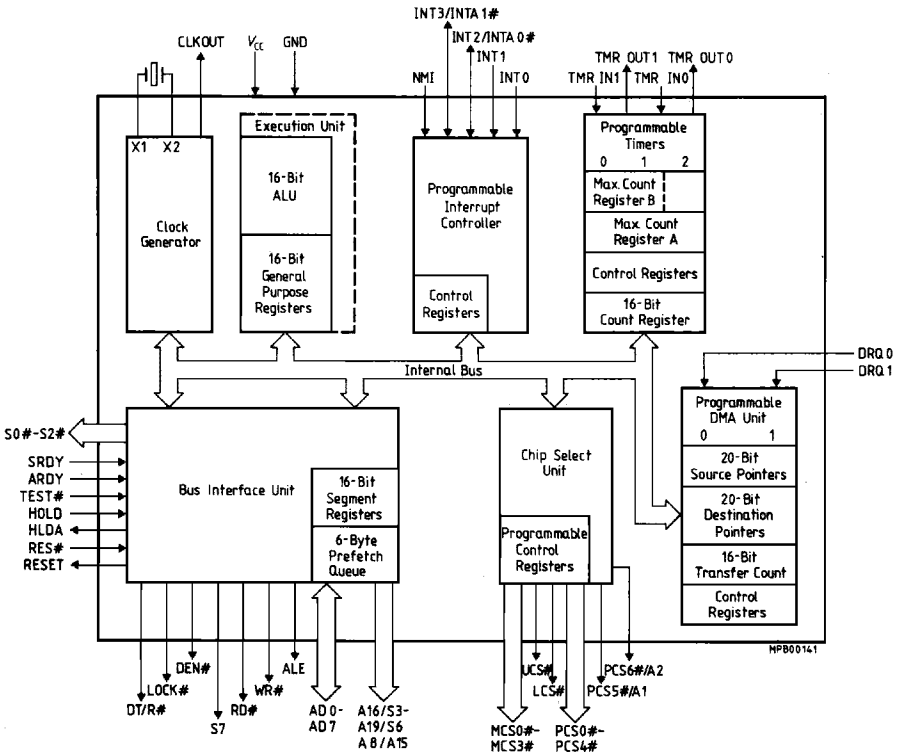
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ARDY	55	I	**ASYNCHRONOUS READY** Informs the SAB 80188 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input and is active high. Only the rising edge is internally synchronized by the SAB 80188. This means that the falling edge of ARDY must be synchronized to the SAB 80188 clock. If connected to V_{CC} no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied low.
CLKOUT	56	O	**CLOCK OUTPUT** Provides the system with a 50% duty cycle waveform. All device pin timings are specified relative in CLKOUT.
RESET	57	O	**RESET** This output indicates that the SAB 80188 CPU is being reset, and can be used as a system reset. It is active high, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59, 58	I	**CRYSTAL INPUTS** X1 and X2 provide an external connection for a fundamental-mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
ALE/QS0	61	O	**ADDRESS LATCH ENABLE/QUEUE STATUS 0** Is provided by the SAB 80188 to latch the address into the SAB 8282A/8283A address latches. ALE is active high. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively half a clock cycle earlier than in the standard SAB 8088. The trailling edge is generated off the CLKOUT rising edge in T1 like in the SAB 8088. Note that ALE is never tristated.
$\overline{RD}$/QSMD	62	O	**READY STROBE** Indicates that the SAB 80188 is performing a memory or I/O read cycle. $\overline{RD}$ is active low for T2, T3 and TW of any read cycle. It is guaranteed not to go low in T2 until after the address bus is tristated. $\overline{RD}$ is active low and tristated during "HOLD". $\overline{RD}$ is driven high for one clock during reset, and then the output driver is tristated. A weak internal pullup mechanism on the $\overline{RD}$ line holds it high when the line is not driven. During reset, the pin is sampled to determine whether the SAB 80188 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the queue status should be provided. $\overline{RD}$ should be connected to GND to provide queue status data.

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{WR}$/QS1</td><td>63</td><td>O</td><td>$\overline{WRITE\ STROBE}$/QUEUE STATUS 1
Indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T2, T3, and TW of any write cycle. It is active low and tristated during "HOLD." It is driven high for one clock during reset, and then tristated. When the SAB 80188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
<table>
<tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr>
<tr><td>0</td><td>0</td><td>No Queue Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Op Code Byte Fetched from the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte Fetched from the Queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the Queue</td></tr>
</table></td></tr>
<tr><td>S7</td><td>64</td><td>O</td><td>STATUS LINE 7
This signal is always high to indicate that the SAB 80188 has an 8-bit data bus, and is tristated off during bus hold.</td></tr>
<tr><td>A19/S6,
A18/S5,
A17/S4,
A16/S3</td><td>65
66
67
68</td><td>O
O
O
O</td><td>ADDRESS BUS OUTPUTS (16 TO 19) and
BUS CYCLE STATUS (3 TO 6)
They reflect the four most significant address bits during T1. These signals are active high. During T2, T3, TW, and T4, status information is available on these lines as encoded below:
<table>
<tr><th></th><th>Low</th><th>High</th></tr>
<tr><td>S6</td><td>Processor Cycle</td><td>DMA Cycle</td></tr>
</table>
S3, S4, and S5 are defined as being low during T2 to T4.</td></tr>
<tr><td>V_{CC}</td><td>9, 43</td><td>I</td><td>POWER SUPPLY (+5V)</td></tr>
<tr><td>GND</td><td>26, 60</td><td>I</td><td>GROUND (0V)</td></tr>
</table>

Block Diagram



Functional Description

The SAB 8086, 8088, 80186, 80188 and 80286 families all contain the same basic set of registers, instructions, and addressing modes. The SAB 80188 processor is upward-compatible with the SAB 8086 and SAB 8088 CPUs.

Register Set

The SAB 80188 base architecture has fourteen registers. These registers are grouped into the following categories.

General registers

Eight 16-bit general-purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment registers

Four 16-bit special-purpose registers select, at any time given, the segments of memory that are immediately addressable for code, stack, and data.

Base and index registers

Four of the general-purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and control registers

Two 16-bit special-purpose registers record or alter certain aspects of the SAB 80188 processor state. These are the instruction pointer register, which contains the offset address of the next sequential instruction to be executed, and the status word register, which contains status and control flag bits.

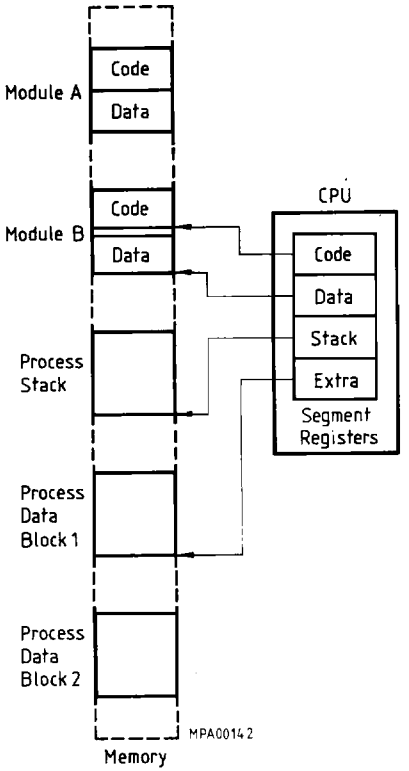
Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64 K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value left by four bits and adding the 16-bit offset value to yield a 20-bit physical address. This allows for a 1 Mbyte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used. These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

Memory Segmentation



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I/O Space

The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero-extended such that A15 to A8 are low I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (status word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware-initiated, INT instructions, and instruction exceptions. Hardware-initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Interrupt Sources

The SAB 80188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type, multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Interrupt Vector Table

Interrupt Name	Vector Type	Default Priority [5]	Related Instructions
Divide Error Exception	0	1 [1]	DIV, IDIV
Single-Step Interrupt	1	12 [2] 2	All
NMI	2	1	All
Breakpoint Interrupt	3	1 [1]	INT
INT0 Detected Overflow Exception	4	1 [1]	INT0
Array Bounds Exception	5	1 [1]	BOUND
Unused Op Code Exception	6	1 [1]	Undefined Op Codes
ESC Op Code Exception	7	1 [1] [3]	ESC Op Codes
Timer 0 Interrupt	8	2A [4]	
Timer 1 Interrupt	18	2B [4]	
Timer 2 Interrupt	19	2C [4]	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INT0 Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

1) These are generated as the result of an instruction execution.
2) This is handled as in the SAB 8088.
3) An escape op code will cause a trap only if the proper bit is set in the peripheral control block relocation register.
4) All three timers constitute one source of request to the interrupt controller. The timer interrupts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each timer interrupt has a separate vector type number.
5) Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin low. $\overline{RES}$ forces the SAB 80188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the SAB 80188 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values.

Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

Clock Generator

The SAB 80188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs and reset circuitry.

Oscillator

The oscillator circuit of the SAB 80188 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the SAB 80188. The crystal frequency selected will be twice the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the SAB 80188.

Ready Synchronization

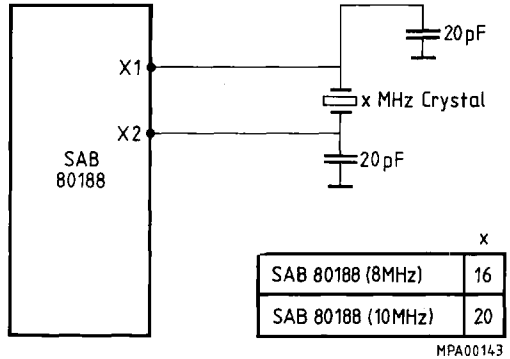
The SAB 80188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T2, T3 and again in the middle of each TW until ARDY is sampled high.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T2, T3 and again at the end of each TW until it is sampled high.

Reset Logic

The SAB 80188 provides both a $\overline{RES}$ input pin and a synchronized reset pin for use with other system components. The $\overline{RES}$ input pin on the SAB 80188 is provided with hysteresis in order to facilitate power-on reset generation via an RC network.

Recommended SAB 80188 Crystal Configuration



	x
SAB 80188 (8MHz)	16
SAB 80188 (10MHz)	20

MPA00143

The following parameters may be used for choosing a crystal:

Temperature range . . . . . 0 to 70 °C
ESR (equivalent series resistance) . . . . . 30 Ω max.
C0 (shunt capacitance of crystal) . . . . . 7.0 pF max.
C1 (load capacitance) . . . . . 20 pF ± 2 pF
Drive level . . . . . 1 mW max.

Local Bus Controller

The SAB 80188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

When the SAB 80188 relinquishes control of the local bus, it tristates $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$ to $\overline{S2}$, $\overline{LOCK}$, AD0 to AD7, A8 to A19, S7 and DT/$\overline{R}$ to allow another master to drive these lines directly.

Local bus controller and reset

Upon receipt of a reset pulse from the $\overline{RES}$ input, the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ high for one clock cycle, then float.
  Note: $\overline{RD}$ is also provided with an internal pullup device to prevent the processor from inadvertently entering queue status mode during reset.
- Drive $\overline{S0}$ to $\overline{S2}$ to the passive state (all high) and then float.
- Drive $\overline{LOCK}$ high and then float.
- Tristate AD0 to AD7, A8 to A19, S7, DT/$\overline{R}$.
- Drive ALE low (ALE is never tristated).
- Drive HLDA low.

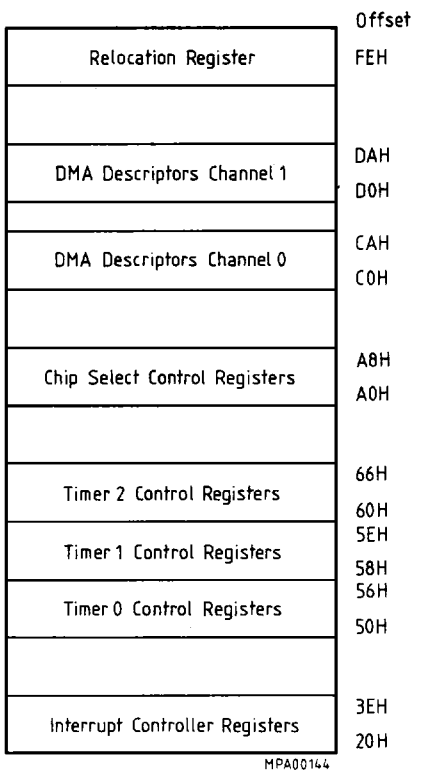
Internal Peripheral Interface

All the SAB 80188 integrated peripherals are controlled via 16-bit registers contained within an internal 256 byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D7 to D0, SRDY, and ARDY will be ignored.

The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block. It provides the upper 12 bits of the base address of the control block.

The integrated SAB 80188 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks.

Internal Register Map



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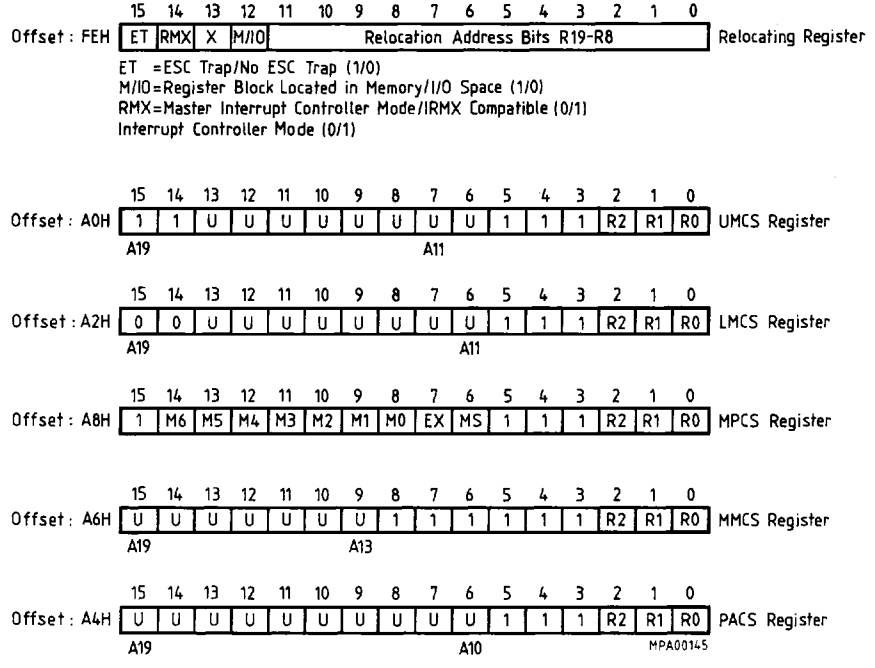
Chip Select Registers



UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1 K	FFF8H
FF800	2 K	FFB8H
FF000	4 K	FF38H
FE000	8 K	FE38H
FC000	16 K	FC38H
F8000	32 K	F838H
F0000	64 K	F038H
E0000	128 K	E038H
C0000	256 K	C038H

LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1 K	0038H
007FFH	2 K	0078H
00FFFH	4 K	00F8H
01FFFH	8 K	01F8H
03FFFH	16 K	03F8H
07FFFH	32 K	07F8H
0FFFFH	64 K	0FF8H
1FFFFH	128 K	1FF8H
3FFFFH	256 K	3FF8H

MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14 to 8
8 K	2 K	0000001B
16 K	4 K	0000010B
32 K	8 K	0000100B
64 K	16 K	0001000B
128 K	32 K	0010000B
256 K	64 K	0100000B
512 K	128 K	1000000B

MS, EX Programming Values

Bit	Description
MS	1=Peripherals Mapped into Memory Space. 0=Peripherals Mapped into I/O Space.
EX	0=5 $\overline{PCS}$ Lines. A1, A2 Provided. 1=7 $\overline{PCS}$ Lines. A1, A2 Are Not Provided.

Ready Bits Programming

R2	R1	R0	Number of Wait States Generated
0	0	0	0 Wait States, External RDY Also Used
0	0	1	1 Wait State Inserted, External RDY Also Used
0	1	0	2 Wait States Inserted, External RDY Also Used
0	1	1	3 Wait States Inserted, External RDY Also Used
1	0	0	0 Wait States, External RDY Ignored
1	0	1	1 Wait State Inserted, External RDY Ignored
1	1	0	2 Wait States Inserted, External RDY Ignored
1	1	1	3 Wait States Inserted, External RDY Ignored

Chip Select Logic

The SAB 80188 contains logic which provides programmable chip select generation for both, memories and peripherals. In addition, it can be programmed to provide ready (or wait state) generation. It can also provide latched address bits A1 and A2. The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The SAB 80188 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

Upper Memory $\overline{CS}$

The SAB 80188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the SAB 80188 begins executing at memory location FFFF0H. After reset, the UMCS register is programmed for a 1 K area. It must be reprogrammed if a larger upper memory area is desired.

Lower Memory $\overline{CS}$

The SAB 80188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip select line will not become active until the LMCS register is accessed.

Midrange Memory $\overline{CS}$

The SAB 80188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

Each of the four chip select lines is active for one of the four equal contiguous divisions of the midrange block. Thus, if the total block size is 32 K, each chip select is active for 8 K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range. After reset, the contents of both of these registers is undefined.

However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

Peripheral Chip Selects

The SAB 80188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0-6}$ are generated by the SAB 80188. The base address is user-programmable; however it can only be a multiple of 1 Kbytes, i.e. the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects.

The starting address of the peripheral chip select block is defined by the PACS register. This register is located at offset A4H in the internal control block. Bits 15 to 6 of this register correspond to bits 19 to 10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block.

PCS Address Ranges

PCS Line	Active between Locations
PCS0	PBA – PBA+127
PCS1	PBA+128 – PBA+255
PCS2	PBA+256 – PBA+383
PCS3	PBA+384 – PBA+511
PCS4	PBA+512 – PBA+639
PCS5	PBA+640 – PBA+767
PCS6	PBA+768 – PBA+895

Ready Generation Logic

The SAB 80188 can generate a ready signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of wait states to be inserted for each peripheral or memory is programmable to provide 0 to 3 wait states for all accesses to the area for which the chip select is active. In addition, the SAB 80188 may be programmed to either ignore external ready for each chip select range individually or to factor external ready with the integrated ready generator.

Ready control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the SAB 80188.

Chip Select/Ready Logic and Reset

Upon reset, the chip select/ready logic will perform the following actions:

- All chip select outputs will be driven high.
- Upon leaving reset, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1 K block with the accompanying ready control bits set at 011 to allow the maximum number of internal wait states in conjunction with external ready consideration (i.e. UMCS resets to FFFBH).
- No other chip select or ready control registers have any predefined values after reset. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

3

DMA Channels

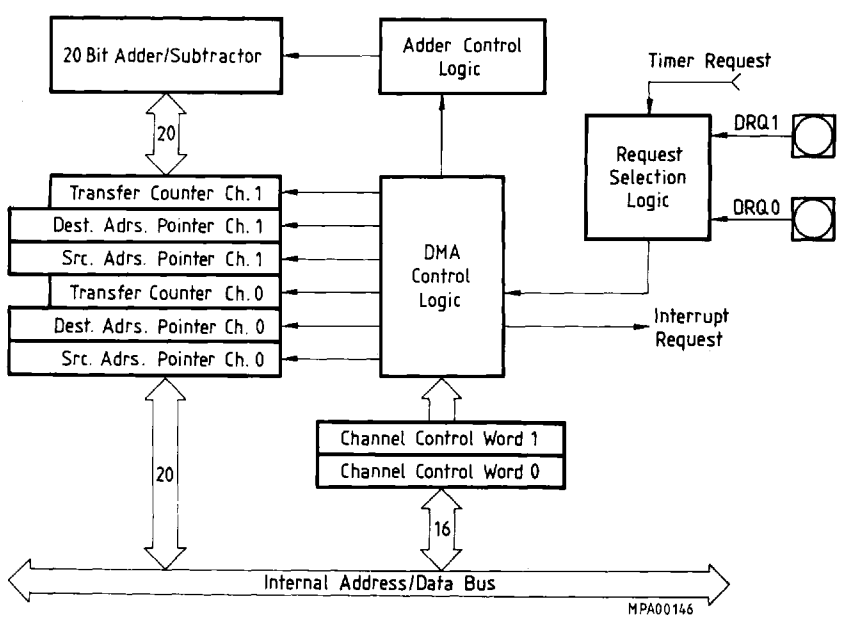
The SAB 80188 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory-to-I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of 1 Mbyte/s.

DMA Channel Control Word Register

Each DMA channel control word determines the mode of operation for the particular SAB 80188 DMA channel.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Unit Block Diagram

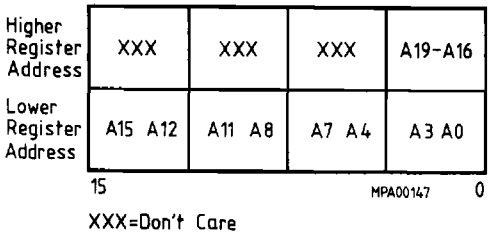


DMA Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/IO#	Destination DEC	INC	M/IO#	Source DEC	INC	TC	INT	SYN		P	TDRQ	X	CHG/NOCHG#	ST/STOP#	X

X=Don't Care

DMA Memory Pointer Register Format



XXX=Don't Care

DMA Control Block Format

Register Name	Register Address	
	Chan. 0	Chan. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

DMA Control Word Bit Description

ST/$\overline{\text{STOP}}$ Start/stop (1/0) channel.

CHG/$\overline{\text{NOCHG}}$ Change/do not change (1/0)ST/$\overline{\text{STOP}}$ bit. If this bit is set when writing to the control word, the ST/$\overline{\text{STOP}}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{\text{STOP}}$ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT Enable interrupts to CPU on byte count termination.

TC If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{\text{STOP}}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN (2 bits) 00 No synchronization.
Note: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
01 Source synchronization. 10 Destination synchronization. 11 Unused.

TDRQ 0: Disable DMA requests from timer 2.
1: Enable DMA requests from timer 2.

Source: INC Increment source pointer by 1 after each transfer.
M/$\overline{\text{IO}}$ Source pointer is in M/IO space (1/0).
DEC Decrement source pointer by 1 after each transfer.

Destin.: INC Increment destination pointer by 1 after each transfer.
M/$\overline{\text{IO}}$ Destination pointer is in M/IO space (1/0).
DEC Decrement destination pointer by 1 after each transfer.

P Channel priority – relative to other channel.
0 low priority. 1 high priority.
Channels will alternate cycles if both set at same priority level.

Bit 0 Bit 0 is not used.

Bit 3 Bit 3 is not used.

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DMA Destination and Source Pointer Register

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA control register.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred.

DMA Priority

The DMA channels may be programmed such that one channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; however, an external bus hold takes priority over an internal DMA cycle.

DMA Channels and Reset

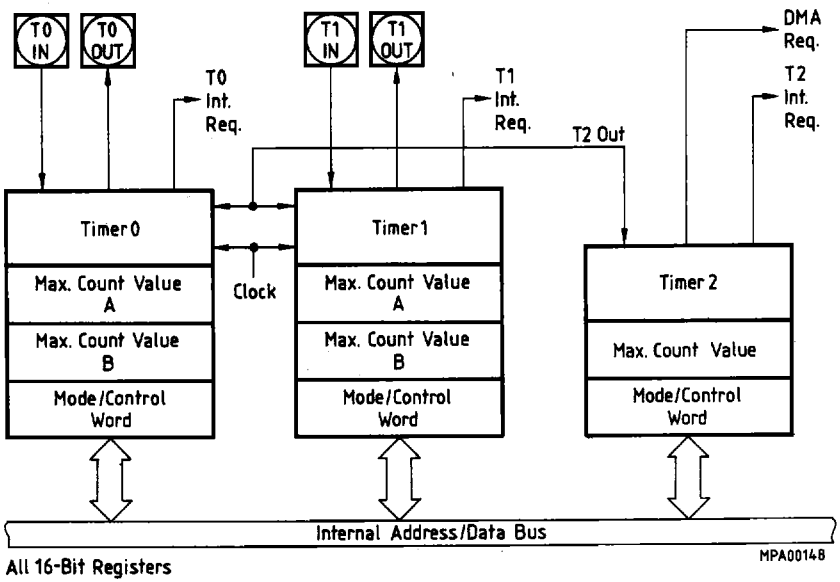
Upon reset, the DMA channels will perform the following actions:

- The start/stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

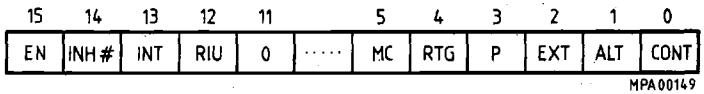
Timers

The SAB 80188 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

Timer Block Diagram



Timer Mode/Control Register



Timer Control Block Format

Register Name	Register Offset		
	TMR 0	TMR 1	TMR 2
Mode/Control Word	56H	5EH	66H
Max. Count B	54H	5CH	not present
Max. Count A	52H	5AH	62H
Count Register	50H	58H	60H

Timer Operation

The timers are controlled by eleven 16-bit registers in the internal peripheral control block. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a max. count register, which defines the maximum count the timer will reach. After reaching the max. count register value, the timer count value will be reset to zero during that same clock.

Each timer gets serviced every fourth CPU clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU clock rate (2 MHz for an 8 MHz CPU clock).

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between max. count registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max. Count Registers

Timers 0 and 1 have two max. count registers, while timer 2 has a single max.count register. These contain the number of events the timer will count. In timers 0 and 1, the max.count register used can alternate between the two max.count values whenever the current maximum count is reached.

Timer Mode/Control Register

The mode/control register allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

ALT:
The ALT bit determines which of two max. count registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one max.count register while the other is being used, and thus provides a method of generating nonrepetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go low for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current max.count register being used (0/1 for B/A).

CONT:
Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the max. count register A value, be reset, count to the register B value, be reset, and halt.

EXT:
The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the SAB 80188 clock. If EXT is set, the timer will count low-to-high transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input-to-output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:
The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:
Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is high, the timer will count; if the input pin is low, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the SAB 80188 clock.

When RTG = 1, the input pin detects low-to-high transitions. The first transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:
The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during which the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:
The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual max.count register mode, an interrupt will be generated each time the value in max.count register A is reached, and each time the value in max.count register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the interrupt controller.)

MC:
The maximum count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual max.count register mode, this bit will be set each time the value in max.count register A is reached, and each time the value in max.count register B is reached. This bit is set regardless of the timer's interrupt enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.
Programmer intervention is required to clear this bit.

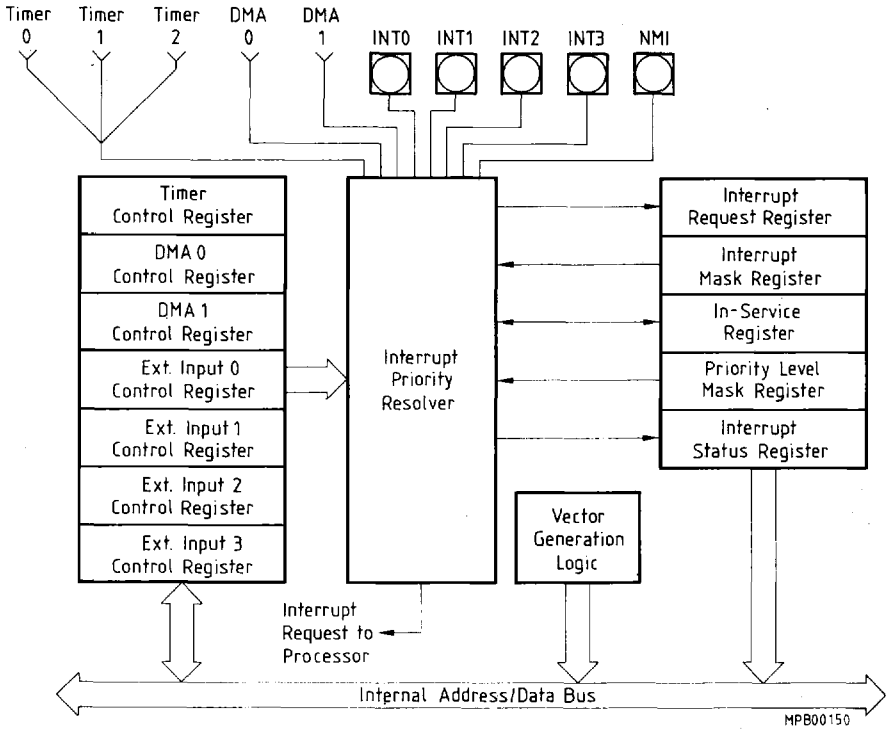
RIU:
The register in use bit indicates which max.count register is currently being used for comparison to the timer count value. A zero indicates register A. The RIU bit cannot be written, i.e. its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.
Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:
ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Timers and Reset

Upon reset, the timers will perform the following actions:

- All EN (enable) bits are reset preventing timer counting.
- All SEL (select) bits are reset to zero. This selects max. count register A, resulting in the timer-out pins going high upon reset.

Interrupt Controller Block Diagram



Interrupt Controller

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The SAB 80188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU. Internal interrupt sources (timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The SAB 80188 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts.
The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the SAB 80188 within the iRMX 86 operating system interrupt structure.

Master Mode Operation

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge output lines. When the interrupt lines are configured in cascade mode, the SAB 80188 interrupt controller will not generate internal interrupt vectors.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the SAB 8259A. The interrupt controller responds identical to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins.

Fully nested mode

When in fully nested mode, four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit (IS) is provided for every interrupt source. If a lower priority device requests an interrupt while the in-service bit is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller.
When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register.

Cascade mode

The SAB 80188 has four interrupt pins and two of them have dual functions. In fully nested mode, the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. INT0 is an interrupt input interfaced to an SAB 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to the peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value INT0 and INT1 control registers.
The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave SAB 8259As.

Special fully nested mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external SAB 8259A masters. In special fully nested mode, the SAB 80188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin.

Polling operation

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the poll word. Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service.

Interrupt Controller Registers (non-iRMX 86 mode)

	Offset
INT3 Control Register	3EH
INT2 Control Register	3CH
INT1 Control Register	3AH
INT0 Control Register	38H
DMA1 Control Register	36H
DMA0 Control Register	34H
Timer Control Register	32H
Interrupt Status Register	30H
Interrupt Request Register	2EH
In-Service Register	2CH
Priority Mask Register	2AH
Mask Register	28H
Poll Status Register	26H
Poll Register	24H
EOI Register	22H

Timer/DMA Control Register Formats

15	14	...	4	3	2	1	0
0	0	...	0	MSK	PR2	PR1	PR0

INT0/INT1 Control Register Formats

15	14	...	7	6	5	4	3	2	1	0
0	0	...	0	SFNM	C	LTM	MSK	PR2	PR1	PR0

INT2/INT3 Control Register Formats

15	14	...	5	4	3	2	1	0
0	0	...	0	LTM	MSK	PR2	PR1	PR0

In-Service, Interrupt Request, and Mask Register Formats

15	14	...	10	9	8	7	6	5	4	3	2	1	0
0	0	...	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Priority Mask Register Format

15	14	...	3	2	1	0
0	0	...	0	PRM2	PRM1	PRM0

Interrupt Status Register Format

15	14	...	7	6	5	4	3	2	1	0
DHLT	0	...	0	0	0	0	0	IRT2	IRT1	IRT0

EOI Register Format

15	14	13	...	5	4	3	2	1	0
SPEC/NSPEC	0	0	...	0	S4	S3	S2	S1	S0

Poll Register Format

15	14	13	...	5	4	3	2	1	0
INT REQ	0	0	...	0	S4	S3	S2	S1	S0

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Master Mode Features

Programmable priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0 to 7) in the control register of each interrupt source.

End-of-interrupt command

The end-of-interrupt (EOI) command is used by the programmer to reset the in-service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The non-specific command does not specify which IS bit is reset.

Trigger mode

The four external interrupt pins can be programmed in either edge or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active high. In the edge-sense mode or the level-trigger mode, the interrupt request must remain active (high) until the interrupt request is acknowledged by the SAB 80188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go low for at least one clock cycle to reenable the input.

Interrupt vectoring

The SAB 80188 interrupt controller will generate interrupt vectors for the integrated DMA channels and the integrated timers. In addition, the interrupt controller will generate interrupt vectors for the external interrupt lines if they are not configured in cascade or special fully nested mode.

Interrupt Controller Registers

In-service register

This register contains the in-service bit for each of the interrupt sources. The in-service bit is set to indicate that a source's service routine is in progress. When an in-service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the in-service bit for all three timers; the D0 and D1 bits are the in-service bits for the two DMA channels; the I0 – I3 bits are the in-service bits for the external interrupt pins.

Interrupt request register

The internal interrupt sources have interrupt request bits inside the interrupt controller. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

Mask register

This is a 16-bit register that contains a mask bit for each interrupt source. A one in a bit position corresponding to a particular source serves to mask the source from generating interrupts. These mask bits are exactly the same bits which are used in the individual control registers.

Priority mask register

This register is used to mask all interrupts below particular interrupt priority levels. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified.

Interrupt status register

This register contains general interrupt controller status information. The bits in the status register have the following functions:

DHLT: DMA halt transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests.

Timer, DMA 0, 1 control registers

These registers are the control words for all the internal interrupt sources. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are exactly the same bits as are in the mask register; modifying them in the individual control registers will also modify them in the mask register, and vice versa.

INT0 to INT3 control registers

These registers are the control words for the four external input pins. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

PR0-2: Priority programming information. Highest priority = 000, lowest priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

EOI register

The end-of-interrupt register is a command register which can only be written into. It initiates an EOI command when written to by the SAB 80188 CPU.

S_x: Encoded information that specifies an interrupt source vector type

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, specific = 0.

Poll and poll status registers

These registers contain polling information. They can only be read. Reading the poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt.

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt request = 1; no interrupt request = 0.

iRMX 86 Compatibility Mode

This mode allows iRMX 86-SAB 80188 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave SAB 8259As in cascaded mode. When iRMX mode is used, the internal SAB 80188 interrupt controller will be used as a slave controller to an external master interrupt controller.
Upon reset, the SAB 80188 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the relocation register should be set.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the SAB 80188 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source.

Required iRMX Internal Source Priority Levels

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

iRMX 86 Mode External Interface

In the iRMX 86 configuration of the SAB 80188 the INT0 input is used as the SAB 80188 CPU interrupt input. INT3 functions as an output to send the SAB 80188 slave-interrupt-request to one of the 8 master PIC inputs. Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave SAB 8259As do this internally. Because of pin limitations, the SAB 80188 slave address will have to be decoded externally. $\overline{\text{INT1}}$ is used as a slaveselect input. $\overline{\text{INT2}}$ is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an SAB 8259A.

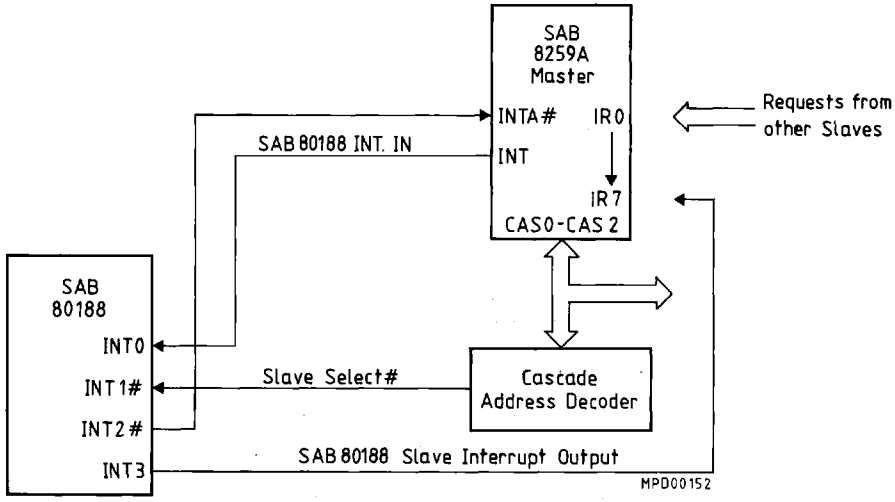
Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of an SAB 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset.

iRMX 86 Interrupt Controller Interconnection



3

Interrupt Controller Registers (iRMX 86 mode)

	Offset
Level 5 Control Register (Timer 2)	3AH
Level 4 Control Register (Timer1)	38H
Level 3 Control Register (DMA1)	36H
Level 2 Control Register (DMA 0)	34H
Level 0 Control Register (Timer0)	32H
Interrupt Status Register	30H
Interrupt-Request Register	2EH
In-Service Register	2CH
Priority-Level Mask Register	2AH
Mask Register	28H
Specific EOI Register	22H
Interrupt Vector Register	20H

Specific EOI Register Format

15	14	13	. . . . .	8	7	6	5	4	3	2	1	0
0	0	0	. . . . .	0	0	0	0	0	0	L2	L1	L0

In-Service, Interrupt Request, and Mask Register Format

15	14	13	. . . . .	8	7	6	5	4	3	2	1	0
0	0	0	. . . . .	0	0	0	TMR 2	TMR 1	D1	D0	0	TMR 0

Control Word Format

15	14	13	. . . . .	8	7	6	5	4	3	2	1	0
0	0	0	. . . . .	0	0	0	0	0	MSK	PR2	PR1	PR0

Interrupt Vector Register Format

15	14	13	. . . . .	8	7	6	5	4	3	2	1	0
0	0	0	. . . . .	0	t4	t3	t2	t1	t0	0	0	0

Priority Level Mask Register

15	14	13	. . . . .	8	7	6	5	4	3	2	1	0
0	0	0	. . . . .	0	0	0	0	0	0	m2	m1	m0

MPA00153

Interrupt Controller Registers in the iRMX 86 Mode

End-of-interrupt register

The end-of-interrupt register is a command register which can only be written to. It initiates an EOI command when written to by the SAB 80188 CPU.

Lx: Encoded value indicating the priority of the IS bit to be reset.

In-service register

This register contains the in-service bit for each of the internal interrupt sources. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers.

Interrupt request register

This register indicates which internal peripherals have interrupt requests pending. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

Mask register

This register contains a mask bit for each interrupt source. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked.

Control registers

These registers are the control words for all the internal interrupt sources.

PRx: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

MSK: Mask bit for the priority level indicated by PRx bits.

Interrupt vector register

This register provides the upper five bits of the interrupt vector address. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

tx: 5-bit field indicating the upper five bits of the vector address.

Priority-level mask register

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

mx: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

Interrupt status register

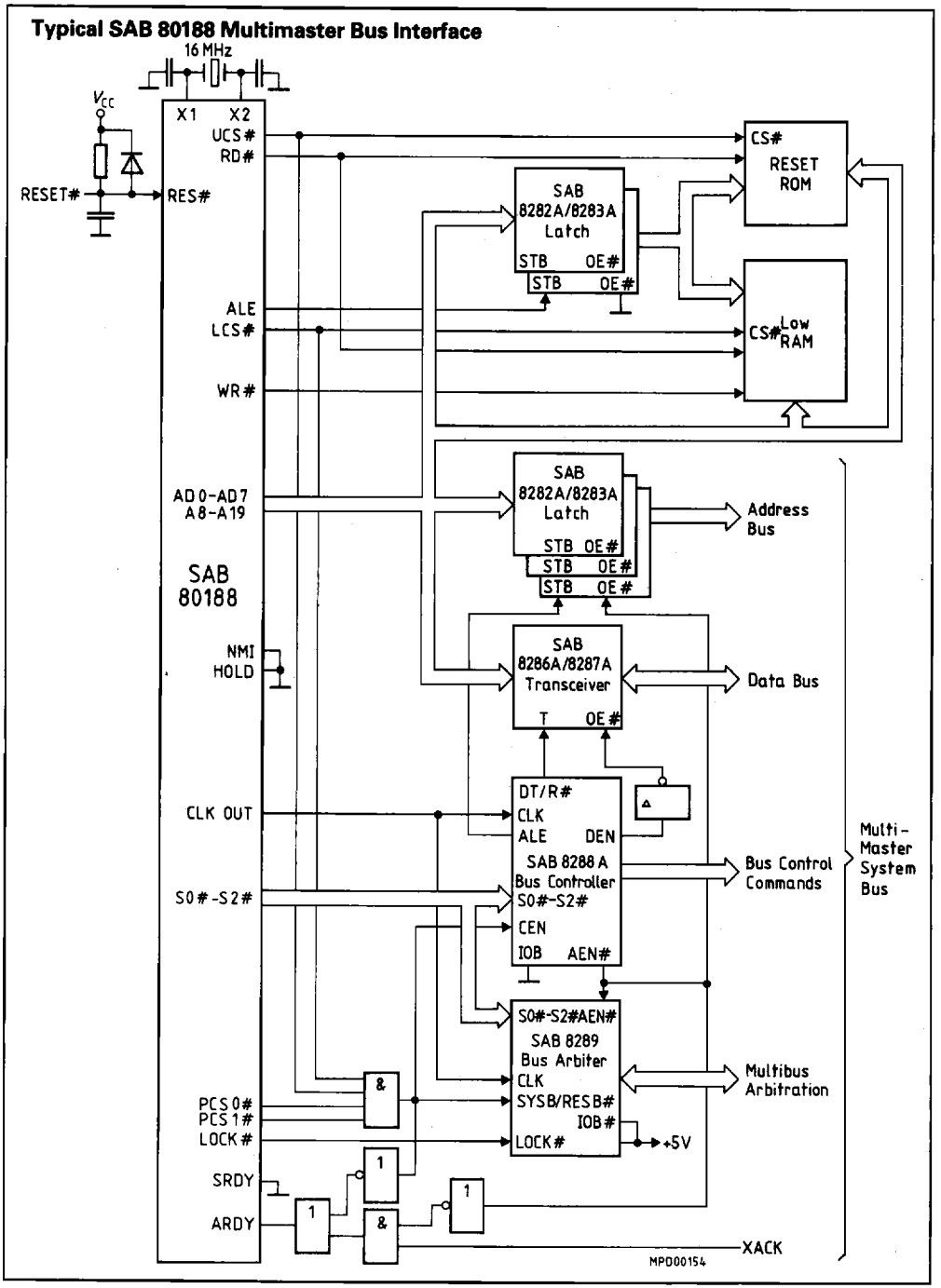
This register is defined exactly as in non-iRMX mode.

Interrupt Controller and Reset

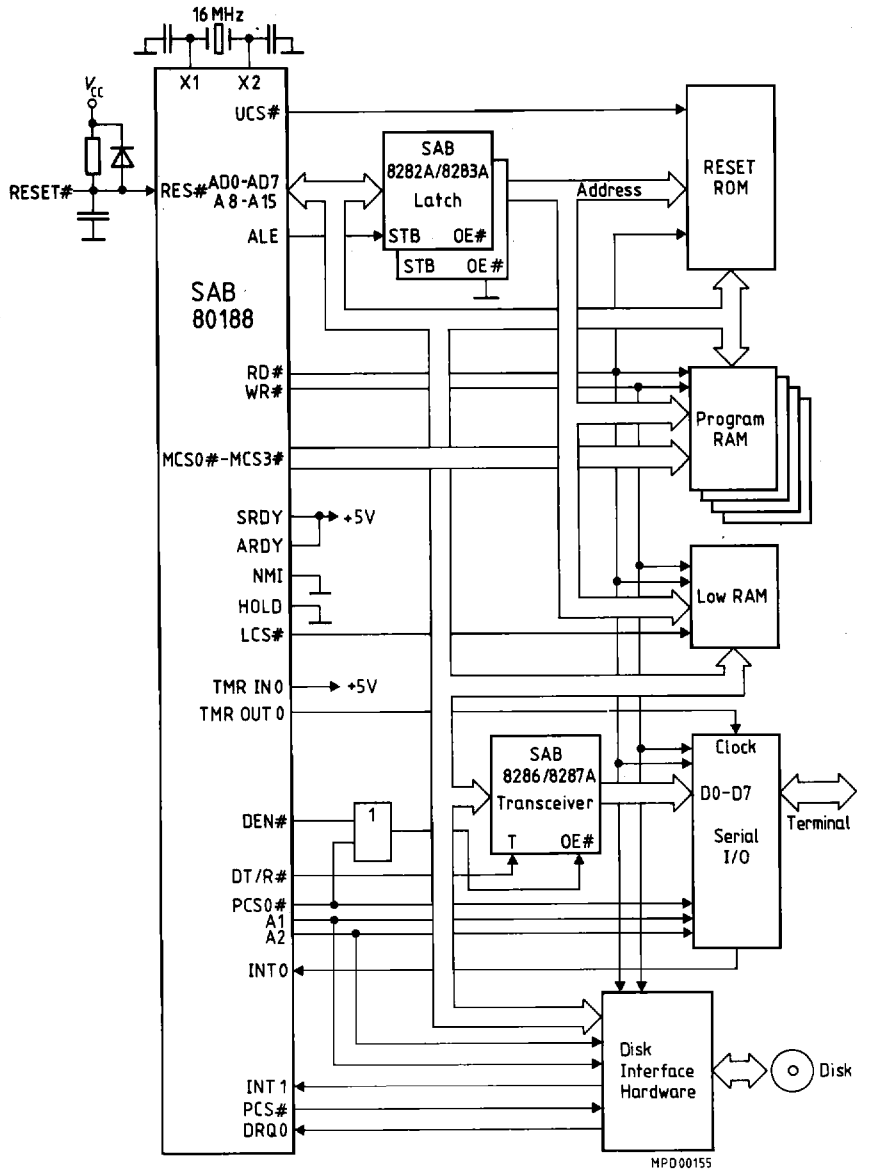
Upon reset, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying fully nested mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All interrupt service bits reset to 0.
- All interrupt request bits reset to 0.
- All MSK (interrupt mask) bits set to 1 (mask).
- All C (cascade) bits reset to 0 (non-cascade).
- All PRM (Priority mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

Typical SAB 80188 Multimaster Bus Interface



Typical SAB 80188 System Configuration



Instruction Timings

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The op code, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word data is located on even-address boundaries.

All jumps and calls include the time required to fetch the op code of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the execution unit.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP	if r/m = 100 then EA = (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP	if r/m = 101 then EA = (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP	if r/m = 110 then EA = (BP) + DISP*
if r/m = 011 then EA = (BP) + (DI) + DISP	if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

REG is assigned according to the following table:

16-bit (w = 1)	8-bit (w = 0)	16-bit (w = 1)	8-bit (w = 0)
000 AX	000 AL	100 SP	100 AH
001 CX	001 CL	101 BP	101 CH
010 DX	010 DL	110 SI	110 DH
011 BX	011 BL	111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

* except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

Note: EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment override prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment register
00	ES
01	CS
10	SS
11	DS

Instruction Set Summary

Function	Format	Clock Cycles	Comments
Data Transfer			
MOV = Move:			
Register to register/memory	1000100w | mod reg r/m	2/12	
Register/memory to register	1000101w | mod reg r/m	2/9	
Immediate to register/memory	1100011w | mod 000 r/m | data | data if w = 1	12–13	8/16-bit
Immediate to register	1011w reg | data | data if w = 1	3–4	8/16-bit
Memory to accumulator	1010000w | addr-low | addr-high	9	
Accumulator to memory	1010001w | addr-low | addr-high	8	
Register/memory to segment register	10001110 | mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 | mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 | mod 110 r/m	16	
Register	01010 reg	10	
Segment register	000reg 110	9	
POP = Pop:			
Memory	10001111 | mod 000 r/m	20	
Register	01011 reg	10	
Segment register	000reg 111 (reg ≠ 01)	8	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Data Transfer (cont'd)			
XCHG = Exchange:			
Register/memory with register	1000011w mod reg r/m	4/17	
Register with accumulator	10010 reg	3	
IN = Input from:			
Fixed port	1110010w port	10	
Variable port	1110110w	8	
OUT = Output to:			
Fixed port	1110011w port	9	
Variable port	1110111w	7	
XLAT = Translate byte to AL	11010111	11	
LEA = Load EA to register	10001101 mod reg r/m	6	
LDS = Load pointer to DS	11000101 mod reg r/m (mod ≠ 11)	18	
LES = Load pointer to ES	11000100 mod reg r/m (mod ≠ 11)	18	
LAHF = Load AH with flags	10011111	2	
SAHF = Store AH into flags	10011110	3	
PUSHF = Push flags	10011100	9	
POPF = Pop flags	10011101	8	
SEGMENT = Segment override:			
CS	00101110	2	
SS	00110110	2	
DS	00111110	2	
ES	00100110	2	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Arithmetic			
ADD = Add:			
Reg./memory with register to either	00000dw | mod reg. r/m	3/10	
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0000010w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg./memory with register to either	000100dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0001010w | data | data if w = 1	3/4	8/16-bit
INC = Increment			
Register/memory	1111111w | mod 000 r/m	3/15	
Register	01000 reg	3	
SUB = Subtract			
Reg./memory and register to either	001010dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0010110w | data | data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg./memory and register to either	000110dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0001110w | data | data if w = 1	3/4	8/16-bit

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
DEC = **Decrement**:			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = **Compare**:			
Register/memory with register	0 0 1 1 1 0 1 w | mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w=01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m		
register–byte		26–28	
register–word		35–37	
memory–byte		32–34	
memory–word		41–43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
register–byte		25–28	
register–word		34–37	
memory–byte		31–34	
memory–word		40–43	

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m		
register–byte		29	
register–word		38	
memory–byte		35	
memory–word		44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m		
register–byte		44–52	
register–word		53–61	
memory–byte		50–58	
memory–word		59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
Logic			
Shift/rotate instructions:			
Register/memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2/15	
Register/memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n/17+n	

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Logic (cont'd):			
AND = **And:**			
Reg./memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data f w = 1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w = 1	3/4	8/16-bit
OR = **Or:**			
Reg./memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w = 1	3/4	8/16-bit
XOR = **Exclusive Or:**			
Reg./memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w = 1	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	3	

Function	Format	Clock Cycles	Comments
String Manipulation:			
MOVS = Move byte/word	1010010w	14	
CMPS = Compare byte/word	1010011w	22	
SCAS = Scan byte/word	1010111w	15	
LODS = Load byte/word to AL/AX	1010110w	12	
STOS = Store byte/word from AL/AX	1010101w	10	
Repeated by count in CX			
MOVS = Move string	11110010 1010010w	8 + 8n	
CMPS = Compare string	1111001z 1010011w	5 + 22n	
SCAS = Scan string	1111001z 1010111w	5 + 15n	
LODS = Load string	11110010 1010110w	6 + 11n	
STOS = Store string	11110010 1010101w	6 + 9n	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Control Transfer:			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	38	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
JMP = Unconditional jump:			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 100 r/m	11/17	
Direct intersegment	11101010 | segment offset segment selector	14	
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	26	
RET = Return from CALL:			
Within segment	11000011	16	
Within seg. adding immediate to SP	11000010 | data-low | data-high	18	
Intersegment	11001011	22	
Intersegment adding immediate to SP	11001010 | data-low | data-high	25	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
JE/JZ = Jump on equal/zero	01110100 disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100 disp	4/13	
JLE/JNG = Jump on less or equal/not greater	01111110 disp	4/13	
JB/JNAE = Jump on below/not above or equal	01110010 disp	4/13	
JBE/JNA = Jump on below or equal/not above	01110110 disp	4/13	
JP/JPE = Jump on parity/parity even	01111010 disp	4/13	
JO = Jump on overflow	01110000 disp	4/13	
JS = Jump on sign	01111000 disp	4/13	
JNE/JNZ = Jump on not equal/not zero	01110101 disp	4/13	
JNL/JGE = Jump on not less/greater or equal	01111101 disp	4/13	
JNLE/JG = Jump on not less or equal/greater	01111111 disp	4/13	
JNB/JAE = Jump on not below/above or equal	01110011 disp	4/13	
JNBE/JA = Jump on not below or equal/above	01110111 disp	4/13	
JNP/JPO = Jump on not parity/parity odd	01111011 disp	4/13	
JNO = Jump on not overflow	01110001 disp	4/13	
JNS = Jump on not sign	01111001 disp	4/13	
JCXZ = Jump on CX zero	11100011 disp	5/15	
LOOP = Loop CX times	11100010 disp	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001 disp	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000 disp	6/16	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
[redacted]			
INT = **Interrupt:**			
Type specified	11001101 | type	47	
Type 3	11001100	45	
INTO = Interrupt on overflow	11001110	48/4	if INT taken/ if INT not taken
IRET = Interrupt return	11001111	28	
[redacted]			

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Processor Control			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{\text{TEST}}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor extension escape	11011TTT mod LLL r/m (TTT LLL are op codes to processor extension)	6	

Absolute Maximum Ratings

Ambient temperature under bias . . . . . 0 to 70°C
Storage temperature . . . . . −65 to +150°C
Voltage on any pin with respect to ground . . . . . −0.5 to +7V
Power dissipation 3W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ±10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	−0.5	+0.8	V	–
Input high voltage (all except X1 and $\overline{RES}$)	V_{IH}	2.0	V_{CC} +0.5	V	–
Input high voltage ($\overline{RES}$)	V_{IH1}	3.0	V_{CC} +0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_a = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_a = 2.0 mA for all other outputs
Output high voltage	V_{OH}	2.4	–	V	I_{oa} = −400µA
Power supply current	I_{CC}	–	550	mA	T_A = 0°C, All outputs disconnected
		–	450	mA	T_A = 70°C, All outputs disconnected
Input leakage current	I_{LI}	–	±10	µA	0V < V_{IN} < V_{CC}
Output leakage current	I_{LO}	–	±10	µA	0.45V < V_{OUT} < V_{CC}
Clock output low	V_{CLO}	–	0.6	V	I_a = 4.0 mA
Clock output high	V_{CHO}	4.0	–	V	I_{oa} = −200 µA
Clock input low voltage	V_{CLI}	−0.5	0.6	V	–
Clock input high voltage	V_{CHI}	3.9	V_{CC} +1.0	V	–
Input capacitance	C_{IN}	–	10	pF	–
I/O capacitance	C_{IO}	–	20	pF	–

AC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Timing requirements: all timings measured at 1.5V unless otherwise specified

Parameter	Symbol	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
Data in setup (A/D)	t_{DVCL}	20	–	15	–	ns	–
Data in hold (A/D)	t_{CLDX}	10	–	8	–	ns	–
Asynchronous ready (ARDY) active setup time [1]	t_{ARYHCH}	20	–	15	–	ns	–
ARDY inactive setup time	t_{ARYLCL}	35	–	25	–	ns	–
ARDY hold time	t_{CHARYX}	15	–	15	–	ns	–
Asynchronous ready inactive hold time	t_{ARYCHL}	15	–	15	–	ns	–
Synchronous ready (SRDY) transition setup time	t_{SRYCL}	20	–	20	–	ns	–
SRDY transition hold time	t_{CLSRY}	15	–	15	–	ns	–
HOLD setup time [1]	t_{HVCL}	25	–	20	–	ns	–
INTR, NMI, $\overline{\text{TEST}}$, TIMERIN, setup time [1]	t_{INVCH}	25	–	25	–	ns	–
DRQ0, DRQ1 setup time [1]	t_{INVCL}	25	–	20	–	ns	–

[1] To guarantee recognition at next clock.

Master Interfaces Timing Responses

Parameter	Symbol	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
Address valid delay	t_{CLAV}	5	55	5	44	ns	C_L = 20 to 200 pF all outp.
Address hold time	t_{CLAX}	10	–	10	–	ns	–
Address float delay	t_{CLAZ}	t_{CLAX}	35	t_{CLAX}	30	ns	–
Command lines float delay	t_{CHCZ}	–	45	–	40	ns	–
Command lines valid delay (after float)	t_{CHCV}	–	55	–	45	ns	–
ALE width	t_{LHLL}	t_{CLCL}-35	–	t_{CLCL}-30	–	ns	–
ALE active delay	t_{CHLH}	–	35	–	30	ns	–
ALE inactive delay	t_{CHLL}	–	35	–	30	ns	–
Address hold to ALE inactive	t_{LLAX}	t_{CHCL}-25	–	t_{CHCL}-20	–	ns	–
Data valid delay	t_{CLDV}	10	44	10	40	ns	–
Data hold time	t_{CLDOX}	10	–	10	–	ns	–
Data hold after $\overline{WR}$	t_{WHDX}	t_{CLCL}-40	–	t_{CLCL}-34	–	ns	–
Control active delay 1	t_{CVCTV}	10	70	5	40	ns	–
Control active delay 2	t_{CHCTV}	10	55	10	44	ns	–
Control inactive delay	t_{CVDEX}	5	55	5	44	ns	–
$\overline{DEN}$ inactive delay (non-write cycle)	t_{CVDEX}	10	70	10	56	ns	–
Address float to $\overline{RD}$ active	t_{AZRL}	0	–	0	–	ns	–
$\overline{RD}$ active delay	t_{CLRL}	10	70	10	56	ns	–
$\overline{RD}$ inactive delay	t_{CLRH}	10	55	10	44	ns	–
$\overline{RD}$ inactive to address active	t_{RHAV}	t_{CLCL}-40	–	t_{CLCL}-40	–	ns	–
HLDA valid delay	t_{CLHAV}	5	50	5	40	ns	–
$\overline{RD}$ width	t_{RLRH}	2t_{CLCL}-50	–	2t_{CLCL}-46	–	ns	–
$\overline{WR}$ width	t_{WLWH}	2t_{CLCL}-40	–	2t_{CLCL}-34	–	ns	–
Address valid to ALE low	t_{AVAL}	t_{CLCH}-25	–	t_{CLCH}-19	–	ns	–
Status active delay	t_{CHSV}	10	55	10	45	ns	–
Status inactive delay	t_{CLSH}	10	65	10	50	ns	–
Timer output delay	t_{CLTMV}	–	60	–	48	ns	100 pF max.
Reset delay	t_{CLRO}	–	60	–	48	ns	–
Queue status delay	t_{CHQSV}	–	35	–	28	ns	–
Status hold time	t_{CHDX}	10	–	10	–	ns	–
Address valid to clock high	t_{AVCH}	10	–	10	–	ns	–
$\overline{LOCK}$ valid/invalid delay	t_{CLLV}	5	65	5	60	ns	–

Chip Select Timing Responses

Parameter	Symbol	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
Chip select active delay	t_{CLCSV}	–	66	–	45	ns	–
Chip select hold from command inactive	t_{CXCSX}	35	–	35	–	ns	–
Chip select inactive delay	t_{CHCSX}	5	35	5	32	ns	–

CLKIN Requirements

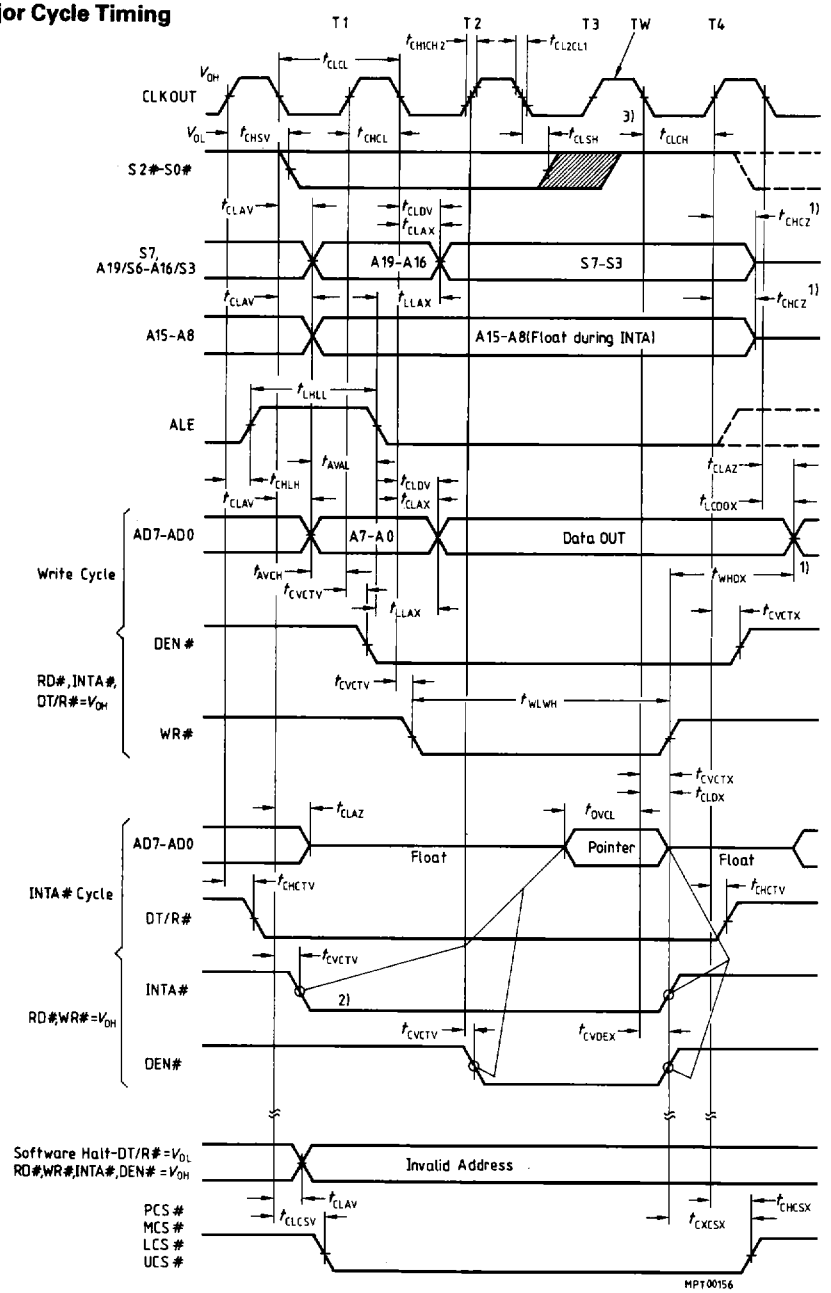
Parameter	Symbol	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
CLKIN period	t_{CKIN}	62.5	250	50	250	ns	–
CLKIN fall time	t_{CKHL}	–	10	–	10	ns	3.5 to 1.0 V
CLKIN rise time	t_{CKLH}	–	10	–	10	ns	1.0 to 3.5 V
CLKIN low time	t_{CLCK}	25	–	20	–	ns	1.5 V
CLKIN high time	t_{CHCK}	25	–	20	–	ns	1.5 V

CLKOUT Timing (200 pF load)

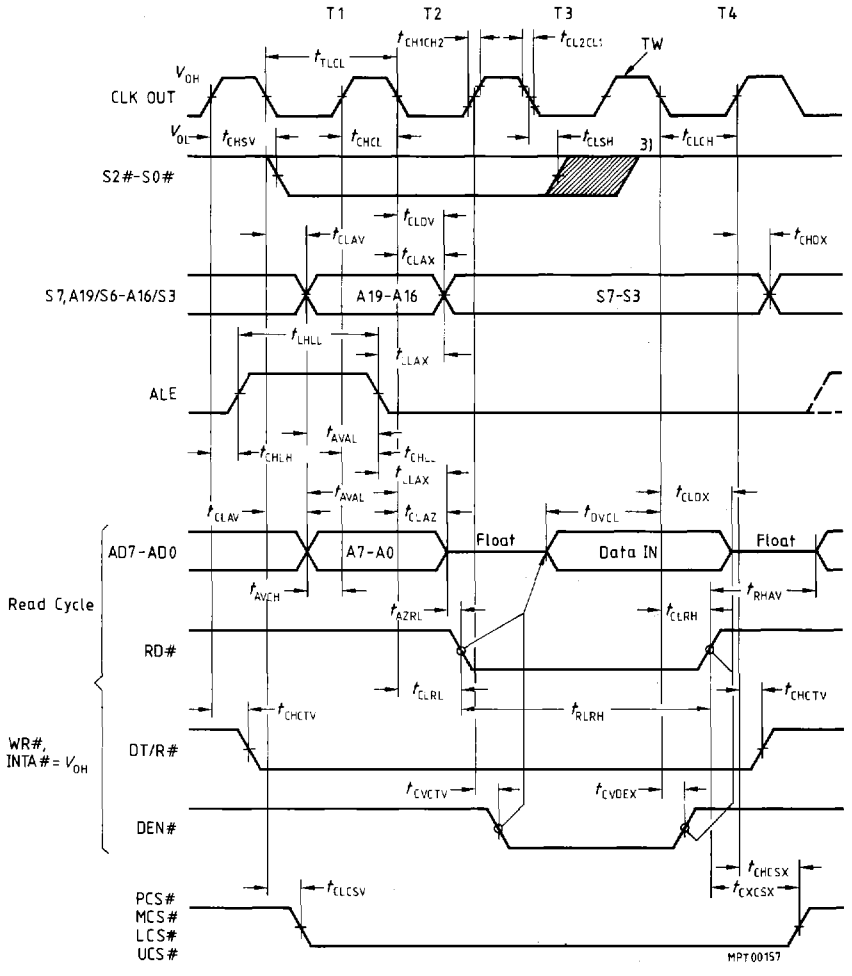
Parameter	Symbol	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
CLKIN to CLKOUT skew	t_{CICO}	–	50	–	25	ns	–
CLKOUT period	t_{CLCL}	125	500	100	500	ns	–
CLKOUT low time	t_{CLCH}	$1/2t_{CLCL}$-7.5	–	$1/2t_{CLCL}$-6.0	–	ns	1.5 V
CLKOUT high time	t_{CHCL}	$1/2t_{CLCL}$-7.5	–	$1/2t_{CLCL}$-6.0	–	ns	1.5 V
CLKOUT rise time	t_{CH1CH2}	–	15	–	12	ns	1.0 to 3.5 V
CLKOUT fall time	t_{CL2CL1}	–	15	–	12	ns	3.5 to 1.0 V

Waveforms

Major Cycle Timing



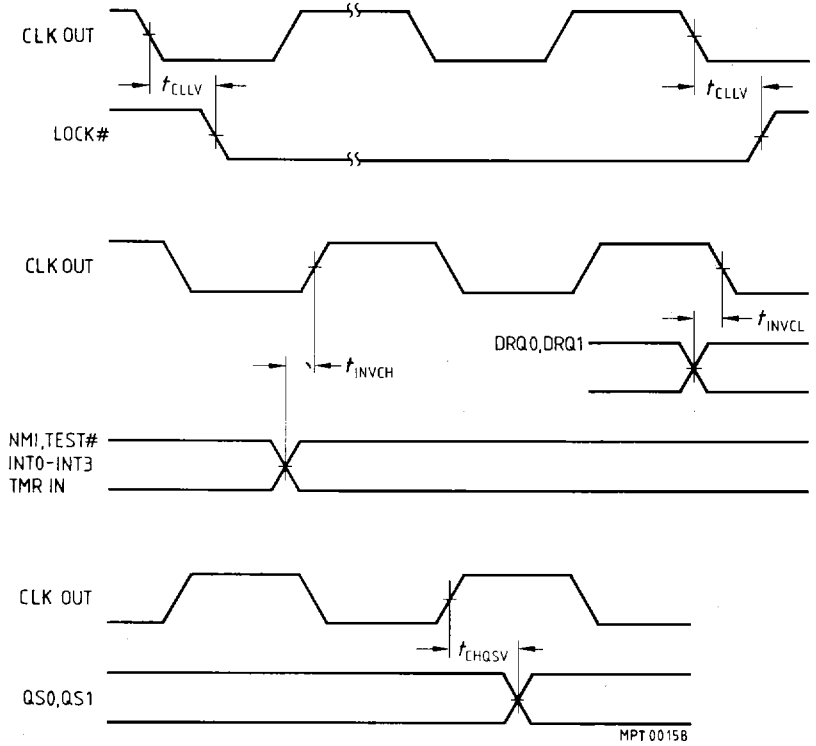
Major Cycle Timing (cont'd)



Notes

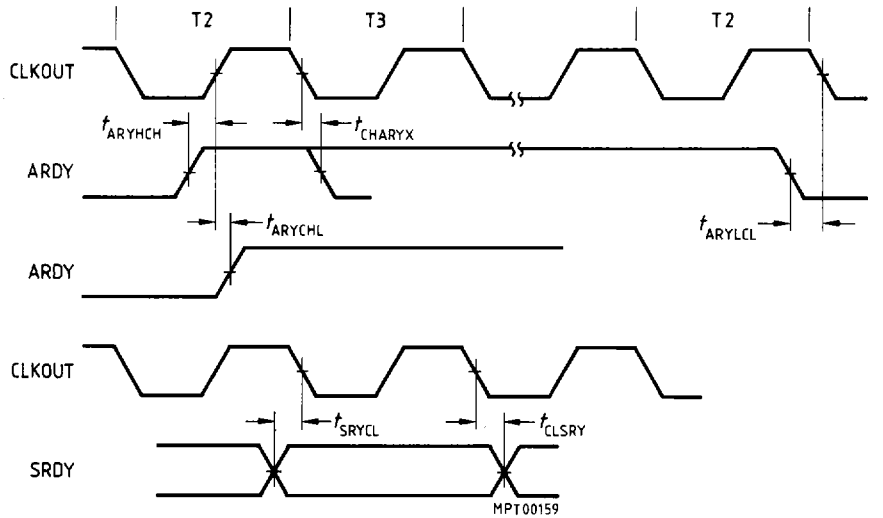
1. Following a write cycle, the local bus is tristated by the SAB 80188 only when the SAB 80188 enters a "hold acknowledge" state.
2. $\overline{\text{INTA}}$ occurs one clock later in iRMX mode.
3. Status inactive just prior to T4.

CLKOUT Timing Relationships

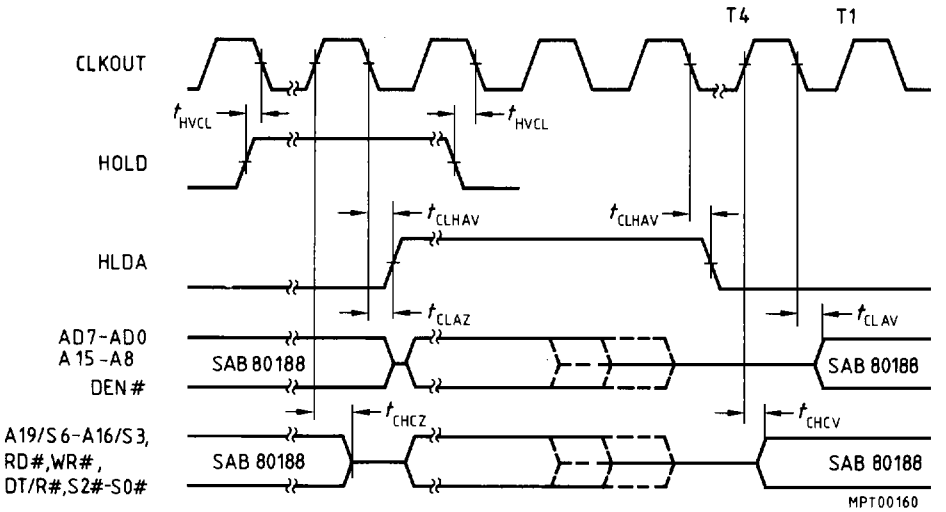


3

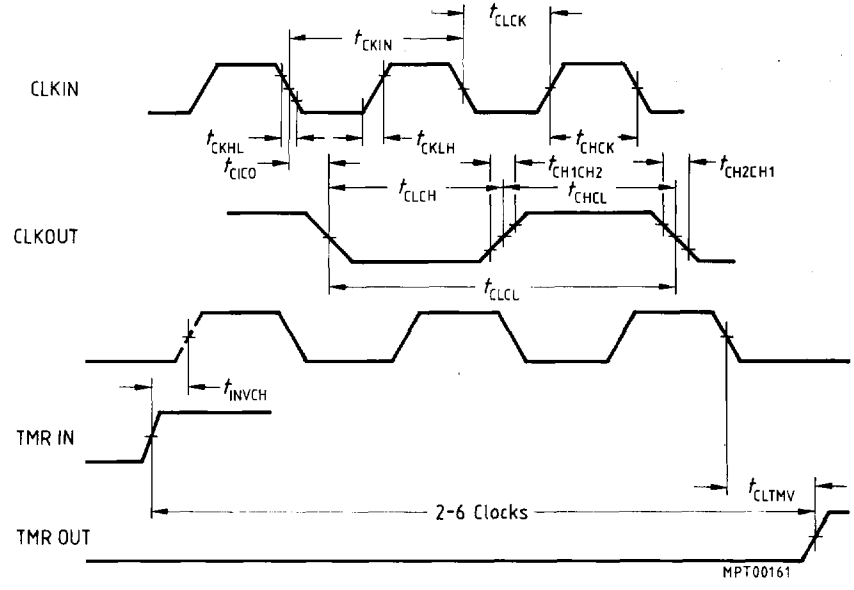
Ready Timing



HOLD-HLDA Timing



Timer Timing



3