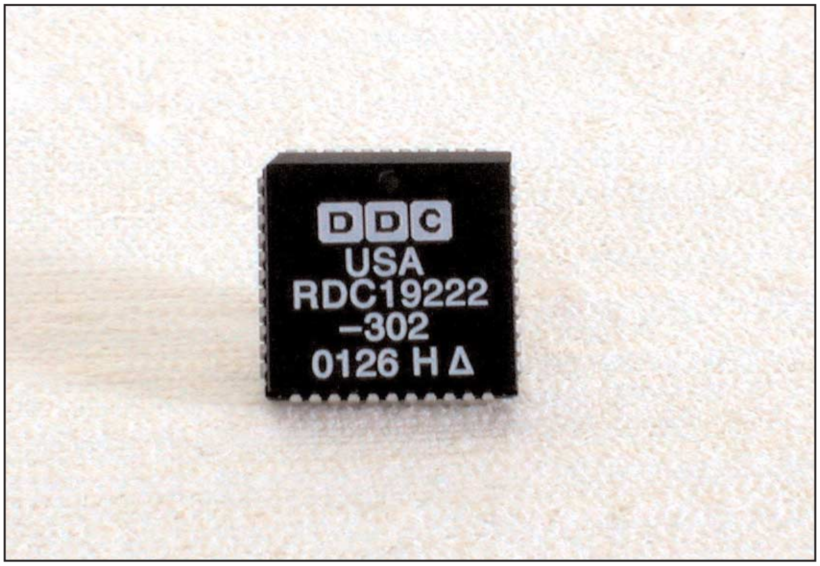
Make sure the next Card you purchase has...

RDC-19220 SERIES

16-BIT MONOLITHIC TRACKING RESOLVER (LVDT)-TO-DIGITAL CONVERTERS



FEATURES

- +5 Volt Only Option
- Only Five External Passive Components
- Programmable:
  - Resolution: 10-, 12-, 14-, or 16-Bit
  - Bandwidth: to 1200 Hz
  - Tracking: to 2300 RPS
- Differential Resolver and LVDT Input Modes
- Velocity Output Eliminates Tachometer
- Built-In-Test (BIT) Output, No 180° Hangup
- Small Size: 40-Pin DDIP or 44-Pin J-Lead Package
- -55° to +125°C Operating Temperature Available

DESCRIPTION

The RDC-19220 Series of converters are low-cost, versatile, 16-bit monolithic, state-of-the-art Resolver(/LVDT)-to-Digital Converters. These single-chip converters are available in small 40-pin DDIP, or 44-pin J-Lead packages and offer programmable features such as resolution, bandwidth and velocity output scaling.

Resolution programming allows selection of 10-, 12-, 14-, or 16-bit, with accuracies to 2.3 min. This feature combines the high tracking rate of a 10-bit converter with the precision and low-speed velocity resolution of a 16-bit converter in one package.

The velocity output (VEL) from the RDC-19220 Series, which can be used to replace a tachometer, is a 4 V signal (3.5 V with the +5 V only option) referenced to ground with a linearity of 0.75% of output voltage. The full scale value of VEL is set by the user with a single resistor.

RDC-19220 Series converters are available with operating temperature ranges of 0° to +70°C, -40° to +85°C and -55° to +125°C. Military processing is available (consult factory).

APPLICATIONS

With its low cost, small size, high accuracy and versatile performance, the RDC-19220 Series converter is ideal for use in modern high-performance industrial and military control systems. Typical applications include motor control, radar antenna positioning, machine tool control, robotics, and process control. MIL-PRF-38534 processing is available for military applications.

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7382

©Data Device Corporation

Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716
631-567-5600 Fax: 631-567-7358
www.ddc-web.com

© 1999 Data Device Corporation

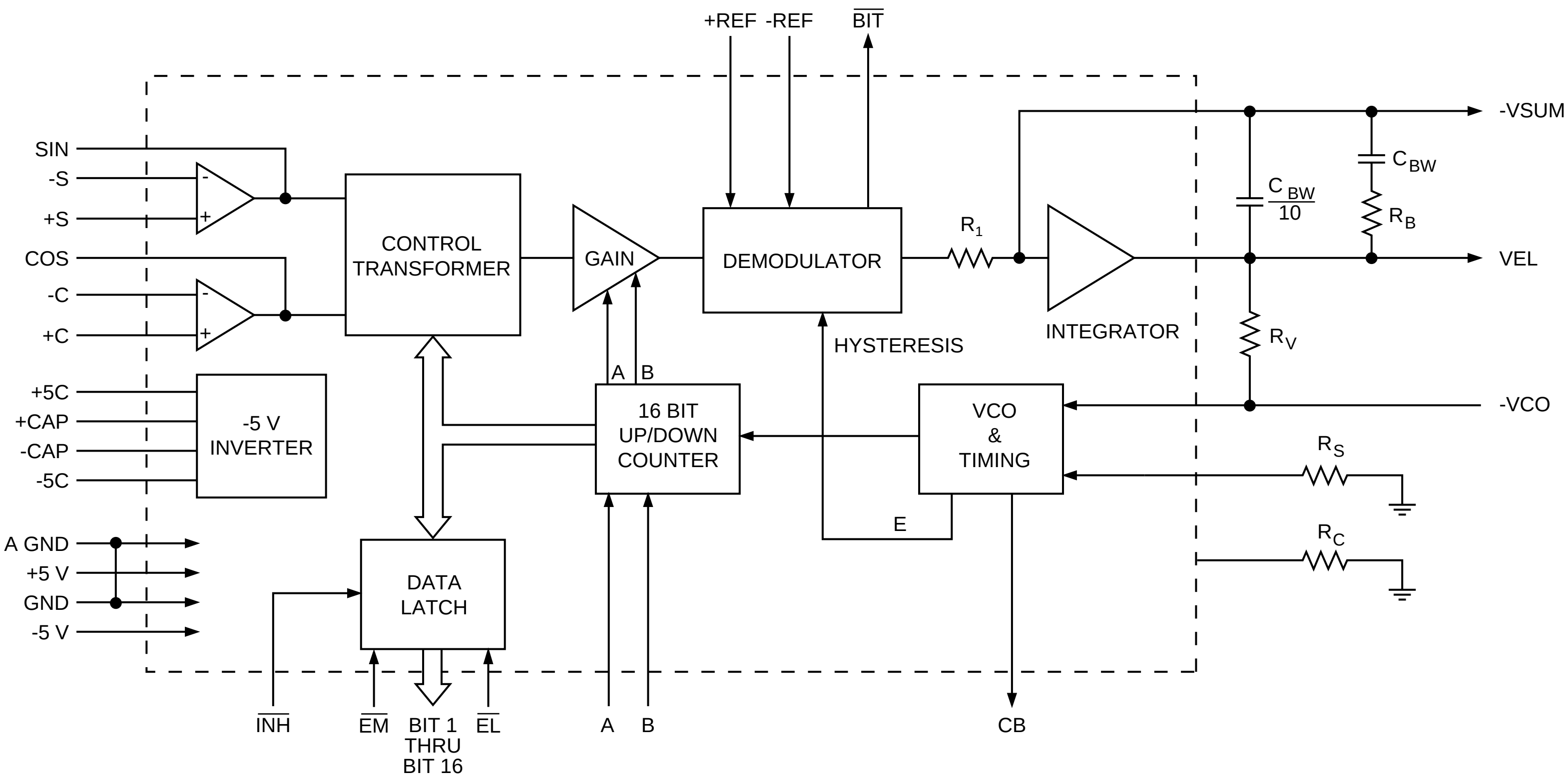


FIGURE 1. RDC-19220 SERIES BLOCK DIAGRAM

TABLE 1. RDC-19220 SPECIFICATIONS

These specifications apply over the rated power supply, temperature and reference frequency ranges, and 10% signal amplitude variation and harmonic distortion.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	10, 12, 14, or 16
ACCURACY	Min	4 or 2 + 1 LSB (note 3)
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE		(+REF, -REF)
Type		Differential
Voltage:		
differential	Vp-p	10 max
single ended	Vp	±5 max
overload	V	±25 continuous, 100 transient
Frequency	Hz	DC to 40,000 (note 4)
Input Impedance	Ohm	10M min // 20 pf
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)
Type		Resolver, differential, groundbased
Voltage: operating	Vrms	2 ±15%
overload	V	±25 continuous
Input impedance	Ohm	10M min//10 pf.
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading =10 µA max pull-up current source to +5 V //5 pF max. CMOS transient protected
Inhibit (INH)		Logic 0 inhibits; Data stable within 0.3 µs
Enable Bits 1 to 8 (EM) Enable Bits 9 to 16 (EL)		Logic 0 enables; Data stable within 150 ns Logic 1 = High Impedance Data High Z within 100 nS
Resolution and Mode Control (A & B) (see notes 1 and 2.)		Mode / B / A / Resolution: resolver 0 0 10 bits " 0 1 12 bits " 1 0 14 bits " 1 1 16 bits LVDT -5 V 0 8 bits " 0 -5 V 10 bits " 1 -5 V 12 bits " -5 V -5 V 14 bits
Outputs		
Parallel Data (1-16)		10, 12, 14, or 16 parallel lines; natural binary angle positive logic (see TABLE 2)
Converter Busy (CB)		0.25 to 0.75 µs positive pulse leading edge initiates counter update.
Zero Index	(ZI)	Logic 1 at all 0s (ENL to -5 V); LSBs are enabled
Built-in-Test (BIT)		Logic 0 for BIT condition. ±100 LSBs of error typ. with a filter of 500 µS, or total Loss-of-Signal (LOS)
Drive Capability		50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100mV min driving CMOS, High Z; 10 uA//5 pF max

TABLE 1. RDC-19220 SPECIFICATIONS (CONT'D)

These specifications apply over the rated power supply, temperature and reference frequency ranges, and 10% signal amplitude variation and harmonic distortion.

PARAMETER	UNIT	VALUE			
DYNAMIC CHARACTERISTICS		(at maximum bandwidth)			
Resolution	bits	10	12	14	16
Tracking Rate (max)(note 4)	rps	1152	288	72	18
Bandwidth(Closed Loop) (max) (note 4)	Hz	1200	1200	600	300
Ka (Note 7)	1/sec^2	5.7M	5.7M	1.4M	360k
A1	1/sec	19.5	19.5	4.9	1.2
A2	1/sec	295k	295k	295k	295k
A	1/sec	2400	2400	1200	600
B	1/sec	1200	1200	600	300
Acceleration (1 LSB lag)	deg/s^2	2M	500k	30k	2k
Settling Time(179° step)	msec	2	8	20	50
VELOCITY CHARACTERISTICS					
Polarity		Positive for increasing angle			
Voltage Range(Full Scale)	V	±4 (at nominal ps)			
Scale Factor Error	%	10 typ	20 max		
Scale Factor TC	PPM/C	100 typ	200 max		
Reversal Error	%	0.75 typ	1.3 max		
Linearity	%	0.25 typ	0.50 max		
Zero Offset	mv	5 typ	10 max		
Zero Offset TC	µV/C	15 typ	30max		
Load	kΩ		8 max		
Noise	(Vp/V)%	1 typ	.125 min 2 max		
POWER SUPPLIES		(note 5)			
Nominal Voltage	V	+5	-5		
Voltage Range	%	± 5	±5		
Max Volt. w/o Damage	V	+7	-7		
Current	mA	14 typ, 22 max (each)			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-20X	°C	-40 to +85			
-10X	°C	-55 to +125			
-A0X	°C	-40 to +125			
Storage					
plastic package	°C	-65 to +150			
ceramic package	°C	-65 to +150			
MOISTURE SENSITIVITY LEVEL	JEDEC	Level 3			
THERMAL RESISTANCE					
Junction-to-Case (θjc)					
40-pin DDIP (ceramic)	°C/W	4.6			
44-pin J-Lead (plastic)	°C/W	72.6			
44-pin J-Lead (ceramic)	°C/W	2.4			
PHYSICAL CHARACTERISTICS					
Size: 40-pin DDIP	in(mm)	2.0 x 0.6 x 0.2 (50.8 x 15.24 x 5.08)			
44-pin J-Lead	in(mm)	0.690 square (17.526)			
Weight:		Plastic	Ceramic		
40-pin DDIP	oz(g)	n/a	0.24 (6.80)		
44-pin J-Lead	oz(g)	0.08 (2.27)	0.065 (1.84)		

Notes for TABLE 1:(from previous page)
1. Unused data bits are set to logic "0."
2. In LVDT mode, bit 16 is LSB for 14-bit resolution or bit 12 is LSB for 10-bit resolution.
3. Accuracy in LVDT mode is 0.15% + 1 LSB of full scale.
4. See text, General Setup Considerations and HigherTracking Rates.
5. See text: General Setup Considerations for RDC19222.
6. Any unused input pins may be left floating (unconnected). All input pins are internally pulled-up to +5 Volts.
7. KA = Acceleration constant, for a full definition see the RDC-19220/RD-19230 application manual acceleration lag section.
8. When using internally generated -5V, the internal -5V charge pump when measured at the converter pin, can read as low as -20% (or -4V).

THEORY OF OPERATION

The RDC-19220 Series of converters are single CMOS custom monolithic chips. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete, high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics and velocity scaling are externally set with passive components.

FIGURE 1 is the functional block diagram of the RDC-19220 Series. The converter operates with ±5 Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of two main sections; a converter and a digital interface. The converter front-end consists of sine and cosine differential input amplifiers. These inputs are protected to ±25 V with 2 kΩ resistors and diode clamps to the ±5 Vdc supplies. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $\mathrm{SIN}\theta\mathrm{COS}\phi - \mathrm{COS}\theta\mathrm{SIN}\phi = \mathrm{SIN}(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

Note: The transfer function of the CT is normally trigonometric, but in LDVT mode the transfer function is triangular (linear) and could thereby convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. For enhanced accuracy, the CT in these converters uses capacitors in precision ratios, instead of the more conventional precision resistor ratios. Capacitors, used as computing elements with op-amps, need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate (67 kHz) to eliminate this drifting and at the same time to cancel out the op-amp offsets.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1(MSB)	180	10800
2	90	5400
3	45	2700
4	22.5	1350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note: $\overline{\mathrm{EM}}$ enables the MSBs and $\overline{\mathrm{EL}}$ enables the LSBs.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies

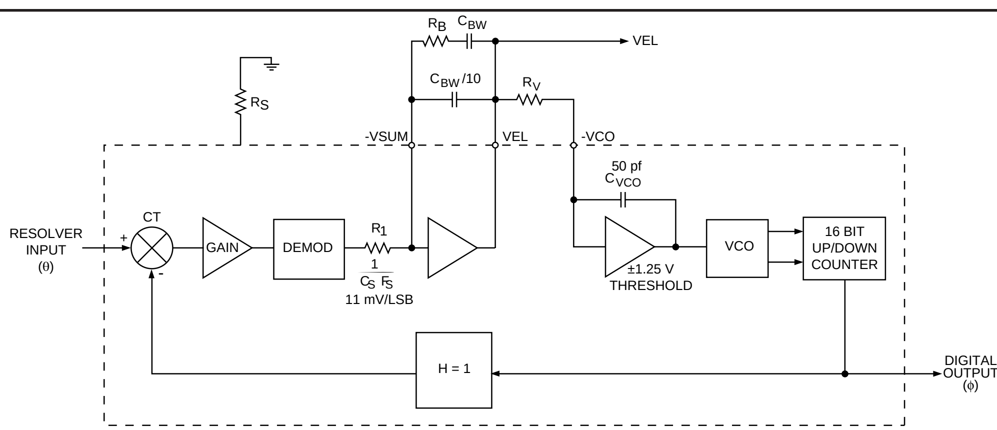


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and its Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2 = A_1A_2$

and B is the frequency of lead compensation.

The components of gain coefficient are error gradient, integrator gain and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod with 2 Vrms input)

- Integrator Gain = $\frac{C_S F_S}{1.1\, C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\, R_V C_{VCO}}$ LSBs per second per volt

where: C_S = 10 pF
F_S = 67 kHz when R_S = 30 kΩ
F_S = 100 kHz when R_S = 20 kΩ
F_S = 134 kHz when R_S = 15 kΩ
C_{VCO} = 50 pF

R_V, R_B, and C_{BW} are selected by the user to set velocity scaling and bandwidth.

GENERAL SETUP CONSIDERATIONS

Note: For detailed application and technical information see the RDC-19220 & RD-19230 series converter applications manual (Document number MN-19220XX-001) which is available for download from the DDC web site @ WWW.DDC-WEB.COM.

DDC has external component selection software which considers all the criteria below, and in a simple fashion, asks the key parameters (carrier frequency, resolution, bandwidth, and tracking rate) to derive the external component value.

The following recommendations should be considered when installing the RDC-19220 Series R/D converters:

1) In setting the bandwidth (BW) and Tracking Rate (TR) (selecting five external components), the system requirements need to be considered. For greatest noise immunity, select the minimum BW and TR the system will allow.

2) Power supplies are ±5 V dc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.

3) Resolver inputs and velocity output are referenced to A GND. This pin should be connected to GND near the converter package. Digital currents flowing through ground will not disturb the analog signals.

4) The $\overline{\text{BIT}}$ output which is active low is activated by an error of approximately 100 LSBs. During normal operation for step inputs or on power up, a large error can exist.

5) This device has several high impedance amplifier inputs (+C, -C, +S, -S, -VCO and -VSUM). These nodes are sensitive to noise and coupling components should be connected as close as possible.

6) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

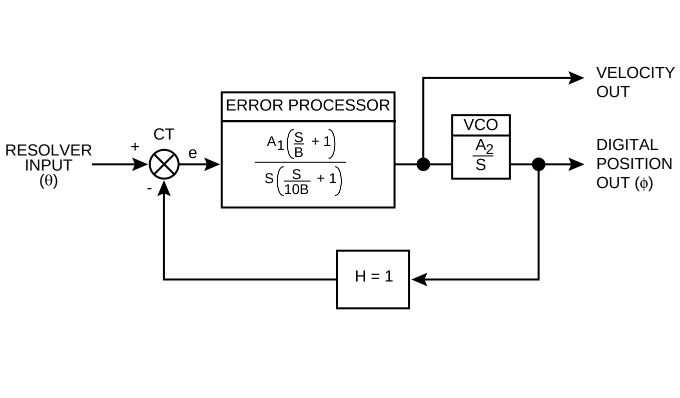


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

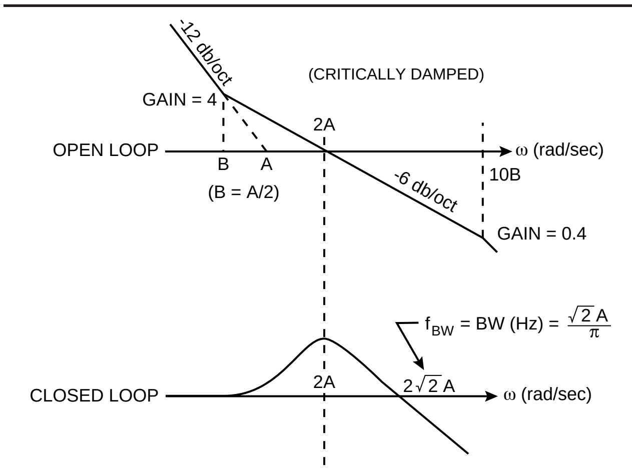


FIGURE 4. BODE PLOTS

TABLE 3. TRACKING/BW RELATIONSHIP	
RPS (MAX)/BW	RESOLUTION
1	10
0.45	12
0.25	14
0.125	16

- Select the desired f_{BW} (closed loop) based on overall system dynamics.

- Select $f_{carrier} \geq 3.5 f_{BW}$

- Compute $R_V = 55\ k\Omega \times \dfrac{\left\{ \text{For the converter's max tracking rate value, see the row indicated in TABLE 4.} \right\}}{\text{Application max. rate}}$

- Compute $C_{BW}\ (pF) = \dfrac{3.2 \times F_S\ (Hz) \times 10^8}{R_V \times (f_{BW})^2}$

- Where F_S = 67 kHz for R_{CLK} = 30 KΩ
  100 kHz for R_{CLK} = 20 KΩ
  134 kHz for R_{CLK} = 15 KΩ

- Compute $R_B = \dfrac{0.9}{C_{BW} \times f_{BW}}$

- Compute $\dfrac{C_{BW}}{10}$

Note: DDC has software available to perform the previous calculations. Contact DDC to request software or visit our website at www.ddc-web.com to download software.

7) Selecting a f_{BW} that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against spin-around is as follows (TABLE 3):

8) **For RDC-19222:**

This version is capable of +5V only operation. It accomplishes this with a charge pump technique that inverts the +5V supply for use as -5V, hence the +5V supply current doubles. The built-in -5 V inverter can be used by connecting pin 2 to 26, pin 17 to 22, a 10 µF/10 Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal), and a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

When using the -5 V inverter, the max. tracking rate should be scaled for a velocity output of 3.5 V max. Use the following equation to determine tracking rate used in the formula on page 5:

$$\text{TR (required)} \times \frac{(4.0)}{(3.5)} = \text{Tracking rate used in calculation}$$

Note: When using the highest BW and Tracking Rates, using the -5 V inverter is not recommended.

HIGHER TRACKING RATES AND CARRIER FREQUENCIES

Tracking rate (nominally 4 V) is limited by two factors: velocity voltage saturation and maximum internal clock rate (nominally 1,333,333 Hz). An understanding of their interaction is essential to extending performance.

The General Setup Considerations section makes note of the selection of R_V for the desired velocity scaling. R_V is the input resistor to an inverting integrator with a 50 pF nominal feedback capacitor. When it integrates to -1.25 V, the converter counts up 1 LSB and when it integrates to +1.25 V, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor; such that, the voltage on it changes 1.25 V in a direction to bring it to 0 V. The output counts per second per volt input is therefore:

$$\frac{1}{(R_V \times 50\ pF \times 1.25)}$$

As an example:

Calculate Rv for the maximum counting rate, at a VEL voltage of 4 V.

For a 12-bit converter there are 2^{12} or 4096 counts per rotation. 1,333,333/4096 = 325 rotations per second or 333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333 \times 50\ pF \times 1.25)} = 48\ k\Omega$$

The maximum rate capability of the RDC-19220 is set by R_S. When R_S = 30 kΩ it is nominally 1,333,333 counts/sec, which equates to 325 rps (rotations per second). This is the absolute maximum rate; it is recommended to only run at <90% of this rate (as seen in TABLE 3), therefore the minimum R_V will be limited to 55 kΩ. The converter maximum tracking rate can be increased 50% in the 16- and 14-bit modes and 100% in the 12- and 10-bit modes by increasing the supply current from 12 to 15 mA (by using an R_C = 23 kΩ), and by increasing the sampling rate by changing R_S to 20 kΩ for 16- and 14-bit resolution or to 15 kΩ for 12- and 10-bit resolution (see TABLE 4).

The maximum carrier frequency can, in the same way, increase from: 5 to 10 kHz in the 16-bit mode, 7 to 14 kHz in the 14-bit mode, 11 to 32 kHz in the 12-bit mode, and 20 to 40 kHz in the 10-bit mode (see TABLE 5).

The maximum tracking rate and carrier frequency for full performance are set by the power supply current control resistor (R_C) per the following tables:

TABLE 4. MAX TRACKING RATE (MIN) IN RPS					
$R_{C/RSET}$ (Ω)	$R_{S/RCLK}$ (Ω)	RESOLUTION			
		10	12	14	16
30k**or open	30k	1152	288	72	18
23k	20k	1728	432	108	27
23k	15k	2304	576	*	*

Depending on the resolution, select one of the values from this row, for use in converter max tracking rate formula. (See previous page for formula.)

* Not recommended.

** The use of a high quality thin-film resistor will provide better temperature stability than leaving open.

TABLE 5. CARRIER FREQUENCY (MAX) IN KHZ					
$R_C/RSET$ (Ω)	$R_{S/RCLK}$ (Ω)	RESOLUTION			
		10	12	14	16
30k** or open	30k	20	11	7	5
23k	30k	24	12	11	7
23k		34 20k	24	14	10
23k	15k	40	32	*	*

* Not recommended.

** The use of a high quality thin-film resistor will provide better temperature stability than leaving open.

Note: R_C "Rcurrent" = RSET
R_S "Rsample" = RCLK

TABLE 6. TRANSFORMERS									
P/N	TYPE	FREQUENCY (HZ)*	IN (VRMS)*	OUT (VRMS)**	ANGLE ACCURACY***	LENGTH (IN)	WIDTH (IN)	HEIGHT (IN)	FIGURE NUMBER
52034	S - R	400	11.8	2	1	0.81	0.61	0.3	5A
52035	S - R	400	90	2	1	0.81	0.61	0.3	5A
52036	R - R	400	11.8	2	1	0.81	0.61	0.3	5B
52037	R - R	400	26	2	1	0.81	0.61	0.3	5B
52038	R - R	400	90	2	1	0.81	0.61	0.3	5B
B-426	Reference	400	115	3.4	N/A	0.81	0.61	0.32	5C
52039-X	Synchro	60	90	2	1	1.1	1.14	.42	5D
24133-X	Reference	60	115	3/6 ****	N/A	1.125	1.125	.42	5D

* ±10% Frequency (Hz) and Line-to-Line input voltage (Vrms) tolerances
** 2 Vrms Output Magnitudes are -2 Vrms ±0.5% full scale
*** Angle Accuracy (Max Minutes)
**** 3 Vrms to ground or 6 Vrms differential (±3% full scale)
Dimensions are for each individual main and teaser
60 Hz Synchro transformers are active (requires ±15 Vdc power supplies)
400 Hz transformer temperature range: -55°C to +125°C
60 Hz transformer (52039-X, 24133-X) temperature ranges: add to part number -1 or -3,
-1 = -55°C to +85°C
-3 = 0 to +70°C

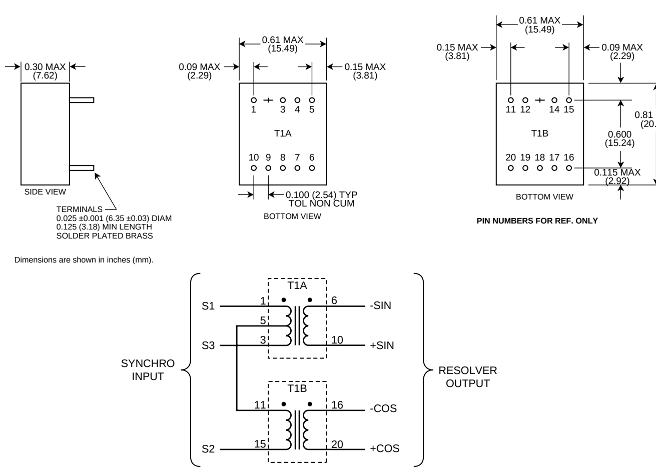


FIGURE 5A. TRANSFORMER LAYOUT AND SCHEMATIC (SYNCHRO INPUT - 52034/52035)

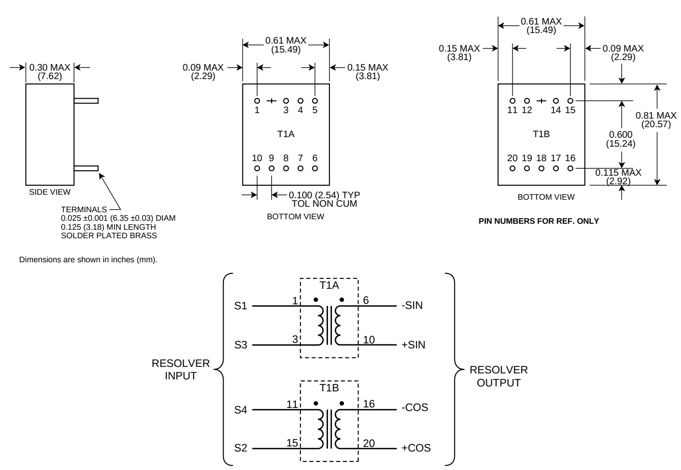
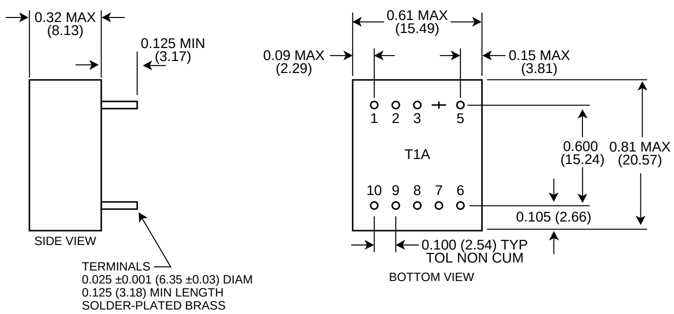


FIGURE 5B. TRANSFORMER LAYOUT AND SCHEMATIC (RESOLVER INPUT - 52036/52037/52038)



Dimensions are shown in inches (mm).

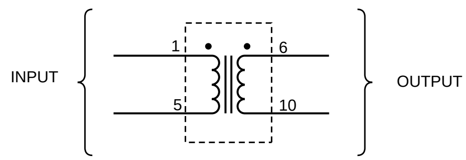
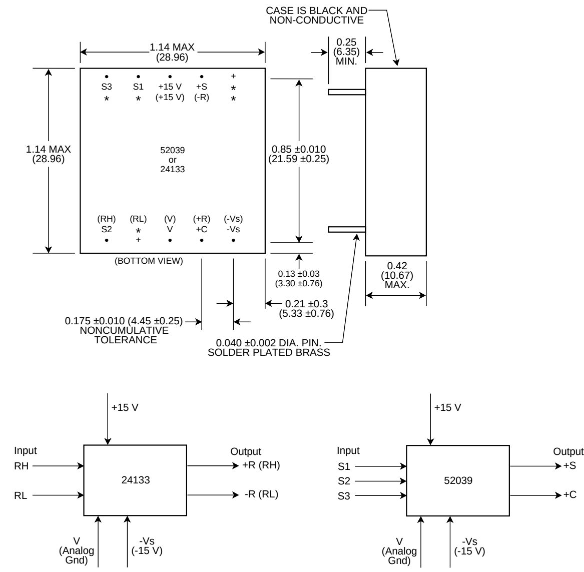


FIGURE 5C. TRANSFORMER LAYOUT AND SCHEMATIC (REFERENCE INPUT - B-426)



The mechanical outline is the same for the synchro input transformer (52039) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.

FIGURE 5D. 60 HZ SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS (SYNCHRO INPUT - 52039 / REFERENCE INPUT - 24133)

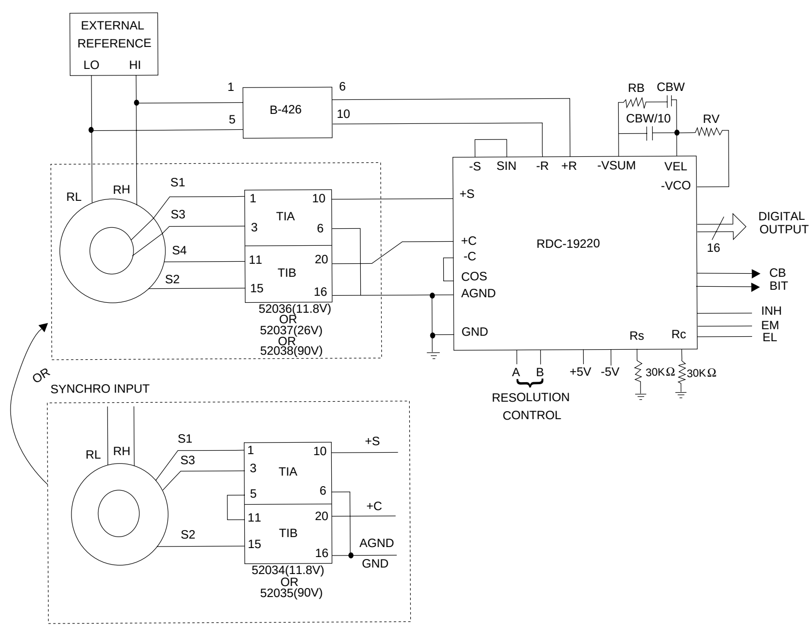
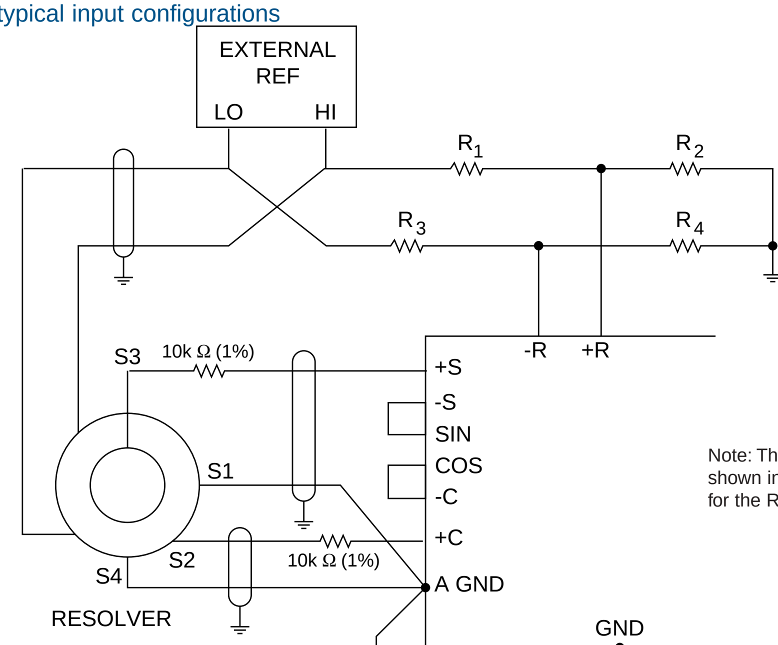


FIGURE 6. TYPICAL TRANSFORMER CONNECTIONS

TYPICAL INPUT CONNECTIONS

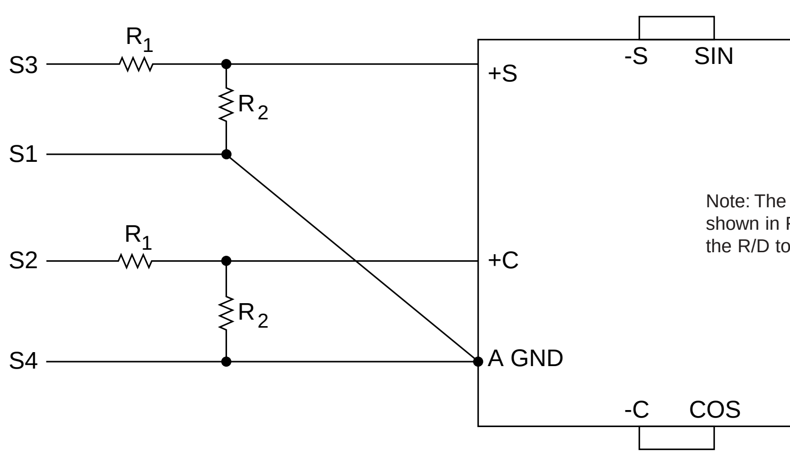
FIGURES 7 through 9 illustrate typical input configurations



Note: The five external BW components as shown in FIGURE 1 and 2 are necessary for the R/D to function.

Notes:
1) Resistors selected to limit Vref peak to between 1 V and 4 V.
2) External reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.
3) See thin film network DDC-55688-1.

FIGURE 7A. TYPICAL CONNECTIONS, 2 V RESOLVER, DIRECT INPUT



Note: The five external BW components as shown in FIGURE 1 and 2 are necessary for the R/D to function.

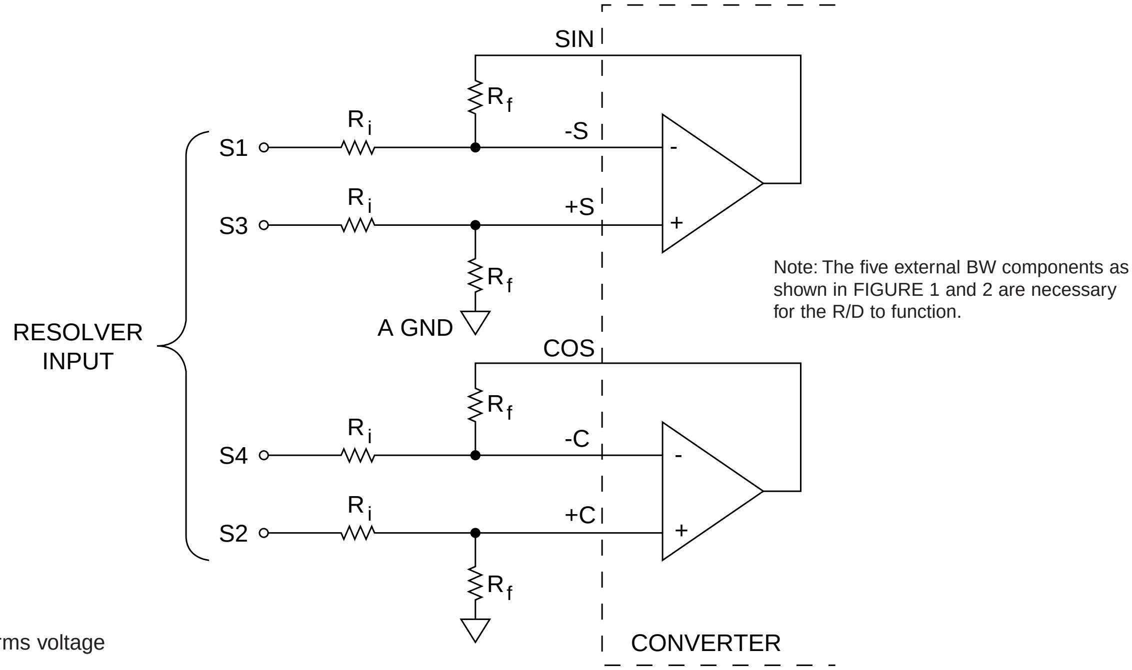
$$\frac{R2}{R1 + R2} = \frac{2}{X\ \text{Volt}}$$

R1 + R2 should not load the Resolver too much; it is recommended to use a R2 = 10k.

R1 + R2 Ratio Errors will result in Angular Errors,

2 cycle, 0.1% Ratio Error = 0.029° Peak Error.

FIGURE 7B. TYPICAL CONNECTIONS, X- VOLT RESOLVER, DIRECT INPUT

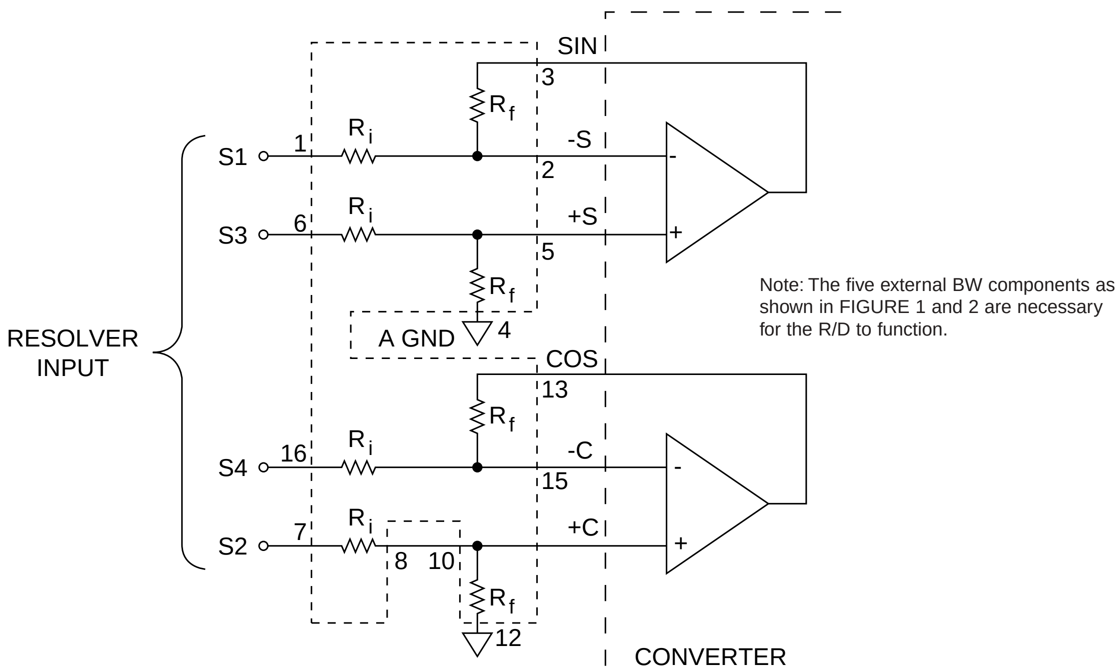


$\frac{Ri}{Rf}$ x 2 Vrms = Resolver L-L rms voltage

Rf ≥ 6 kΩ

S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.

FIGURE 8A. DIFFERENTIAL RESOLVER INPUT



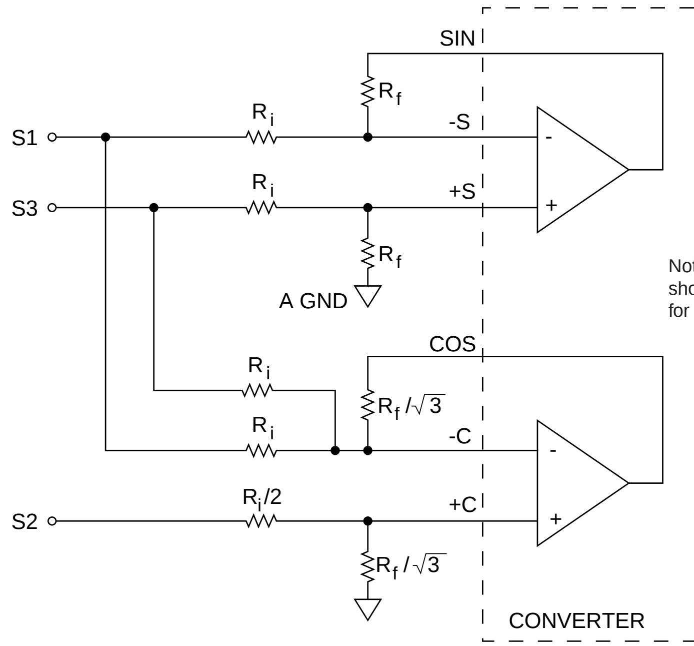
S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.

For DDC-49530 or DDC-57470: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.

For DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.

Maximum addition error is 1 minute.

FIGURE 8B. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530, DDC-57470 (11.8 V), DDC-73089 (2V), OR DDC-49590 (90 V)



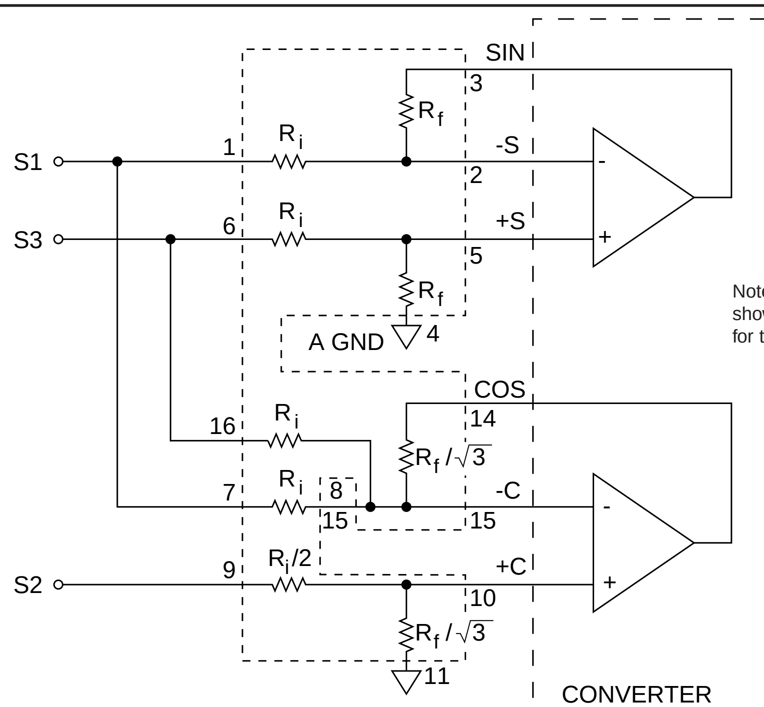
Note: The five external BW components as shown in FIGURE 1 and 2 are necessary for the R/D to function.

$\frac{Ri}{Rf}$ x 2 Vrms = Synchro L-L rms voltage

Rf ≥ 6 kΩ

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded, In both cases the shield should be tied to GND at the converter.

FIGURE 9A. SYNCHRO INPUT



Note: The five external BW components as shown in FIGURE 1 and 2 are necessary for the R/D to function.

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded, In both cases the shield should be tied to GND at the converter.

90 V input = DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.

11.8 V input = DDC-49530 or DDC-57470: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.

Maximum addition error is 1 minute.

FIGURE 9B. SYNCHRO INPUT, USING DDC-49530/DDC-57470 (11.8 V), DDC-73089 (2V) OR DDC-49590 (90 V)

The carrier frequency should be 1/10, or less, of the sampling frequency in order to have many samples per carrier cycle. The converter will work with reduced quadrature rejection at a carrier frequency up to 1/4 the sampling frequency. Carrier frequency should be at least 3.5 times the BW in order to eliminate the chance of jitter.

REDUCED POWER SUPPLY CURRENTS

When R_S = 30 kΩ (tracking rate is not being pushed), nominal power supply current can be cut from 14 to 9 mA by setting R_C = 53 kΩ.

TRANSFORMER ISOLATION

System requirements often include electrical isolation. There are transformers available for reference and synchro/resolver signal isolation. TABLE 6 includes a listing of the most common transformers. The synchro/resolver transformers reduce the voltage to 2 Vrms for a direct connection to the converter. See FIGURES 5A, 5B, 5C and 5D for transformer layouts and schematics, and FIGURE 6 for typical connections.

DC INPUTS

As noted in TABLE 1 the RDC-19220 will accept dc inputs. It is necessary to set the REF input to dc by tying +REF to +5 V and -REF to GND or -5 V. (With dc inputs, the converter will function from 0 to 180° and BIT will remain at logic 0.)

VELOCITY TRIMMING

RDC-19220 Series specifications for velocity scaling, reversal error and offset are contained in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 10 shows the setup for trimming these parameters with external pots. It should also be noted that when the resolution is changed, VEL scaling is also changed. Since the VEL output is from an integrator with capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

INCREASED TRACKING/DECREASED SETTLING (GEAR SHIFTING)

Connecting the $\overline{\text{BIT}}$ output to the resolution control lines (A and B) will change the resolution of the converter down (“gear shift”) and make the converter settle faster and track at higher rates. The converter bandwidth is independent of the resolution.

ADDITIONAL ERROR SOURCES

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. This voltage is due to capacitive or inductive coupling in the synchro or resolver signals. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given in the following formula:

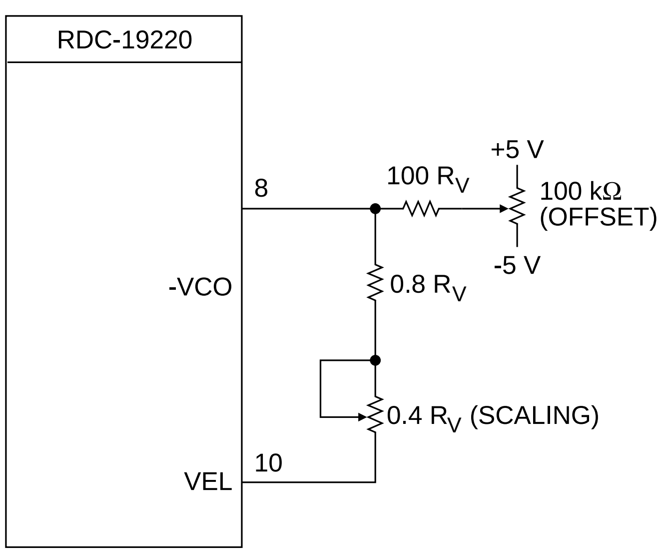
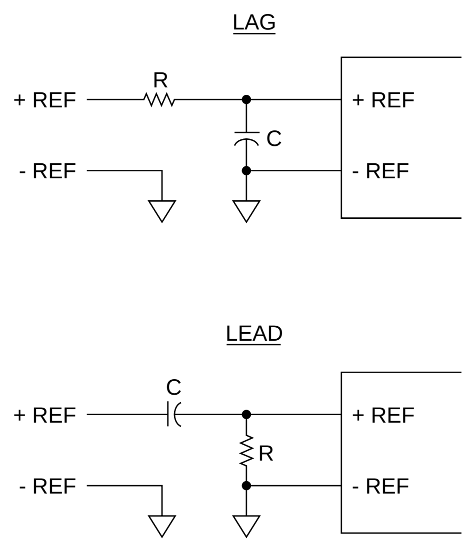


FIGURE 10. VELOCITY TRIMMING



$$\tan \varphi = \frac{X_c}{R}$$

Where φ = desired phase-shift

$$X_c = \frac{1}{2\pi fc}$$

Where f = carrier frequency
Where c = capacitance

FIGURE 11. PHASE-SHIFT COMPENSATION

Magnitude of Error = (Quadrature Voltage/F.S.signal) • tan α

Where:

Magnitude of Error is in radians
Quadrature Voltage is in volts
Full Scale signal is in volts
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8 mV
Let: F.S. signal = 11.8 V
Let: α = 6°

Then: Magnitude of Error = 0.36 min @ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier frequency) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotation speed is the rps (rotations per second) of the synchro or resolver.
Carrier frequency is the REF in Hz.

FIGURE 11 illustrates a circuit to LEAD or LAG the reference into the converter that will compensate for phase-shift between the signal and the reference to reduce the effects of the quadrature.

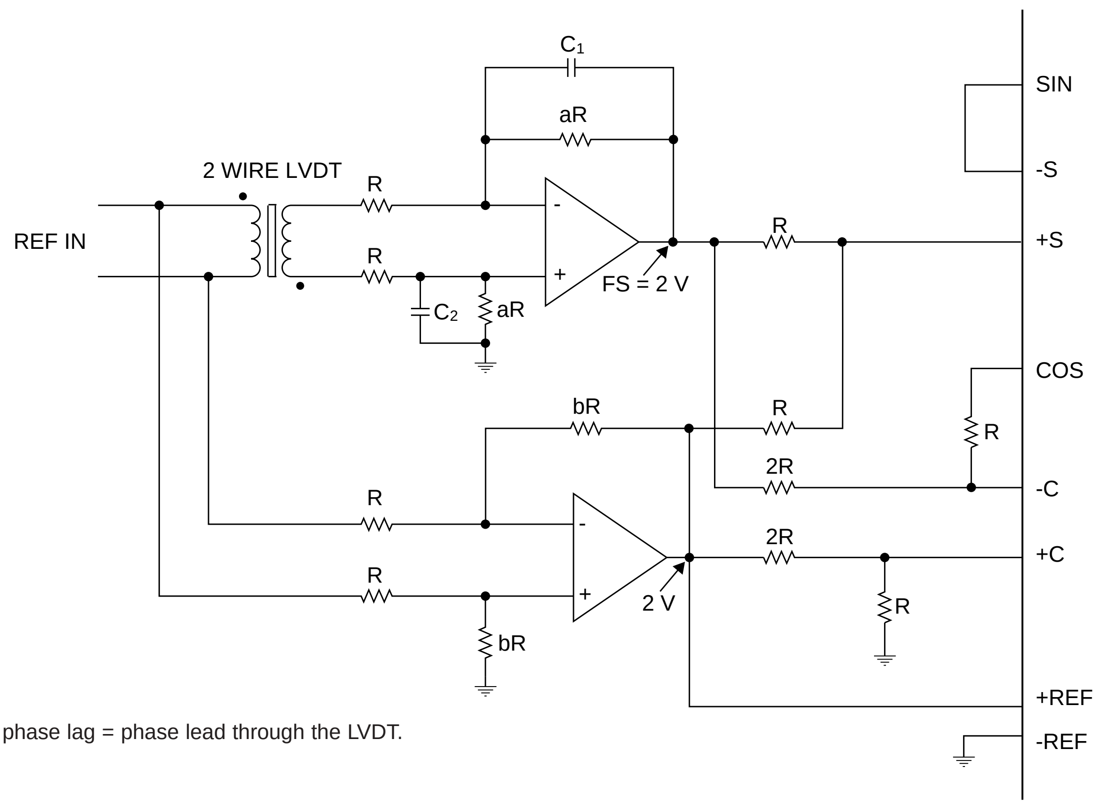
LVDT MODE

As shown in TABLE 1 the RDC-19220 Series units can be made to operate as LVDT-to-digital converters by connecting Resolution Control inputs A and B to “0,” “1,” or the -5 volt supply. In this mode the RDC-19220 Series functions as a ratiometric tracking linear converter. When linear ac inputs are applied from a LVDT the converter operates over one quarter of its range. This

TABLE 7. LVDT OUTPUT CODE (14-BIT R/D OR 12-BIT LVDT)

LVDT OUTPUT	MSB			LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx

Note: TABLE 7 refers to FIGURE 12C.



$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

FIGURE 12A. 2-WIRE LVDT DIRECT INPUT

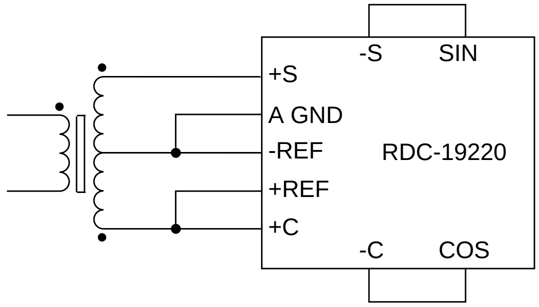
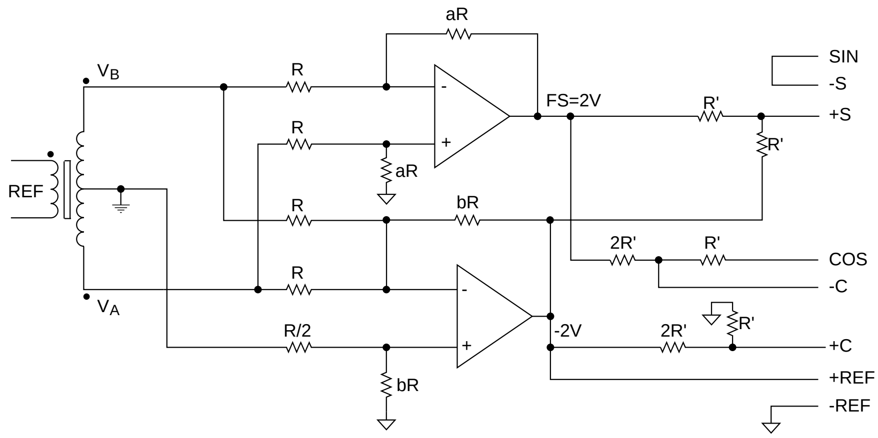
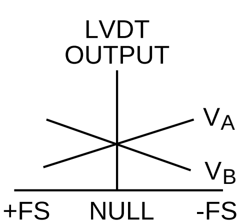


FIGURE 12B. 3-WIRE LVDT DIRECT INPUT



Notes:
1. R' ≥ 10kΩ
2. Consideration for the value of R is LVDT loading.
3. RMS values given.
4. Use the absolute values of Va and Vb when subtracting per the formula for calculating resistance values, and then use the calculated sign of "Va and Vb" for calculating SIN and COS. The calculations shown are based upon full scale travel being to the Va side of the LVDT.
5. See the RDC application manual for calculation examples.
6. Negative voltages are 180˚ phase from the reference



$$b = \frac{1}{V_{Anull}} = \frac{1}{V_{Bnull}}$$

$$a = \frac{2}{(V_A - V_B)_{max.}}$$

$$SIN = -1V + \frac{a}{2}(V_A - V_B)$$

$$COS = -1V - \frac{a}{2}(V_A - V_B)$$

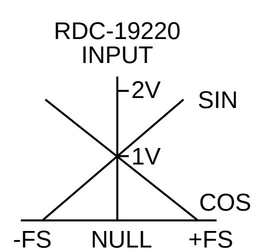


FIGURE 12C. 3-WIRE LVDT SCALING CIRCUIT

results in two less bits of resolution for LVDT mode than are provided in resolver mode.

FIGURE 12B shows a direct LVDT 2 Vrms full scale input. Some LDVT output signals will need to be scaled to be compatible with the converter input. FIGURE 12C is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant “a” is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant “b” is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op-amp, such as a 4741 type, and precision film resistors of 0.1% tolerance. FIGURE 12A illustrates a 2-wire LVDT configuration.

Data output of the RDC-19220 Series is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by **all zeros** and the most positive stroke of the LVDT is represented by **all ones**. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code “01” and negative overrange is indicated by code “11” (see TABLE 7).

INHIBIT, ENABLE, AND CB TIMING

The Inhibit ($\overline{\text{INH}}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 13, angular output data is valid 300 ns maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{\text{EM}}$) is used for the most significant 8 bits and Enable LSBs ($\overline{\text{EL}}$) is used for the least significant 8 bits. As shown in FIGURE 14, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in FIGURE 15, output data is valid 50 ns maximum after the middle of the CB pulse. CB pulse width is 1/40 Fs, which is nominally 375 ns.

Note: The converter $\overline{\text{INH}}$ may be applied regardless of the CB line state. If the CB is busy the converter $\overline{\text{INH}}$ will wait for CB to finish before setting the $\overline{\text{INH}}$ latch. Therefore, there is no need to monitor the CB line when applying an inhibit signal to the converter.

BUILT-IN-TEST ($\overline{\text{BIT}}$)

The Built-In-Test output ($\overline{\text{BIT}}$) monitors the level of error from the demodulator. This signal is the difference in the input and output angles and ideally should be zero. However, if it exceeds approximately 100 LSBs (of the selected resolution) the logic level at $\overline{\text{BIT}}$ will change from a logic 1 to a logic 0.

This condition will occur during a large step and reset after the converter settles out. $\overline{\text{BIT}}$ will also change to logic 0 for an over-velocity condition, because the converter loop cannot maintain input/output or if the converter malfunctions where it cannot

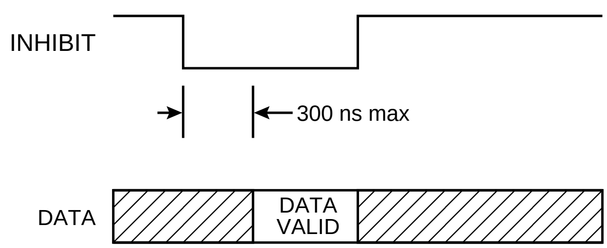


FIGURE 13. INHIBIT TIMING

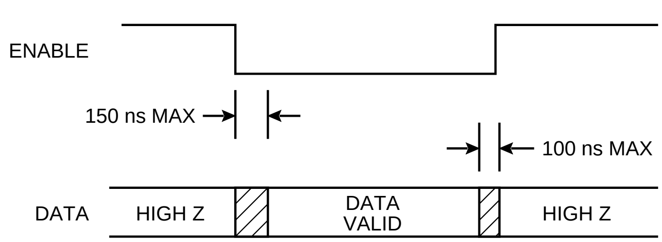


FIGURE 14. ENABLE TIMING

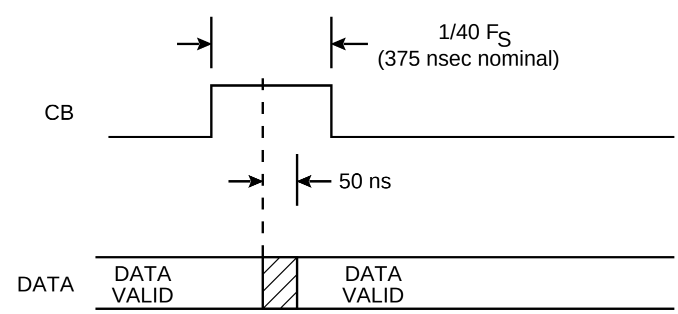


FIGURE 15. CONVERTER BUSY TIMING

maintain the loop at a null. $\overline{\text{BIT}}$ will also be set low for a detected total Loss-of-Signal (LOS). The $\overline{\text{BIT}}$ signal may pulse during certain error conditions (i.e., converter spin around or signal amplitude on threshold of LOS).

LOS will be detected if both sin and cos input voltages are less than 800 mV peak.

ENCODER EMULATION

The RDC-19220 can be made to emulate incremental optical encoder output signals, where such an interface is desired. This

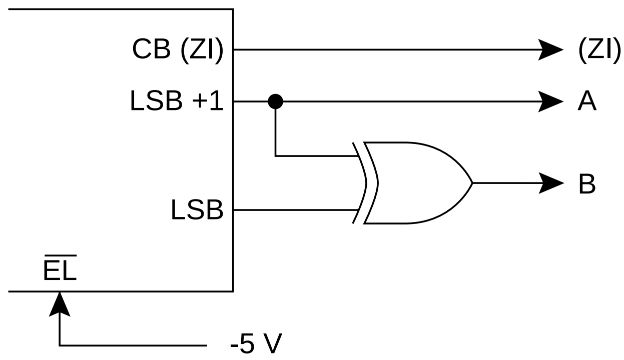
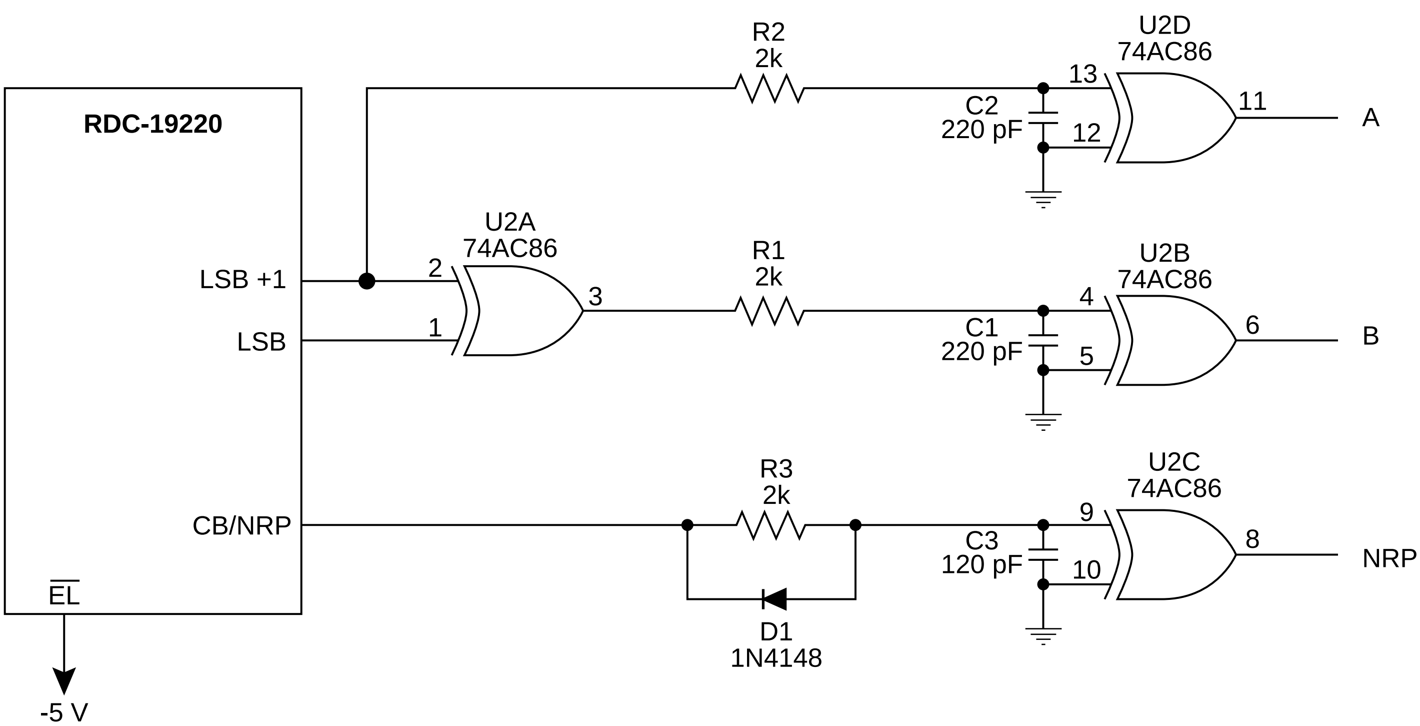


FIGURE 16A. INCREMENTAL ENCODER EMULATION



NOTE: CMOS LOGIC IS RECOMMENDED. TTL AND TTL COMPATIBLE LOGIC WILL SKEW THE DELAYS.

FIGURE 16B. FILTERED/BUFFERED ENCODER EMULATOR CIRCUIT

TYPICAL -5 VOLT CIRCUITS

Since the 40-pin DDIP RDC-19220 does not have a pinout for the -5 V inverter, it may be necessary to create a -5 V from other supplies on the board. FIGURE 17 illustrates several possibilities.

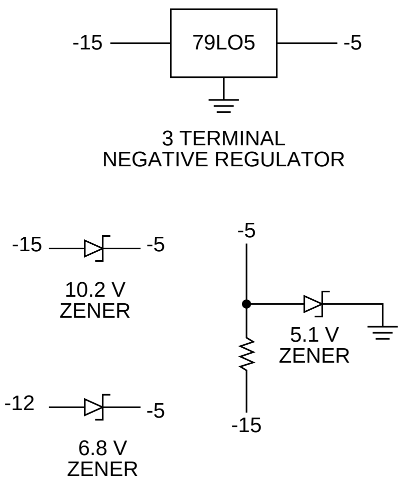


FIGURE 17. TYPICAL -5 VOLT CIRCUITS

TABLE 8. RDC-19220 PINOUTS (40-PIN)					
#	NAME	DESCRIPTION	#	NAME	DESCRIPTION
1	A	Resolution Control	40	+5 V	Power Supply
2	B	Resolution Control	39	$\overline{EL}$	Enable LSBs (see note)
3	$\overline{INH}$	Inhibit	38	Bit 16	LSB
4	+REF	+Reference Input	37	Bit 8	
5	-REF	-Reference Input	36	Bit 15	
6	-VCO	Neg VCO Input	35	Bit 7	
7	-VSUM	Vel Sum Point	34	Bit 14	
8	VEL	Velocity Output	33	Bit 6	
9	+C	Signal Input	32	Bit 13	
10	COS	Signal Output	31	Bit 5	
11	-C	Signal Input	30	Bit 12	
12	+S	Signal Input	29	Bit 4	
13	+SIN	Signal Output	28	Bit 11	
14	-S	Signal Input	27	Bit 3	
15	-5 V	Power Supply	26	Bit 10	
16	R_S	Sampling Set	25	Bit 2	
17	R_C	Current Set	24	Bit 9	
18	$\overline{EM}$	Enable MSBs	23	Bit 1	MSB
19	A GND	Analog Ground	22	CB	Converter Busy
20	GND	Ground	21	$\overline{BIT}$	Built-In-Test

PINOUT FUNCTION TABLES BY MODEL NUMBER

The TABLES 8 and 9 detail pinout functions by the DDC model number.

The RDC-19220 has differential inputs but requires both ±5 V power supplies.

The RDC-19222 has differential inputs and can be used with the +5 V only option.

TABLE 9. RDC-19222 PINOUTS (44-PIN, +5 V ONLY)			
#	NAME	#	NAME
1	$\overline{EL}$	44	Bit 16 (LSB)
2	+5 V	43	Bit 8
3	A	42	Bit 15
4	B	41	Bit 7
5	$\overline{INH}$	40	Bit 14
6	+REF	39	Bit 6
7	-REF	38	Bit 13
8	-VCO	37	Bit 5
9	-VSUM	36	Bit 12
10	VEL	35	Bit 4
11	+C	34	Bit 11
12	COS	33	Bit 3
13	-C	32	Bit 10
14	+S	31	Bit 2
15	SIN	30	Bit 9
16	-S	29	Bit 1 (MSB)
17	-5 V	28	CB
18	RS	27	$\overline{BIT}$
19	RC	26	+5C (+5 V)
20	$\overline{EM}$	25	+CAP
21	A GND	24	GND
22	-5C (-5 V)	23	-CAP

NOTES:

1. When -5 V is applied to pin 1 ($\overline{EL}$), Converter Busy (CB) becomes Zero index (ZI).

2. When using the built-in -5 V inverter: connect pin 2 to 26, pin 17 to 22, and a 10 µF/10 Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal). Connect a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

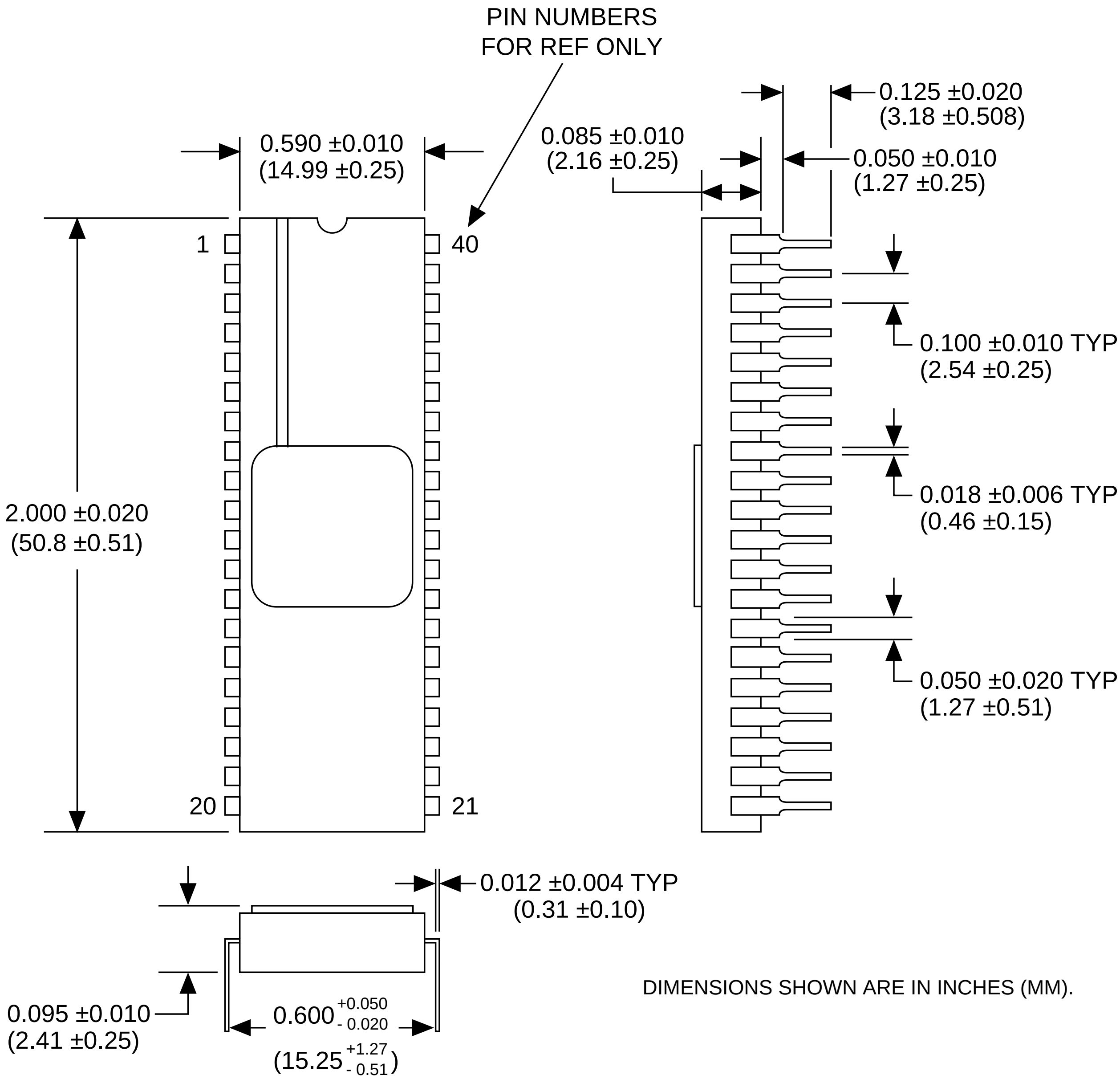


FIGURE 18. RDC-19220 (40-PIN DDIP) CERAMIC PACKAGE MECHANICAL OUTLINE

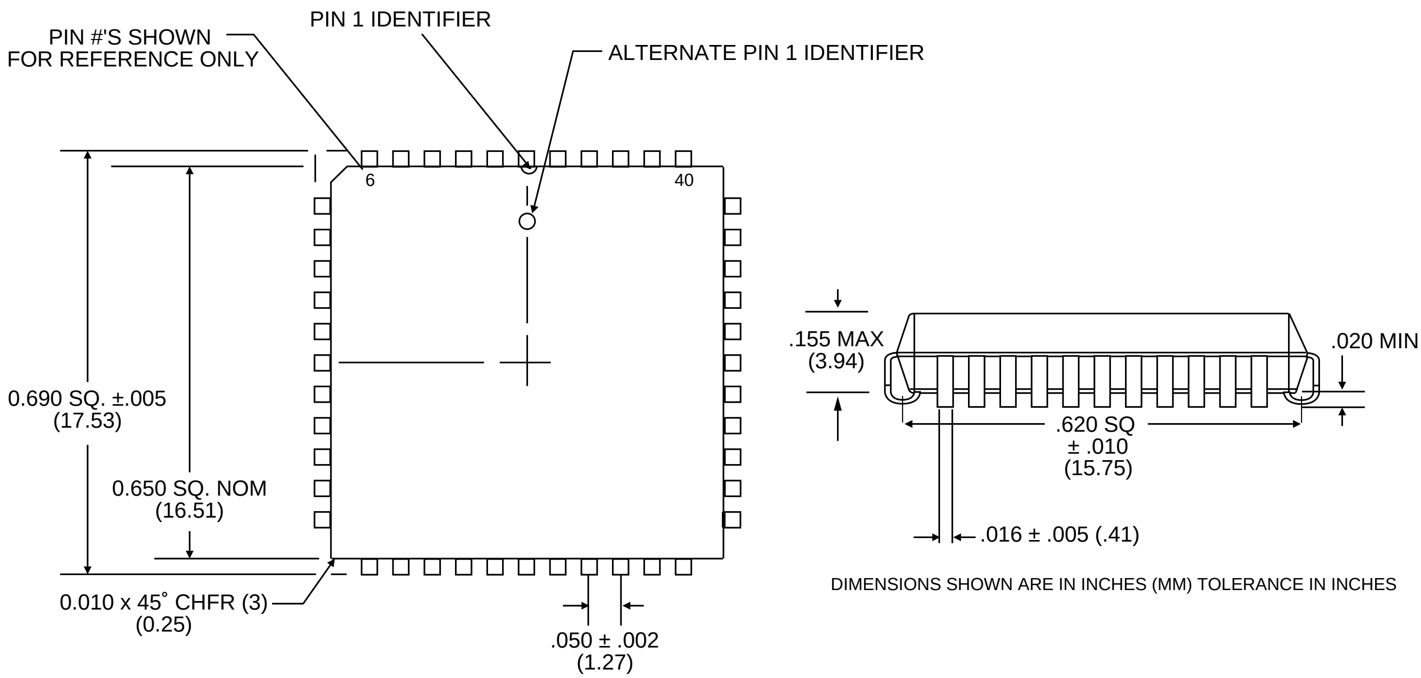


FIGURE 19. RDC-19222 (44-PIN PLASTIC J-LEAD) MECHANICAL OUTLINE

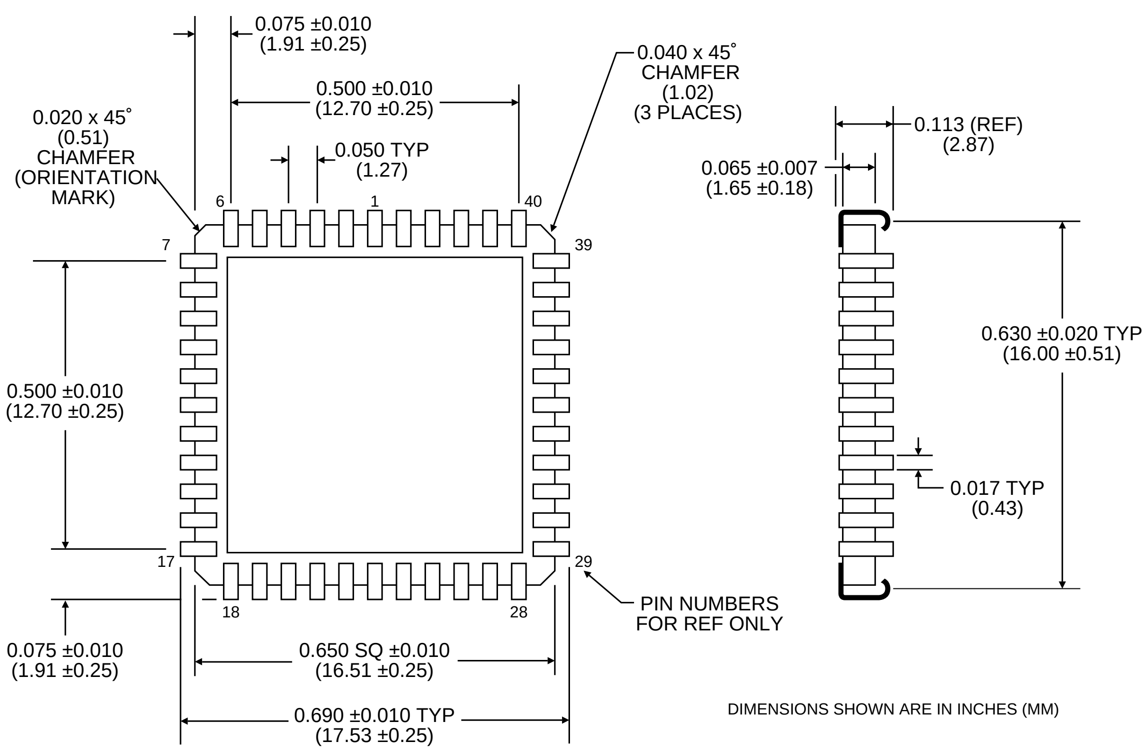


FIGURE 20. RDC-19222 (44-PIN CERAMIC J-LEAD) MECHANICAL OUTLINE

ORDERING INFORMATION

RDC-1922X - XXXX (Ceramic Package)

Supplemental Process Requirements:

T = Tape and Reel (Not available in 40-pin DDIP package)
S = Pre-Cap Source Inspection
L = 100% Pull Test
Q = Pre-Cap Source and 100% Pull Test
K = One Lot Date Code
W = One Lot Date Code and Pre-Cap Source Inspection
Y = One Lot Date Code and 100% Pull Test
Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
Blank = None of the Above

Accuracy:

3 = 2 minutes + 1 LSB

Process Requirements:

0 = Standard DDC Processing, without Burn-In
1 = MIL-PRF-38534 Compliant
2 = Standard DDC Processing, with Burn-In
3 = MIL-PRF-38534 Compliant, with PIND testing
4 = MIL-PRF-38534 Compliant, with Solder Dip
5 = MIL-PRF-38534 Compliant, with PIND testing, and Solder Dip
6 = Standard DDC Processing, with PIND testing, and Burn-In
7 = Standard DDC Processing, with Solder Dip, and Burn-In
9 = Standard DDC Processing, with Solder Dip, without Burn-In

Temperature Grade / Data Requirements:

1 = -55 to +125°C
4 = -55 to +125°C, with Variables Test Data

Package:

0 = 40-Pin DDIP, (“+5 volt only” power supply feature - not available)
2 = 44-Pin J-Lead

THIN-FILM RESISTOR NETWORKS: (Operating temperature range: -55 to +125°C)

DDC-49530 = 11.8 V input, DIP
DDC-57470 = 11.8 V input, surface mount
DDC-49590 = 90 V input, DIP
DDC-55688-1 = 2 V direct, DIP
DDC-73089 = 2 V differential, surface mount
DDC-57471 = 90 V input, surface mount

STANDARD DDC PROCESSING

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017,and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015, 1030*	Table 1

* When applicable

External Component Selection Software (refer to General Setup Conditions section) can be downloaded from DDC’s web site: www.ddc-web.com.

ORDERING INFORMATION

RDC-19222 - XXXX (Plastic Package: 44-pin J-Lead)

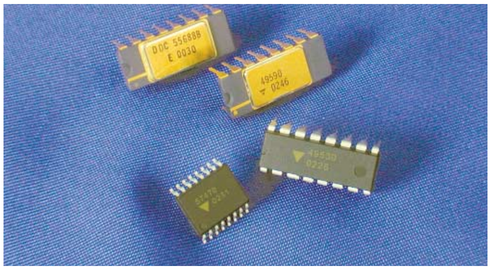
Supplemental Process Requirements:
T = Tape and Reel
Blank = None of the Above

Accuracy:
2 = 4 minutes + 1 LSB
3 = 2 minutes + 1 LSB

Process Requirements:
0 = No Burn-In
9 = Solder Dip, without Burn-In

Temperature Grade:
2 = -40 to +85°C
3 = 0 to +70°C
A = -40 to +125°C

THIN FILM RESISTOR NETWORKS FOR MOTION FEEDBACK PRODUCTS



Description

DDC converters such as the RDC-19220/2S and RD-19230 require closely matched 2Vrms Sin/Cos input voltages to minimize digital error. DDC has custom thin film resistor networks that provide the correctly matched 2Vrms converter outputs for 11.8Vrms Resolver/Synchro or 90Vrms synchro applications.

Any imbalance of the resistance ratio between the Sin/Cos inputs will create errors in the digital output. DDC's custom thin film resistor networks have very low imbalance percentages. The networks matched to 0.02%, which equates to 1LSB of error for a 16-bit application.

THIN FILM RESISTOR NETWORK	INPUT VOLTAGE (VRMS)	OUTPUT VOLTAGE (VRMS)	PACKAGE TYPE
DDC-55688-1	2 Single Ended	2	Ceramic DIP
DDC-49530	11.8	2	Plastic DIP
DDC-57470	11.8	2	Surface Mount
DDC-49590	90	2	Ceramic DIP
DDC-73089	2 Differential	2	Surface Mount
DDC-57471	90	2	Surface Mount

Note: For thin film network specifications see the "Thin Film Network Specifications for Motion Feedback Products" Data Sheet available from the DDC website.

The information in this data sheet is believed to be accurate; however, no responsibility is
assumed by Data Device Corporation for its use, and no license or rights are
granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

Please visit our web site at **www.ddc-web.com** for the latest information.

DDC®
®Data Device Corporation
105 Wilbur Place, Bohemia, New York, U.S.A. 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7382

Headquarters, N.Y., U.S.A. - Tel: (631) 567-5600, Fax: (631) 567-7358
Southeast, U.S.A. - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast, U.S.A. - Tel: (714) 895-9777, Fax: (714) 895-4988
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Ireland - Tel: +353-21-341065, Fax: +353-21-341568
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany - Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

UL® REGISTERED FIRM
DATA DEVICE CORPORATION
REGISTERED TO ISO 9001
FILE NO. A5976

PRINTED IN THE U.S.A.