MN74HC74/MN74HC74S

Dual D-Type Flip-Flop with Preset and Clear

■ Outline

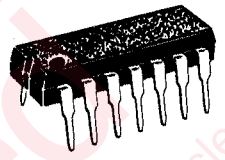
The MN74HC74/MN74HC74S consists of D-type flip-flop with preset inputs and clear inputs, and has two built-in circuits in one chip.

The respective flip-flop has independent data input, preset input, clear input, clock input, and complementary outputs Q and $\overline{Q}$. Each input data is transmitted to the output at the rise of the clock pulse. The preset input and the clear input are independent of the clock input, and their active level is "L".

Owing to the silicon gate CMOS process, these flip-flops have realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL. The outputs of the respective flip-flop can directly drive ten LS TTL inputs.

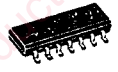
To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

P-1



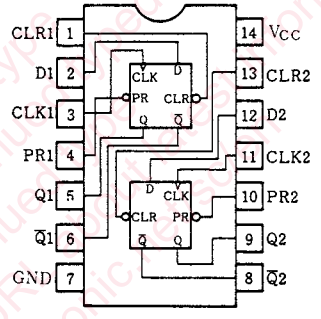
14-pin plastic DIL package

P-2



14-pin PANAFLAT package (SO-14D)

Pin Configuration

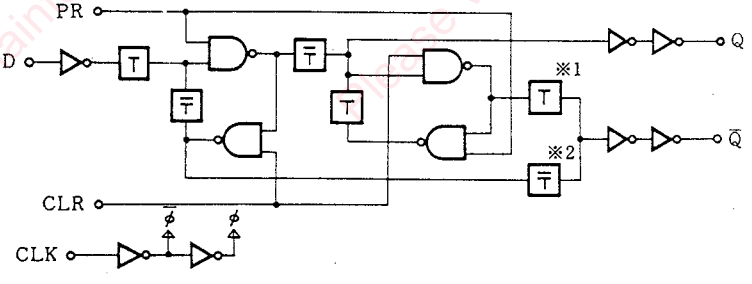


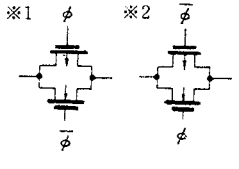
■ Truth Table

Input				Output	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	×	Q_0	$\overline{Q}_0$

Note) 1. × : "H" or "L" either will do.
2. ↗ : Leading in positive direction
3. Q_0 : Q level before input conditions in table are confirmed.
4. $\overline{Q}_0$: $\overline{Q}$ level before input conditions in table are confirmed.
5. H* : When preset, clear are "L", Q $\overline{Q}$ are H but when preset, clear are "H" simultaneously, state of Q, $\overline{Q}$ can not be predicted.

■ Logic Diagram





■ Absolute Maximum Ratings

Item			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protective diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature			T_{stg}	−65~+150	°C
Power dissipation	MN74HC74	Ta=−40~+60°C	P_D	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC74S	Ta=−40~+60°C	P_D	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item	Symbol	V_{CC}(V)	Rating	Unit
Operating power supply voltage	V_{CC}		1.4~6.0	V
Input output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature	T_A		−40~+85	°C
Input rise, fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Item	Symbol	V_{CC} (V)	Test Condition			Temperature					Unit
			V_I	V_O	Unit	Ta=25°C			Ta=−40~+85°C		
						min.	typ.	max.	min.	max.	
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4,4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.92			3.84		
		6.0		−5.2	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Static supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

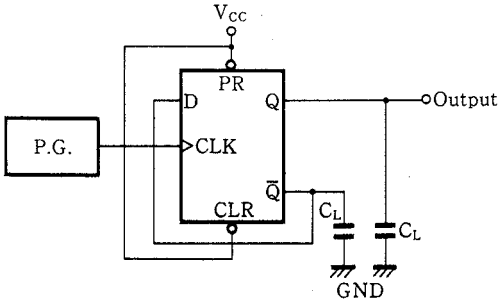
■ AC Characteristics (GND=0V, Input transition time≦6ns, C_L=50pF)

Item	Symbol	V_{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			11	26		33	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			11	26		33	
Propagation time PR, CLR→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			10	26		33	
Propagation time PR, CLR→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0			32	150		190	ns
		4.5			13	30		38	
		6.0			10	26		33	
Minimum set-up time	t_{su}	2.0			7	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
Minimum hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width PR, CLR	t_w	2.0			26	75		95	ns
		4.5			9	15		19	
		6.0			7	13		16	
Minimum recovery time PR, CLR	t_{rem}	2.0			5	75		95	ns
		4.5			4	15		19	
		6.0			2	13		16	
Maximum clock frequency	f_{max}	2.0		6	20		4		MHz
		4.5		30	58		24		
		6.0		35	70		28		

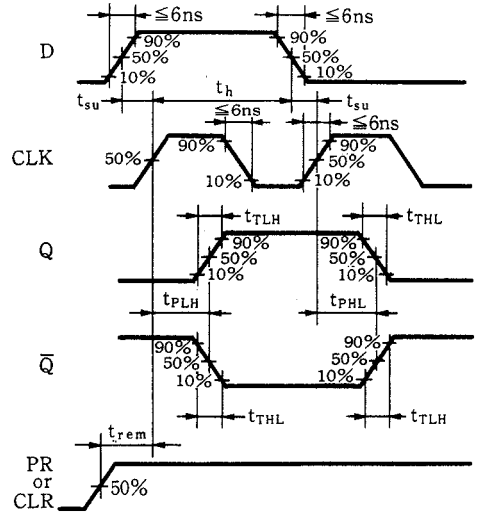
- Switching time measuring circuit and waveforms

(1) t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring circuit

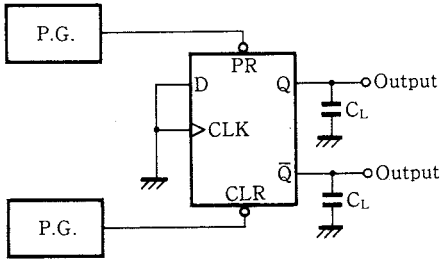


2. Switching waveforms



(2) t_{PLH}/t_{PHL} (PR, CLR→Q $\overline{Q}$), t_w (PR, CLR)

1. Measuring circuit



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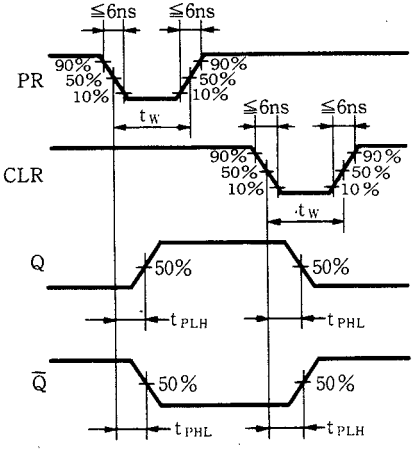

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