PRELIMINARY

256K x 1 CMOS Static RAM

FEATURES

- Fast Access Times: 25/35/45 ns
- Standard 300-Mil DIP
- Space Saving 300-Mil SOJ
- JEDEC Standard Pinout
- Separate Data Input and Output
- Low Standby Power
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Three State Output

DESCRIPTION

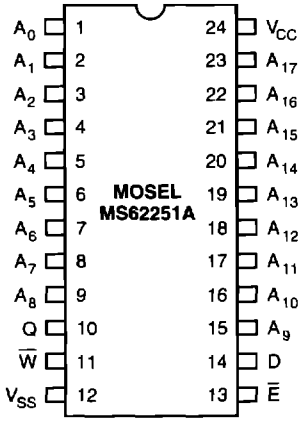
The MS62251A is a high speed 262,144 bit static RAM organized as 256K x 1. Fully static in operation, the Chip Enable ($\overline{E}$) reduces power to the chip when HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the D pin to the memory location specified by the address lines.

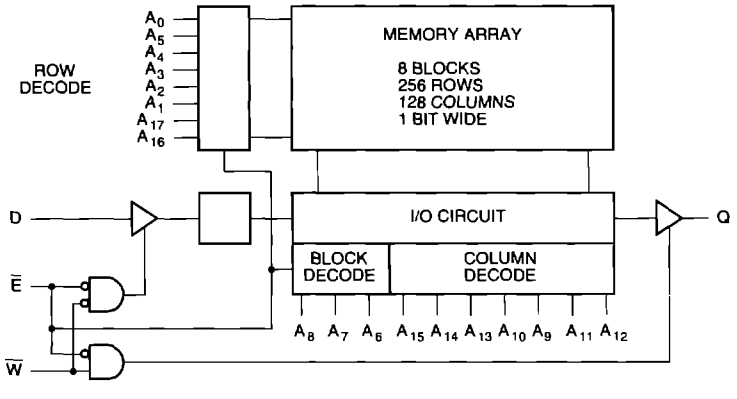
When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read of the memory location specified by the address lines will occur.

High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{17} Address Inputs

These 18 address inputs select one of the 256K x 1 bit segments in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The Q pin will be in the high-impedance state when deselected.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH, output data will be present at the Q pin; when $\overline{W}$ is LOW, the data present on the D pin will be written into the selected memory locations.

D, Q Data Input and Data Output Ports

The separate, data-in and data-out ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$	I/O OPERATION
Standby	H	X	High Z
Read	L	H	D_{OUT}
Write	L	L	D_{IN}

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

ABSOLUTE MAXIMUM RATINGS (1)

PARAMETER NAME	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-65 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	D C Output Current		±40	mA

See Notes following "AC ELECTRICAL CHARACTERISTICS"

DC ELECTRICAL CHARACTERISTICS (0°C to +70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage		4.5		5.5	V
V_{SS}	Supply Voltage		0		0	V
V_{IL}	Guaranteed Input LOW Voltage (3)		-0.5		0.8	V
V_{IH}	Guaranteed Input HIGH Voltage (1)		2 2		V_{CC} + 0.5	V
I_{CC1}	Operating Current (4)	Output open, t_{RC} = 25ns			150	mA
I_{CC1}	Operating Current (4)	Output open, t_{RC} = 35ns			120	mA
I_{CC1}	Operating Current (4)	Output open, t_{RC} = 45ns			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$-0.2V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min			5	mA
I_{LI}	Input Leakage Current	V_{in} = 0V to V_{CC}	-2		2	µA
I_{LO}	Output Leakage Current	V_{in} = 0V to V_{CC}	-10		10	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V

See Notes following "AC ELECTRICAL CHARACTERISTICS"

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

PARAMETER NAME	PARAMETER	CONDITIONS	MAX.	UNIT
C_D	Input Capacitance	V_D = 0V	5	pF
C_Q	Output Capacitance	V_Q = 0V	7	pF

1 This parameter is guaranteed and not tested

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	-25 MIN.	-25 MAX.	-35 MIN.	-35 MAX.	-45 MIN.	-45 MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [7] [8]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [7], [8]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [8]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [8]		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Timing	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		40		ns
t_{AW}	Address Valid to End of Write	20		30		40		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		30		40		ns
t_{DW}	Input Data Setup Time	13		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [7] [8]		10		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [7] [8]	0		0		0		ns

NOTES:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics

2 Output should not be shorted for more than 30 seconds

3 Negative undershoot of up to 3 0V is permitted once per cycle

4 I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times

5 *Capacitances are maximum values at 25°C measured at 1 0 MHz* with V_{Bias}=0V and V_{CC}=5 0V

6 Switching Characteristics measurements specified at "AC Test Conditions" levels

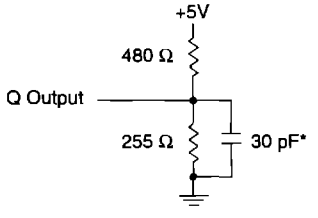
7. Active output to High-Z and High-Z to active output tests specified for a ±200mV transition from steady levels into the test load

8 Sample tested only

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load, Timing Tests	See Figure Below

AC TEST LOAD



* Includes scope and jig capacitance

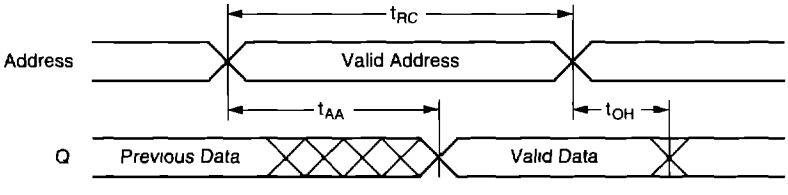
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

SWITCHING WAVEFORMS - READ CYCLE

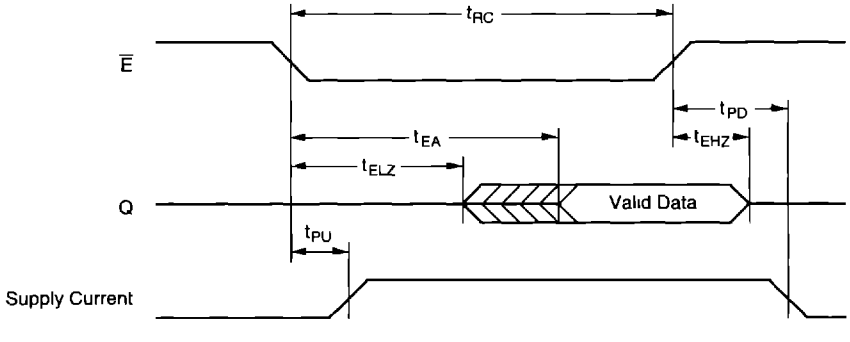
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Q implies that Data-out is in Low-Z state and the data may not be valid.



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

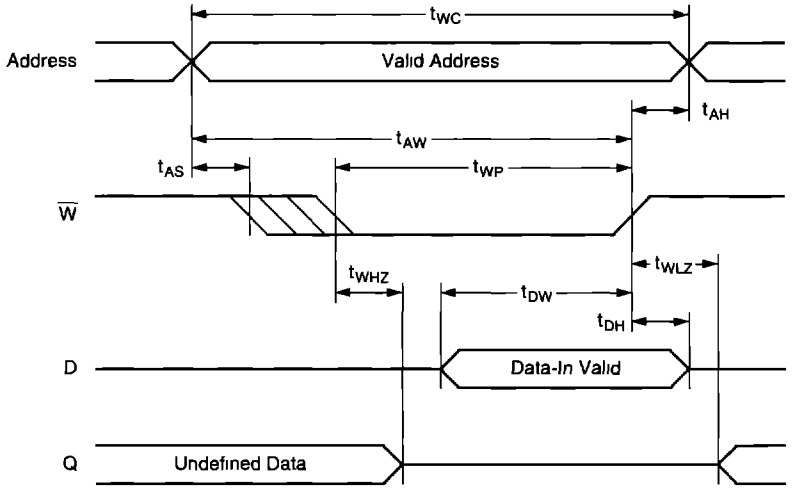


SWITCHING WAVEFORM - WRITE CYCLE

Addresses must be stable during Write Cycles. The output will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW.

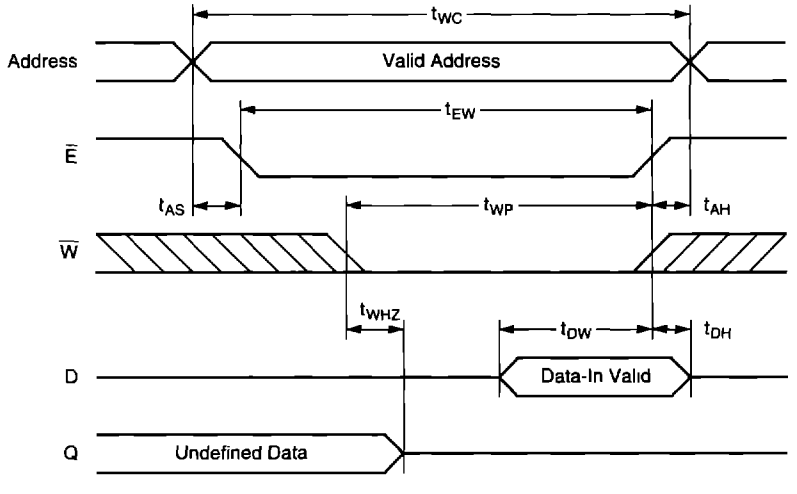
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW.



Write Cycle No. 2 ($\overline{E}$ Controlled)

Data-out may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS62251A-25NC	P24-2	0°C to +70°C
25	MS62251A-25RC	R24-1	0°C to +70°C
35	MS62251A-35NC	P24-2	0°C to +70°C
35	MS62251A-35RC	R24-1	0°C to +70°C
45	MS62251A-45NC	P24-2	0°C to +70°C
45	MS62251A-45RC	R24-1	0°C to +70°C