LXT388

Dual T1/E1/J1 Transceiver

Datasheet

The LXT388 is a dual short haul Pulse Code Modulation (PCM) transceiver for use in both 1.544 Mbps (T1) and 2.048 Mbps (E1) applications. It incorporates four receivers and two transmitters in a single LQFP-100 package.

The transmit drivers provide low impedance independent of the transmit pattern and supply voltage variations. The LXT388 transmits shaped waveforms meeting G.703 and T1.102 specifications. The LXT388 meets the latest transmit return loss specifications, such as ETSI ETS-300166.

The LXT388 differential receivers provide high noise margin for T1/E1 short-haul operation. In addition, the LXT388 includes two extra receiver/jitter attenuation blocks that can be used for Driver Performance Monitoring (DPM) in the active channels. These blocks can also be used to provide jitter attenuation in the receive and transmit paths simultaneously.

Jitter attenuation performance meets the latest international specifications such as CTR12/13. The jitter attenuator was optimized for Synchronous Optical NETwork/Synchronous Digital Hierarchy (SONET/SDH) applications including a 32/64 bit FIFO and a second order DPLL.

The LXT388 includes Intel® Hitless Protection Switching (Intel® HPS) feature which helps increase quality of service and eliminates relays in redundancy and 1+1 protection applications. Fast tristate-able drivers and a constant delay jitter attenuator are critical to achieving Intel® HPS.

Applications

- SONET/SDH tributary interfaces
- Digital cross connects
- Public/private switching trunk line interfaces
- Microwave transmission systems
- M13, E1-E3 MUX

Product Features

- Driver Performance Monitor (DPM)
- Tx and Rx Jitter Attenuator
- Single rail 3.3V supply with 5V tolerant inputs
- Superior crystal-less jitter attenuator
  - Meets ETSI CTR12/13, ITU G.736, G.742, G.823 and AT&T Pub 62411 specifications
  - Optimized for SONET/SDH applications, meets ITU G.783 mapping jitter specification
  - Constant throughput delay jitter attenuator
- Intel® HPS for 1 to 1 protection without relays
- HDB3, B8ZS, or AMI line encoder/decoder
- Analog/digital and remote loopback testing functions
- LOS per ITU G.775, ETS 300 233 and T1.231
- JTAG Boundary Scan test port per IEEE 1149.1
- 100 pin LQFP package
- Low power consumption of 150mW per channel (typical)

As of January 15, 2001, this document replaces the Level One document *LXT388 — Dual T1/E1/J1 Transceiver*.

Order Number: 249269-002
February 2001

Contents

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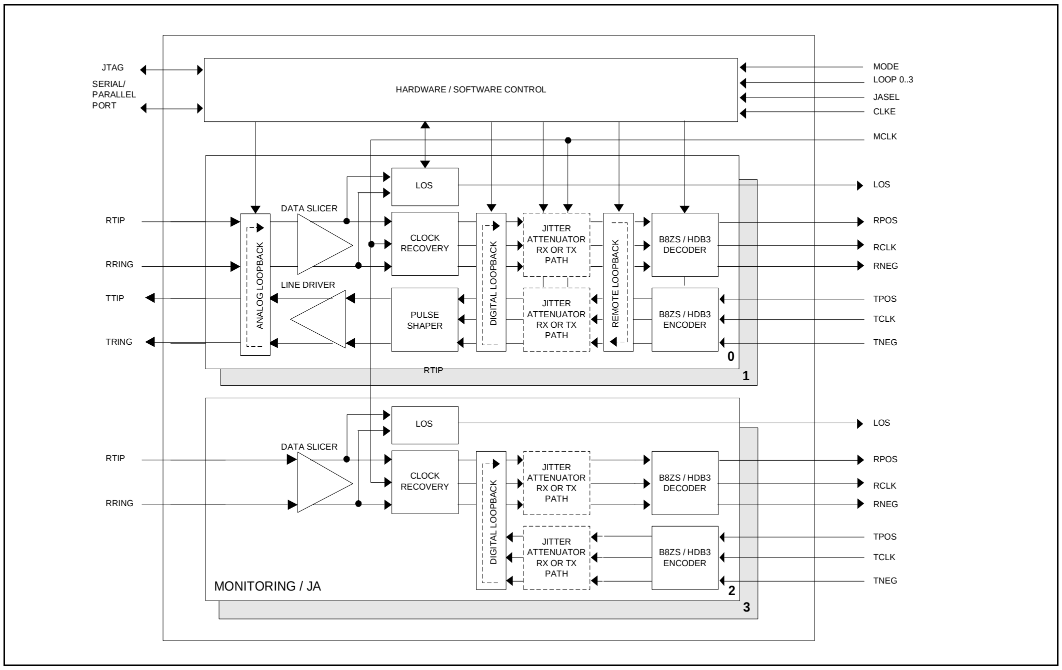
Revision History

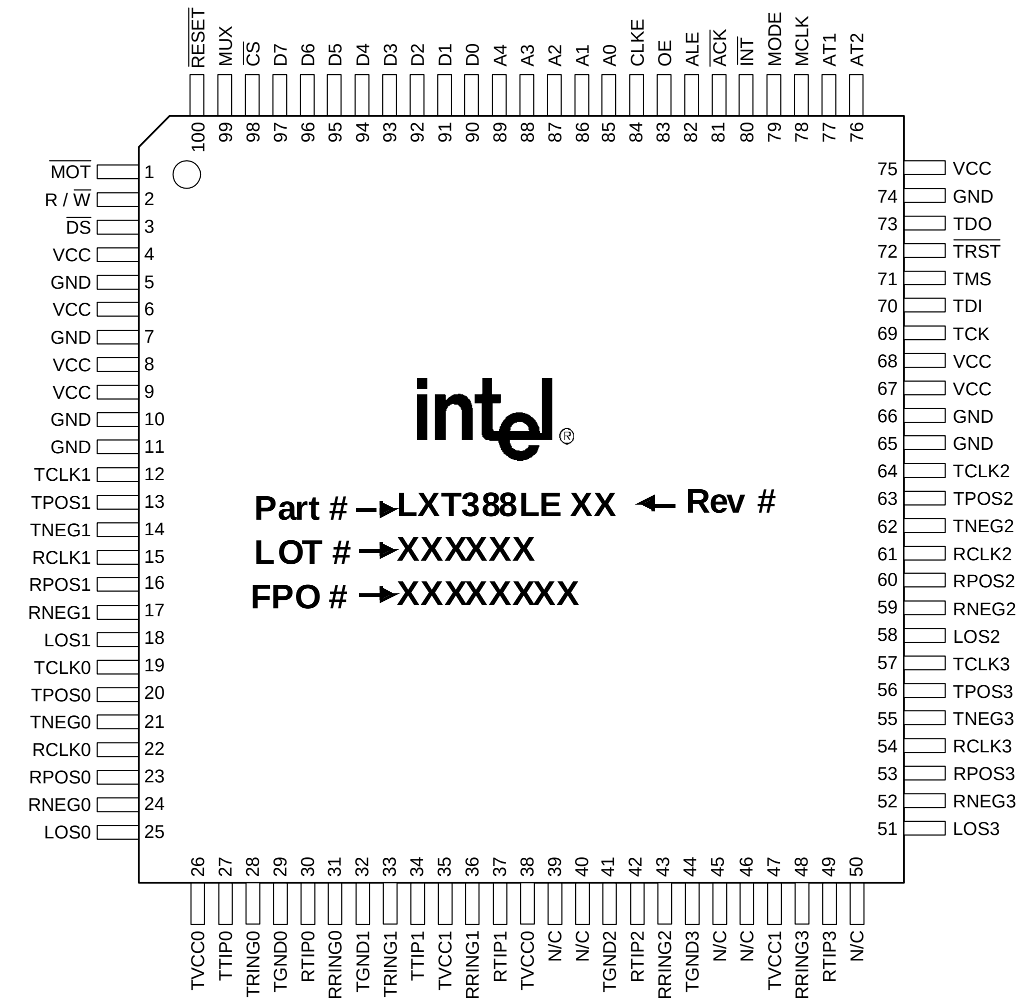
Revision	Date	Description
-002	02/12/01	Figure 2, changed pin 70 from TCK to TDI. Figure 2, changed pin 71 from GND to TCK. Moved Product Features from page 9 to page 1. Added Intel® to page 1, 3, and 35.

Figure 1. LXT388 Block Diagram



1.0 Pin Assignments and Signal Description

Figure 2. LXT388 Low-Profile Quad Flate Package (LQFP) 100 Pin Assignments and Package Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Assignments and Signal Descriptions - Power and N/C

Pin # LQFP	Symbol	I/O[1]	Description
5, 7, 10, 11, 65, 66, 74	GND	S	Power Supply Ground. Connect all pins to power supply ground.
4, 6, 8, 9, 67, 68, 75,	VCC	S	Power Supply. Connect all pins to +3.3 volt power supply
-	TVCC	S	**Transmit Driver Power Supply**. Power supply pins for the output drivers. TVCC pins can be connected to either a 3.3V or 5V power supply. Refer to "Transmitter" on page 24 for details.
26	TVCC0	S	**Transmit Driver Power Supply**. Power supply pin for the port 0 output driver. TVCC pins can be connected to either a 3.3V or 5V power supply. Refer to the Transmitter description.
29	TGND0	S	**Transmit Driver Ground**. Ground pin for the output driver.
32	TGND1	S	Transmit Driver Ground.
35	TVCC1	S	Transmit Driver Power Supply. Power supply pin for the port 1 output driver. TVCC pins can be connected to either a 3.3V or 5V power supply. Refer to the Transmitter description.
38	TVCC0	S	Transmit Driver Power Supply. Power supply pin for the port 0 output driver. TVCC pins can be connected to either a 3.3V or 5V power supply. Refer to the Transmitter description.
39 40	N/C	N/C	**Not Connected.** These pins **must** be left open for normal operation.
41	TGND2	S	**Transmit Driver Ground.**
44	TGND3	S	**Transmit Driver Ground.**
45 46	N/C	N/C	**Not Connected.** These pins **must** be left open for normal operation.
47	TVCC1	S	Transmit Driver Power Supply. Power supply pin for the port 1 output driver. TVCC pins can be connected to either a 3.3V or 5V power supply. Refer to the Transmitter description.
50	N/C	NC	**Not Connected.** These pins **must** be left open for normal operation.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 2. Pin Assignments and Signal Descriptions - Digital Interface

Pin # LQFP	Symbol	I/O[1]	Description
12	TCLK1	DI	**Transmit Clock.**
13	TPOS1/ TDATA1	DI DI	**Transmit Positive Data.** **Transmit Data.**
14	TNEG1/ UBS1	DI DI	**Transmit Negative Data.** **Unipolar/Bipolar Select.**
15	RCLK1	DO	**Receive Clock.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 2. Pin Assignments and Signal Descriptions - Digital Interface (Continued)

<table>
<tr><th>Pin #
LQFP</th><th>Symbol</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>16</td><td>RPOS1/
RDATA1</td><td>DO
DO</td><td>Receive Positive Data.
Receive Data.</td></tr>
<tr><td>17</td><td>RNEG1/
BPV1</td><td>DO
DO</td><td>Receive Negative Data.
Bipolar Violation Detect.</td></tr>
<tr><td>18</td><td>LOS1</td><td>DO</td><td>Loss of Signal.</td></tr>
<tr><td>19</td><td>TCLK0</td><td>DI</td><td>Transmit Clock. During normal operation TCLK is active, and TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is Low, the output drivers enter a low power high Z mode. If TCLK is High for more than 16 clock cycles the pulse shaping circuit is disabled and the transmit output pulse widths are determined by the TPOS and TNEG duty cycles.
<table>
<tr><th>TCLK</th><th>Operating Mode</th></tr>
<tr><td>Clocked</td><td>Normal operation</td></tr>
<tr><td>H</td><td>TAOS (if MCLK supplied)</td></tr>
<tr><td>H</td><td>Disable transmit pulse shaping (when MCLK is not available)</td></tr>
<tr><td>L</td><td>Driver outputs enter tri-state</td></tr>
</table>
When pulse shaping is disabled, it is possible to overheat and damage the LXT384 device by leaving transmit inputs high continuously. For example a programmable ASIC might leave all outputs high until it is programmed. To prevent this clock one of these signals: TPOS, TNEG, TCLK or MCLK. Another solution is to set one of these signals low: TPOS, TNEG, TCLK, or OE.
Note that the TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.</td></tr>
<tr><td>20</td><td>TPOS0/
TDATA0</td><td>DI
DI</td><td rowspan="2">Transmit Positive Data.
Transmit Data.
Transmit Negative Data.
Unipolar/Bipolar Select.
<u>Bipolar Mode</u>:
TPOS/TNEG are active high NRZ inputs. TPOS indicates the transmission of a positive pulse whereas TNEG indicates the transmission of a negative pulse.
<u>Unipolar Mode</u>:
When TNEG/UBS is pulled High for more than 16 consecutive TCLK clock cycles, unipolar I/O is selected. In unipolar mode, B8ZS/HDB3 or AMI encoding/decoding is determined by the CODEN pin (hardware mode) or by the CODEN bit in the GCR register (software mode).
TDATA is the data input in unipolar I/O mode.
<table>
<tr><th>TPOS</th><th>TNEG</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>1</td><td>0</td><td>Positive Mark</td></tr>
<tr><td>0</td><td>1</td><td>Negative Mark</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table></td></tr>
<tr><td>21</td><td>TNEG0/
UBS0</td><td>DI
DI</td></tr>
<tr><td colspan="4">1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.</td></tr>
</table>

Table 2. Pin Assignments and Signal Descriptions - Digital Interface (Continued)

Pin # LQFP	Symbol	I/O[1]	Description
22	RCLK0	DO	**Receive Clock**. Normal Mode: This pin provides the recovered clock from the signal received at RTIP and RRING. Under LOS conditions there is a transition from RCLK signal (derived from the recovered data) to MCLK signal at the RCLK output. Data Recovery Mode: If MCLK is High, the clock recovery circuit is disabled and RPOS and RNEG are internally connected to an EXOR that is fed to the RCLK output for external clock recovery applications. RCLK will be in high impedance state if the MCLK pin is Low.
23	RPOS0/ RDATA0	DO DO	**Receive Positive.** **Receive Data.** **Receive Negative Data.** **Bipolar Violation Detect.** Bipolar Mode: In clock recovery mode these pins act as active high bipolar non return to zero (NRZ) receive signal outputs. A High signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A High signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. These signals are valid on the falling or rising edges of RCLK depending on the CLKE input. In Data recovery Mode these pins act as RZ data receiver outputs. The output polarity is selectable with CLKE (Active High output polarity when CLKE is High and Active Low Polarity when CLKE is Low). RPOS and RNEG will go to the high impedance state when the MCLK pin is Low. Unipolar Mode: In uni-polar mode, the LXT388 asserts BPV High if any in-service Line Code Violation is detected. RDATA acts as the receive data output. Hardware Mode: During a LOS condition, RPOS and RNEG will remain active. Host Mode: RPOS and RNEG will either remain active or insert AIS into the receive path. Selection is determined by the RAISEN bit in the GCR register.
24	RNEG0/ BPV0	DO DO	
25	LOS0	DO	**Loss of Signal**. LOS goes High to indicate a loss of signal, i.e. when the incoming signal has no transitions for a specified time interval. The LOS condition is cleared and the output pin returns to Low when the incoming signal has sufficient number of transitions in a specified time interval. see "Loss of Signal Detector" on page 23
51	LOS3	D DO	**Loss of Signal.**
52	RNEG3/ BPV3	DO DO	**Receive Negative Data.** **Bipolar Violation Detect.**
53	RPOS3/ RDATA3	DO DO	**Receive Positive Data.** **Receive Data.**
54	RCLK3	DO	**Receive Clock.**
55	TNEG3/ UBS3	DI DI	**Transmit Negative Data.** **Unipolar/Bipolar Select.**
56	TPOS3/ TDATA3	DI DI	**Transmit Positive Data.** **Transmit Data.**
57	TCLK3	DI	**Transmit Clock.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 2. Pin Assignments and Signal Descriptions - Digital Interface (Continued)

Pin # LQFP	Symbol	I/O[1]	Description
58	LOS2	DO	**Loss of Signal.**
59	RNEG2/ BPV2	DO DO	**Receive Negative Data.** **Bipolar Violation Detect.**
60	RPOS2/ RDATA2	DO DO	**Receive Positive Data.** **Receive Data.**
61	RCLK2	DO	**Receive Clock.**
62	TNEG2/ UBS2	DI DI	**Transmit Negative Data.** **Unipolar/Bipolar Select.**
63	TPOS2/ TDATA2	DI DI	**Transmit Positive Data.** **Transmit Data.**
64	TCLK2	DI	**Transmit Clock.**
78	MCLK	DI	**Master Clock**. MCLK is an independent, free-running reference clock. It's frequency should be 1.544 MHz for T1 operation and 2.048 MHz for E1 operation. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit • Timing reference for the integrated digital jitter attenuator • Generation of RCLK signal during a loss of signal condition • Reference clock during a blue alarm transmit all ones condition • Reference timing for the parallel processor wait state generation logic If MCLK is High, the PLL clock recovery circuit is disabled. In this mode, the LXT388 operates as simple data receiver. If MCLK is Low, the complete receive path is powered down and the output pins RCLK, RPOS and RNEG are switched to Tri-state mode. MCLK is not required if LXT388 is used as a simple analog front-end without clock recovery and jitter attenuation. Note that wait state generation via RDY/$\overline{\text{ACK}}$ is not available if MCLK is not provided.
100	$\overline{\text{RESET}}$	DI	**Reset Input.** (Added in Revision B1) In either hardware mode or software mode, setting $\overline{\text{RESET}}$ low will begin to initialize the LXT388 and freeze the device until set high. One microsecond after setting $\overline{\text{RESET}}$ high, initialization will complete and the LXT388 will be ready for normal operation. Only revision B1 requires a pull up resistor to VCC at this pin between 1 and 10 kohms in value. It is necessary to retain the pull up resistor for other revisions. Please refer to the section on Reset Operation for more information.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 3. Pin Assignments and Signal Descriptions - Analog Interface

Pin # LQFP	Symbol	I/O[1]	Description
27 28	TTIP0 TRING0	AO AO	**Transmit Tip.** **Transmit Ring.** These pins are differential line driver outputs. TTIP and TRING will be in high impedance state if the TCLK pin is Low or the OE pin is Low. In software mode, TTIP and TRING can be tristated on a port-by-port basis by writing a ‘1’ to the $\overline{OEx}$ bit in the Output Enable Register (OER).
30 31	RTIP0 RRING0	AI AI	**Receive Tip.** **Receive Ring.** These pins are the inputs to the differential line receiver. Data and clock are recovered and output on the RPOS/RNEG and RCLK pins.
33 34	TRING1 TTIP1	AO AO	**Transmit Ring.** **Transmit Tip.**
36 37	RRING1 RTIP1	AI AI	**Receive Ring.** **Receive Tip.**
42 43	RTIP2 RRING2	AI AI	**Receive TIP.** **Receive Ring.**
48 49	RRING3 RTIP3	AI AI	**Receive Ring.** **Receive Tip.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 4. Pin Assignments and Signal Descriptions - JTAG Port

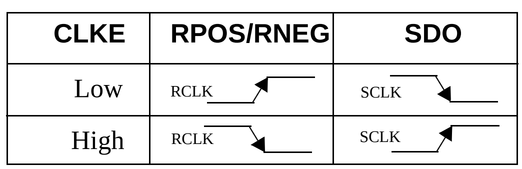
Pin # LQFP	Symbol	I/O[1]	Description
76	AT2	AO	**JTAG Analog Output Test Port 2.**
77	AT1	AI	**JTAG Analog Input Test Port 1.**
72	$\overline{TRST}$		**JTAG Controller Reset.** Input is used to reset the JTAG controller. $\overline{TRST}$ is pulled up internally and may be left disconnected.
71	TMS	DI	**JTAG Test Mode Select.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.
69	TCK	DI	**JTAG Clock.** Clock input for JTAG. Connect to GND when not used.
73	TDO	DO	**JTAG Data Output.** Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. Updated on falling edge of TCK.
70	TDI	DI	**JTAG Data Input**. Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 5. Pin Assignments and Signal Descriptions - Microprocessor/Configuration

<table>
<tr><th>Pin #
LQFP</th><th>Symbol</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>$\overline{\text{MOT}}$/INTL/
$\overline{\text{CODEN}}$</td><td>DI
DI</td><td>Motorola/Intel/Codec Enable Select.
<u>Host Mode:</u>
When Low, the host interface is configured for Motorola microcontrollers. When High, the host interface is configured for Intel microcontrollers.
<u>Hardware Mode:</u>
This pin determines the line encode/decode selection when in unipolar mode:
When Low, B8ZS/HDB3 encoders/decoders are enabled for T1/E1 respectively. When High, enables AMI encoder/decoder (transparent mode).</td></tr>
<tr><td>2</td><td>R / $\overline{\text{W}}$/
RD/
LEN1</td><td>DI
DI
DI</td><td>Read/Write (Motorola Mode).
Read Enable (Intel mode).
Line Length Equalizer (Hardware Mode).
<u>Host Mode</u>
This pin functions as the read/write signal in Motorola mode and as the Read Enable in Intel mode.
<u>Hardware Mode</u>
This pin determines the shape and amplitude of the transmit pulse. Refer to Table 6.</td></tr>
<tr><td>3</td><td>$\overline{\text{DS}}$/
$\overline{\text{WR}}$/
SDI/
LEN0</td><td>DI
DI
DI
DI</td><td>Data Strobe (Motorola Mode).
Write Enable (Intel mode).
Serial Data Input (Serial Mode).
Line Length Equalizer (Hardware Mode).
<u>Host Mode</u>
This pin acts as data strobe in Motorola mode and as Write Enable in Intel mode. In serial mode this pin is used as Serial Data Input.
<u>Hardware Mode</u>
This pin determines the shape and amplitude of the transmit pulse. Refer to Table 6.</td></tr>
<tr><td>79</td><td>MODE</td><td>DI</td><td>Mode Select. This pin is used to select the operating mode of the LXT386. In Hardware Mode, the parallel processor interface is disabled and hardwired pins are used to control configuration and report status.
In Parallel Host Mode, the parallel port interface pins are used to control configuration and report status.
In Serial Host Mode the serial interface pins: SDI, SDO, SCLK and $\overline{\text{CS}}$ are used
<table>
<tr><th>MODE</th><th>Operating Mode</th></tr>
<tr><td>L</td><td>Hardware Mode</td></tr>
<tr><td>H</td><td>Parallel Host Mode</td></tr>
<tr><td>Vcc/2</td><td>Serial Host Mode</td></tr>
</table>
For Serial Host Mode, the pin should connected to a resistive divider consisting of two 10 kΩ resistors across Vcc and Ground.</td></tr>
<tr><td>80</td><td>$\overline{\text{INT}}$</td><td>DO</td><td>Interrupt. This active Low, maskable, open drain output requires an external 10k pull up resistor. If the corresponding interrupt enable bit is enabled, $\overline{\text{INT}}$ goes Low to flag the host when the LXT388 changes state (see details in the interrupt handling section). The microprocessor INT input should be set to level triggering.</td></tr>
<tr><td colspan="4">1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.</td></tr>
</table>

Table 5. Pin Assignments and Signal Descriptions - Microprocessor/Configuration

Pin # LQFP	Symbol	I/O[1]	Description
81	$\overline{ACK}$/ RDY/ SDO	DO DO DO	**Data Transfer acknowledge** (Motorola Mode). **Ready** (Intel mode). **Serial Data Output** (Serial Mode). Motorola Mode A Low signal during a databus read operation indicates that the information is valid. A Low signal during a write operation acknowledges that a data transfer into the addressed register has been accepted (acknowledge signal).Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g. read modify write). Intel Mode A High signal acknowledges that a register access operation has been completed (Ready Signal). A Low signal on this pin signals that a data transfer operation is in progress. The pin goes tristate after completion of a bus cycle. Serial Mode If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes into high Z state during a serial port write access.
82	ALE/ SCLK/ $\overline{AS}$/ LEN2	DI DI DI DI	**Address Latch Enable** (Host Mode). **Shift Clock** (Serial Mode). **Address Strobe** (Motorola Mode). **Line Length Equalizer** (Hardware Mode). Host Mode The address on the multiplexed address/data bus is clocked into the device with the falling edge of ALE. In serial Host mode this pin acts as serial shift clock. In Motorola mode this pin acts a an active Low address strobe. Hardware Mode This pin determines the shape and amplitude of the transmit pulse in transceivers 0 and 1. It also determines the receiver setting (T1 or E1) in all the receivers. Please refer to Table 6 on page 26.
83	OE	DI	**Output Driver Enable.** If this pin is asserted Low all analog driver outputs immediately enter a high impedance mode to support redundancy applications without external mechanical relays. All other internal circuitry stays active. In software mode, TTIP and TRING can be tristated on a port-by-port basis by writing a '1' to the $\overline{OE}$x bit in the Output Enable Register (OER).
84	CLKE	DI	**Clock Edge Select.** In clock recovery mode, setting CLKE High causes RDATA or RPOS and RNEG to be valid on the falling edge of RCLK and SDO to be valid on the rising edge of SCLK. Setting CLKE Low makes RDATA or RPOS and RNEG to be valid on the rising edge of RCLK and SDO to be valid on the falling edge of SCLK. In Data recovery Mode, RDATA or RPOS/RNEG are active High output polarity when CLKE is High and active low polarity when CLKE is Low. 

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 5. Pin Assignments and Signal Descriptions - Microprocessor/Configuration

Pin # LQFP	Symbol	I/O[1]	Description
89 88 87 86 85	A4 A3 A2 A1 A0	DI DI DI DI DI	**Address Select Inputs**. Host Mode In non-multiplexed host mode, these pins function as non-multiplexed address pins. In multiplexed host mode, these pins must be connected to Ground. Hardware Mode These pins must be grounded.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 5. Pin Assignments and Signal Descriptions - Microprocessor/Configuration

<table>
<tr><th>Pin #
LQFP</th><th>Symbol</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>90
91
92
93
94
95
96
97</td><td>D0/LOOP0
D1/LOOP1
D2/LOOP2
D3/LOOP3
D4/DLOOP0
D5/DLOOP1
D6/DLOOP2
D7/DLOOP3</td><td>DI/O
DI/O
DI/O
DI/O
DI/O
DI/O
DI/O
DI/O</td><td>Loopback Mode Select/Parallel Data bus.
<u>Host Mode:</u>
When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data port.
When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 -A7.
In serial Mode, D0-7 should be grounded.
<u>Hardware Mode:</u>
In hardware mode, these pins control the operation of transceivers 0, 1 and receivers 2, 3 according to the table below.
During remote loopback mode, data on TPOS and TNEG is ignored and data received on RTIP and RRING is looped around and retransmitted on TTIP and TRING. Note: in data recovery mode, the pulse template cannot be guaranteed while in a remote loopback.
In analog local loopback mode, data received on RTIP and RRING is ignored and data transmitted on TTIP and TRING is internally looped around and routed back to the receiver inputs.
<table>
<tr><th>LOOP</th><th>DLOOP</th><th>Operating Mode
Transceivers 0,1</th><th>Operating Mode
Receivers 2, 3</th></tr>
<tr><td>Open</td><td>x</td><td>Normal Mode</td><td>Normal Mode</td></tr>
<tr><td>0</td><td>x</td><td>Remote Loopback</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>Analog Local Loopback</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>Digital Local Loopback</td><td>Digital Local Loopback</td></tr>
</table>
In digital local loopback mode, data received on TCLK/TPOS/TNEG is digitally looped back to RCLK/RPOS/RNEG.
Figure 9 through Figure 14 illustrate the different loopback modes.
Note: When these inputs are left open, they stay in a high impedance state. Therefore, the layout design should not route signals with fast transitions near the LOOP pins. This practice will minimize capacitive coupling.</td></tr>
<tr><td>99</td><td>MUX</td><td>DI</td><td>Multiplexed/Non-Multiplexed Select.
When Low the parallel host interface operates in non-multiplexed mode. When High the parallel host interface operates in multiplexed mode. In hardware mode tie this unused input low.</td></tr>
<tr><td colspan="4">1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.</td></tr>
</table>

Table 5. Pin Assignments and Signal Descriptions - Microprocessor/Configuration

Pin # LQFP	Symbol	I/O[1]	Description
98	$\overline{CS}$/ JASEL	DI DI	**Chip Select/Jitter Attenuator Select.** Host Mode This active Low input is used to access the serial/parallel interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low. Hardware Mode This input determines the Jitter Attenuator position in the data path. <table><tr><th>JASEL</th><th>JA Position</th></tr><tr><td>L</td><td>Transmit path</td></tr><tr><td>H</td><td>Receive path</td></tr><tr><td>Z</td><td>Disabled</td></tr></table>

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

2.0 Functional Description

The LXT388 is a fully integrated dual line interface unit designed for T1 1.544 Mbps and E1 2.048 Mbps short haul applications. It features two complete transceivers and two additional receiver and jitter attenuation blocks. These block allow the LXT388 to work as a quad T1/E1 receiver with jitter attenuation. Alternatively, these blocks can be used for Driver Performance Monitoring (DPM) in the transceiver channel. They can also be used for jitter attenuation in the receive and transmit paths simultaneously as discussed in “Driver Performance Monitoring” on page 29.

Each transceiver front end interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission.

The LXT388 can be controlled through hard-wired pins or by a microprocessor through a serial or parallel interface (Host mode).

The transmitter timing reference is TCLK, and the receiver reference clock is MCLK. The LXT388 is designed to operate without any reference clock when used as an analog front-end (line driver and data recovery). MCLK is mandatory if the on chip clock recovery capability is used. All four clock recovery circuits share the same reference clock defined by the MCLK input signal.

2.1 Initialization

During power up, the transceiver remains static until the power supply reaches approximately 60% of VCC. During power-up, an internal reset sets all registers to their default values and resets the status and state machines for the LOS.

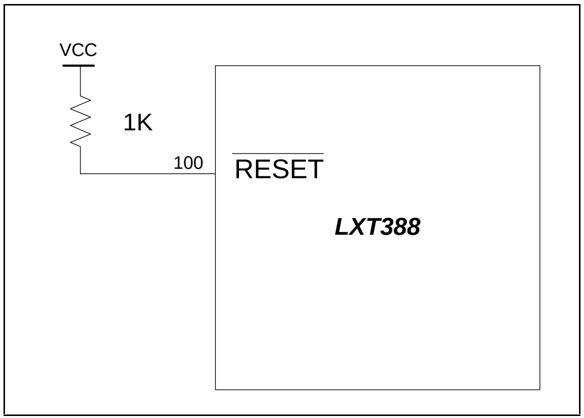
2.1.1 Reset Operation

With revision B1, no-connect pin 100 converted to the $\overline{\text{RESET}}$ pin. Only revsion B1 requires a pull up resistor to VCC at pin 100 in the LQFP package as shown in Figure 3.

There are two methods of resetting the LXT388:

1. Override Reset - Setting the $\overline{\text{RESET}}$ pin low in either hardware mode or host mode. Until the $\overline{\text{RESET}}$ pin returns high, the LXT388 remains frozen and will not function. Once the $\overline{\text{RESET}}$ pin has returned high, the LXT388 will operaate normally. Override Reset changes all the internal registers to their default values.
2. Software Reset - Writing to the RES reset register initiates a 1microsecond reset cycle, except in Intel non-multiplexed mode. In Intel non-multiplexed mode, the reset cycle takes 2 microseconds. Please refer to Host Mode section for more information. This operation changes all LXT388 registers to their default values.

Figure 3. Pullup Resistor to $\overline{\text{RESET}}$



2.2 Receiver

The four receivers in the LXT388 are identical. The following paragraphs describe the operation of one.

The twisted-pair input is received via a 1:2 step down transformer. Positive pulses are received at RTIP, negative pulses at RRING. Recovered data is output at RPOS and RNEG in the bipolar mode and at RDATA in the unipolar mode. The recovered clock is output at RCLK. RPOS/RNEG validation relative to RCLK is pin selectable using the CLKE pin.

The receive signal is processed through the peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN2-0 from 011 to 111) the threshold is set to 70% (typical) of the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LEN2-0 = 000), the threshold is set to 50% (typical).

The receiver is capable of accurately recovering signals with up to 12 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.150 V (typical) to provide immunity from impulsive noise.

After processing through the data slicers, the received signal goes to the data and timing recovery section. The data and timing recovery circuits provide an input jitter tolerance better than required by Pub 62411 and ITU G.823, as shown in Test Specifications, Figure 34.

Depending on the options selected, recovered clock and data signals may be routed through the jitter attenuator, through the B8ZS/HDB3/AMI decoder, and may be output to the framer as either bipolar or unipolar data.

2.2.1 Loss of Signal Detector

The loss of signal detector in the LXT388 uses a dedicated analog and digital loss of signal detection circuit. It is independent of its internal data slicer comparators and complies to the latest ITU G.775 and ANSI T1.231 recommendations. Under software control, the detector can be configured to comply to the ETSI ETS 300 233 specification (LACS Register). In hardware mode, the LXT388 supports LOS per G.775 for E1 and ANSI T1.231 for T1 operation.

The receiver monitor loads a digital counter at the RCLK frequency. The counter is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Depending on the operation mode, a certain number of consecutive zeros sets the LOS signal. The recovered clock is replaced by MCLK at the RCLK output. When the LOS condition is cleared, the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK. RPOS/RNEG will reflect the data content at the receiver input during the entire LOS detection period for that channel.

2.2.1.1 E1 Mode

In G.775 mode a loss of signal is detected if the signal is below 200mV (typical) for 32 consecutive pulse intervals. When the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros and the signal level exceeds 250mV (typical), the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK.

In ETSI 300 233 mode, a loss of signal is detected if the signal is below 200mV for 2048 consecutive intervals (1 ms). The LOS condition is cleared and the output pin returns to Low when the incoming signal has transitions when the signal level is equal or greater than 250mV for more than 32 consecutive pulse intervals. This mode is activated by setting the LACS register bit to one. If it is necessary to use AIS with LOS, see errata 10.3 for a way to implement this.

2.2.1.2 T1 Mode

The T1.231 LOS detection criteria is employed. LOS is detected if the signal is below 200mV for 175 contiguous pulse positions. The LOS condition is terminated upon detecting an average pulse density of 12.5% over a period of 175 contiguous pulse positions starting with the receipt of a pulse. The incoming signal is considered to have transitions when the signal level is equal or greater than 250mV.

2.2.1.3 Data Recovery Mode

In data recovery mode the LOS digital timing is derived from a internal self timed circuit. RPOS/RNEG stay active during loss of signal. The analog LOS detector complies with ITU-G.775 recommendation. The LXT388 monitors the incoming signal amplitude. Any signal below 200mV for more than 30µs (typical) will assert the corresponding LOS pin. The LOS condition is cleared when the signal amplitude rises above 250mV. The LXT388 requires more than 10 and less than 255 bit periods to declare a LOS condition in accordance to ITU G.775.

2.2.2 Alarm Indication Signal (AIS) Detection

The AIS detection is performed by the receiver independent of any loopback mode. This feature is available in host mode only. Because there is no clock in data recovery mode, AIS detection will not work in that mode. AIS requires MCLK to have clock applied, since this function depends on the clock to count the number of ones in an interval.

2.2.2.1 E1 Mode

One detection mode suitable for both ETSI and ITU is available when the LACS register bits are cleared to zero. If the LACS register bit is set to one, see errata 10.3 to implement this.

ETSI ETS300233 and G.775 detection

The AIS condition is declared when the received data stream contains less than 3 zeros within a period of 512 bits.

The AIS condition is cleared when 3 or more zeros within 512 bits are detected.

2.2.2.2 T1 Mode

ANSI T1.231 detection is employed.

The AIS condition is declared when less than 9 zeros are detected in any string of 8192 bits. This corresponds to a 99.9% ones density over a period of 5.3 ms.

The AIS condition is cleared when the received signal contains 9 or more zeros in any string of 8192 bits.

2.2.3 In Service Code Violation Monitoring

In unipolar I/O mode with HDB3/B8ZS decoding, the LXT388 reports bipolar violations on RNEG/BPV for one RCLK period for every HDB3/B8ZS code violation that is not part of the zero code substitution rules. In AMI mode, all bipolar violations (two consecutive pulses with the same polarity) are reported at the BPV output.

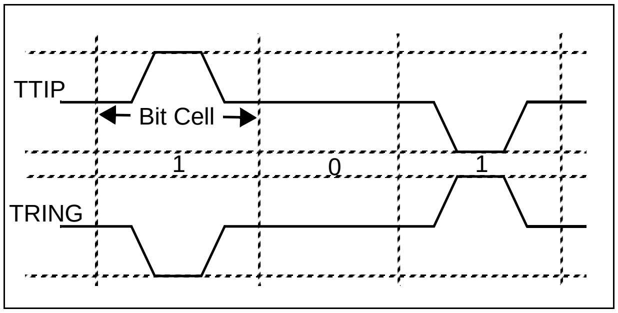
2.3 Transmitter

The two low power transmitters of the LXT388 are identical.

Transmit data is clocked serially into the device at TPOS/TNEG in the bipolar mode or at TDATA in the unipolar mode. The transmit clock (TCLK) supplies the input synchronization. Unipolar I/O and HDB3/B8ZS/AMI encoding/decoding is selected by pulling TNEG High for more than 16 consecutive TCLK clock cycles. The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. Refer to the Test Specifications Section for MCLK and TCLK timing characteristics. If TCLK is not supplied, the transmitter remains powered down and the TTIP/TRING outputs are held in a High Z state. In addition, fast output tristatability is also available through the OE pin (all ports) and/or the port's $\overline{\text{OEx}}$ bit in the Output Enable Register (OER).

Zero suppression is available only in Unipolar Mode. The two zero-suppression types are B8ZS, used in T1 environments, and HDB3, used in E1 environments. The scheme selected depends on whether the device is set for T1 or E1 operation (determined by LEN2-0 pulse shaping settings). The LXT388 also supports AMI line coding/decoding as shown in Figure 4. In Hardware mode, AMI coding/decoding is selected by the $\overline{\text{CODEN}}$ pin. In host mode, AMI coding/decoding is selected by bit 4 in the GCR (Global Control Register).

Figure 4. 50% AMI Encoding



Each output driver is supplied by a separate power supply (TVCC and TGND). The transmit pulse shaper is bypassed if no MCLK is supplied while TCLK is pulled high. In this case TPOS and TNEG control the pulse width and polarity on TTIP and TRING. With MCLK supplied and TCLK pulled high the driver enters TAOS (Transmit All Ones pattern). Note: The TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.TAOS is inhibited during Remote Loopback.

2.3.0.1 Hardware Mode

In hardware mode, pins LEN0-2 determine the pulse shaping as described in Table 6 on page 26. The LEN settings also determine whether the operating mode is T1 or E1. Note that in T1 operation mode, all four ports will share the same pulse shaping setting. Independent pulse shaping for each channel is available in host mode.

2.3.0.2 Host Mode

In Host Mode, the contents of the Pulse Shaping Data Register (PSDAT) determines the shape of pulse output at TTIP/TRING. Refer to Table 28 on page 45 and Table 29 on page 45.

2.3.1 Transmit Pulse Shaping

The transmitted pulse shape is internally generated using a high speed D/A converter. Shaped pulses are further applied to the line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance regardless of whether it is driving marks, spaces or if it is in transition. This well controlled dynamic impedance provides excellent return loss when used with external precision resistors (± 1% accuracy) in series with the transformer.

2.3.1.1 Output Driver Power Supply

The output driver power supply (TVCC pins) can be either 3.3V or 5V nominal. When TVCC=5V, LXT388 drives both E1 (75Ω/120Ω) and T1 100Ω lines through a 1:2 transformer and 11Ω/9.1Ω series resistors.

When TVCC=3.3V, the LXT388 drives E1 (75Ω/120Ω) lines through a 1:2 transformer and 11Ω series resistor. A configuration with a 1:2 transformer and without series resistors should be used to drive T1 100Ω lines.

Table 6. Line Length Equalizer Inputs

LEN2	LEN1	LEN0	Line Length[1]	Cable Loss[2]	Operation Mode
0	1	1	0 - 133 ft. ABAM	0.6 dB	T1
1	0	0	133 - 266 ft. ABAM	1.2 dB	T1
1	0	1	266 - 399 ft. ABAM	1.8 dB	T1
1	1	0	399 - 533 ft. ABAM	2.4 dB	T1
1	1	1	533 - 655 ft. ABAM	3.0 dB	T1
0	0	0	E1 G.703, 75Ω coaxial cable and 120Ω twisted pair cable.		E1

1. Line length from LXT388 to DSX-1 cross-connect point.
2. Maximum cable loss at 772KHz.

Removing the series resistors for T1 applications with TVCC=3.3V, improves the power consumption of the device. See Table 40 on page 55.

Series resistors in the transmit configuration improve the transmit return loss performance. Good transmit return loss performance minimizes reflections in harsh cable environments. In addition, series resistors provide protection against surges coupled to the device. The resistors should be used in systems requiring protection switching without external relays. Please refer to Figure 5 on page 28 for the recommended external line circuitry.

2.3.1.2 Power Sequencing

For the LXT384, we recommend sequencing TVCC first then VCC second or at the same time as TVCC to prevent excessive current draw.

2.4 Line Protection

Figure 5 on page 28 shows recommended line interface circuitry. In the receive side, the 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (70 kΩ typical) the resistors do not affect the receiver sensitivity. In the transmit side, the Schottky diodes D1-D4 protect the output driver.While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

2.5 Driver Failure Monitor

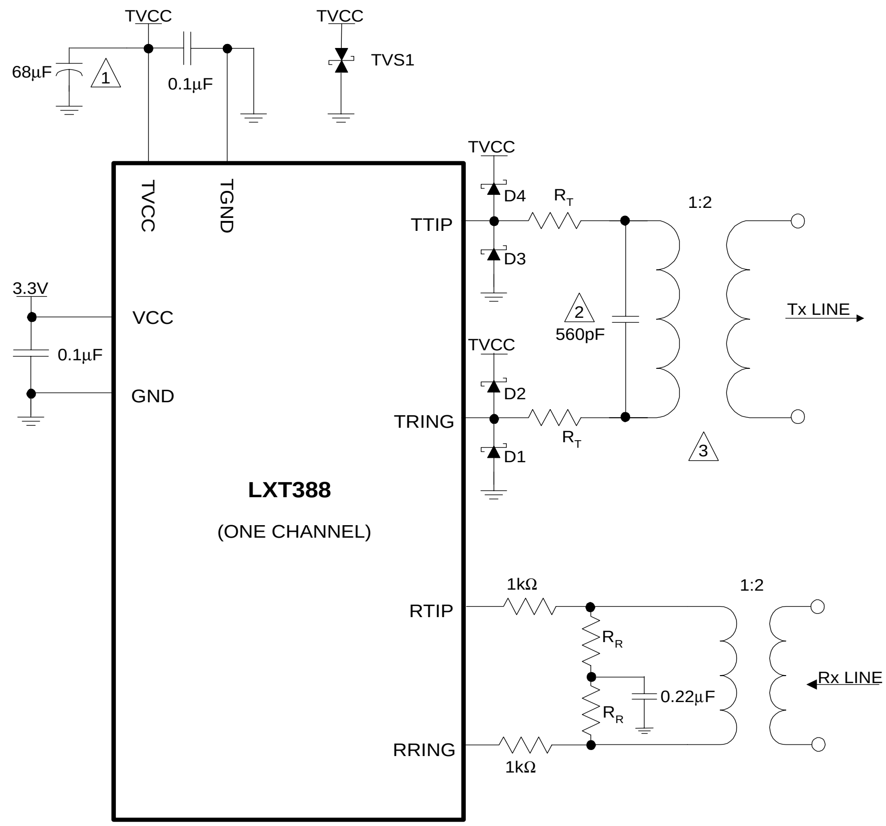
The LXT388 transceiver incorporates a internal power Driver Failure Monitor (DFM) in parallel with TTIP and TRING that is capable of detecting secondary shorts without cable. DFM is available only in configurations with no transmit series resistors (T1 mode with TVCC=3.3V). This feature is available in the serial and parallel host modes but not available in the hardware mode of operation.

A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current, is used to detect a secondary short failure. Secondary shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver short circuit fail (DFM) is reported in the respective register by setting an interrupt. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Note: Unterminated lines of adequate length ($\lambda/4$) may effectively behave as short-circuits as seen by the driver and therefore trigger the DFM. Under these circumstances, the alarm should be disabled.

In addition, the LXT388 features output driver short-circuit protection. When the output current exceeds 100 mA, LXT388 limits the driver's output voltage to avoid damage.

Figure 5. External Transmit/Receive Line Circuitry

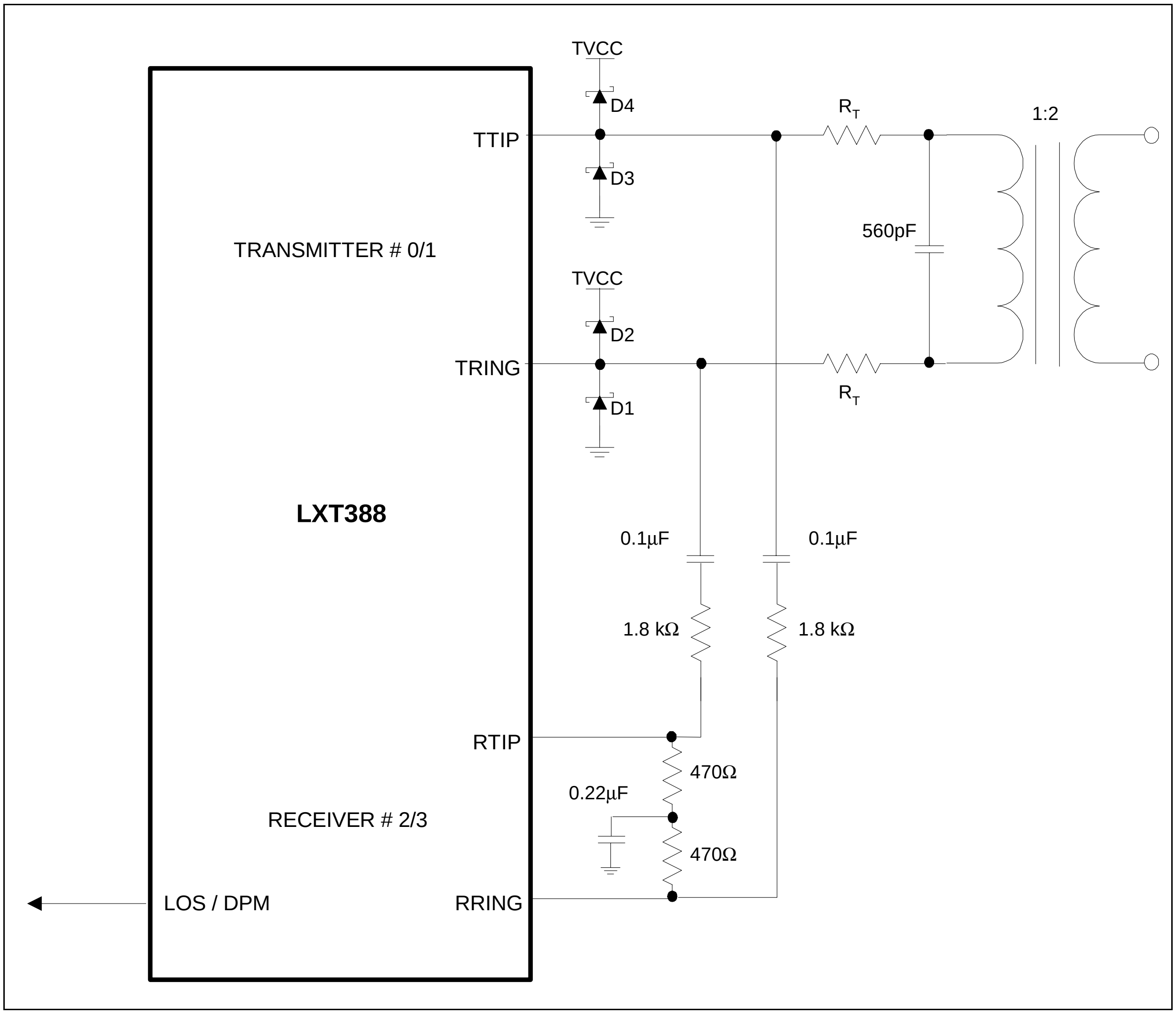


1 Common decoupling capacitor for all TVCC and TGND pins.

2 Typical value. Adjust for actual board parasitics to obtain optimum return loss.

3 Refer to Transformer Specifications Table for transformer specifications.

Figure 6. Driver Performance Monitoring



2.6 Driver Performance Monitor

The two additional receiver blocks in the LXT388 can be used to monitor the transmitter performance in channels 0 and 1 as illustrated in Figure 6.

The transmitter outputs in channels 0 and 1 are connected to receivers 2 and 3 through capacitive coupling. If the output driver stops transmitting data, the LOS output in the monitoring receiver will be asserted indicating a driver failure. Therefore, the LOS output effectively acts as a driver performance monitor indicator (DPM). This alarm is also available in host mode through the LOS registers.

The DPM set and reset operation is identical to the LOS set and reset operation as described in "Loss of Signal Detector" on page 23.

Note: T1/E1 receiver operation in channels 2 and 3 is determined by the LEN settings as described in Table 6 on page 26.

2.7 Jitter Attenuation

A digital Jitter Attenuation Loop (JAL) combined with a FIFO provides Jitter attenuation. The JAL is internal and requires no external crystal nor high-frequency (higher than line rate) reference clock.

The FIFO is a 32 x 2-bit or 64 x 2-bit register (selected by the FIFO64 bit in the GCR). Data is clocked into the FIFO with the associated clock signal (TCLK or RCLK), and clocked out of the FIFO with the dejittered JAL clock. See Figure 7. When the FIFO is within two bits of overflowing or underflowing, the FIFO adjusts the output clock by 1/8 of a bit period. The Jitter Attenuator produces a control delay of 17 or 33 bits in the associated path (refer to test specifications). This feature is required for hitless switching applications. This advanced digital jitter attenuator meets latest jitter attenuation specifications. See Table 7.

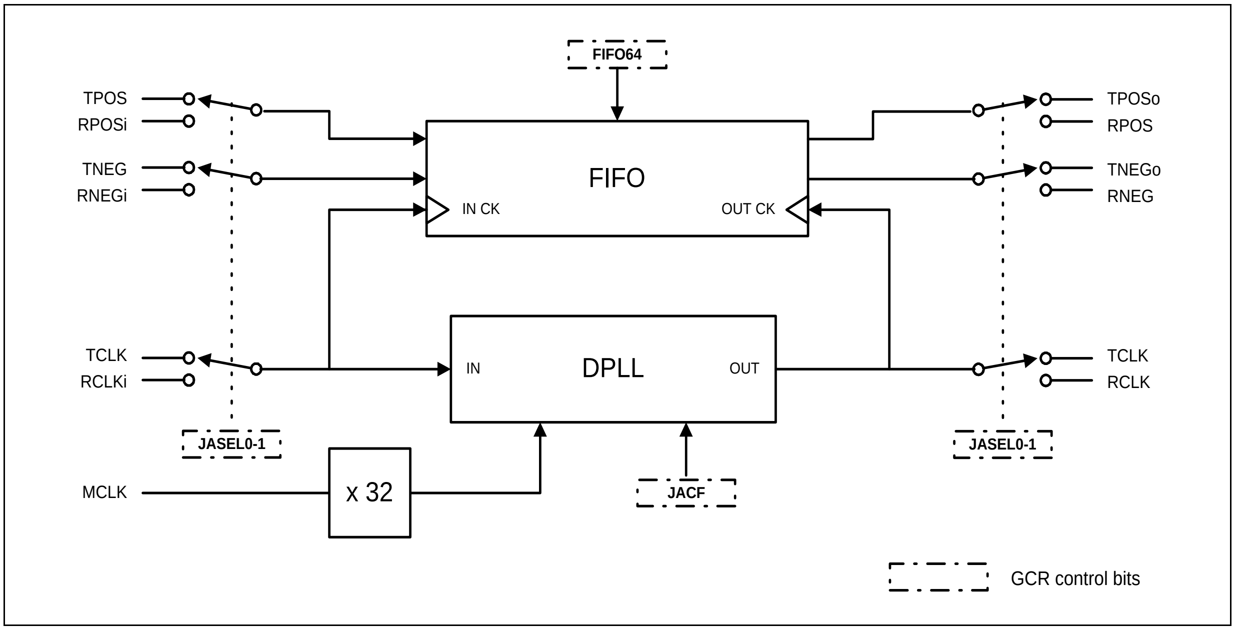
Under software control, the low limit jitter attenuator corner frequency depends on FIFO length and the JACF bit setting (this bit is in the GCR register). In Hardware Mode, the FIFO length is fixed to 64 bits. The corner frequency is fixed to 6 Hz for T1 mode and 3.5 Hz for E1 mode.

Table 7. Jitter Attenuation Specifications

T1	E1
AT&T Pub 62411	ITU-T G.736
GR-253-CORE[1]	ITU-T G.742[3]
TR-TSY-000009[2]	ITU-T G.783[4]
	ETSI CTR12/13
	BAPT 220

1. Category I, R5-203.
2. Section 4.6.3.
3. Section 6.2 When used with the SXT6234 E2-E1 mux/demux.
4. Section 6.2.3.3 combined jitter when used with the SXT6251 21E1 mapper.

Figure 7. Jitter Attenuator Loop

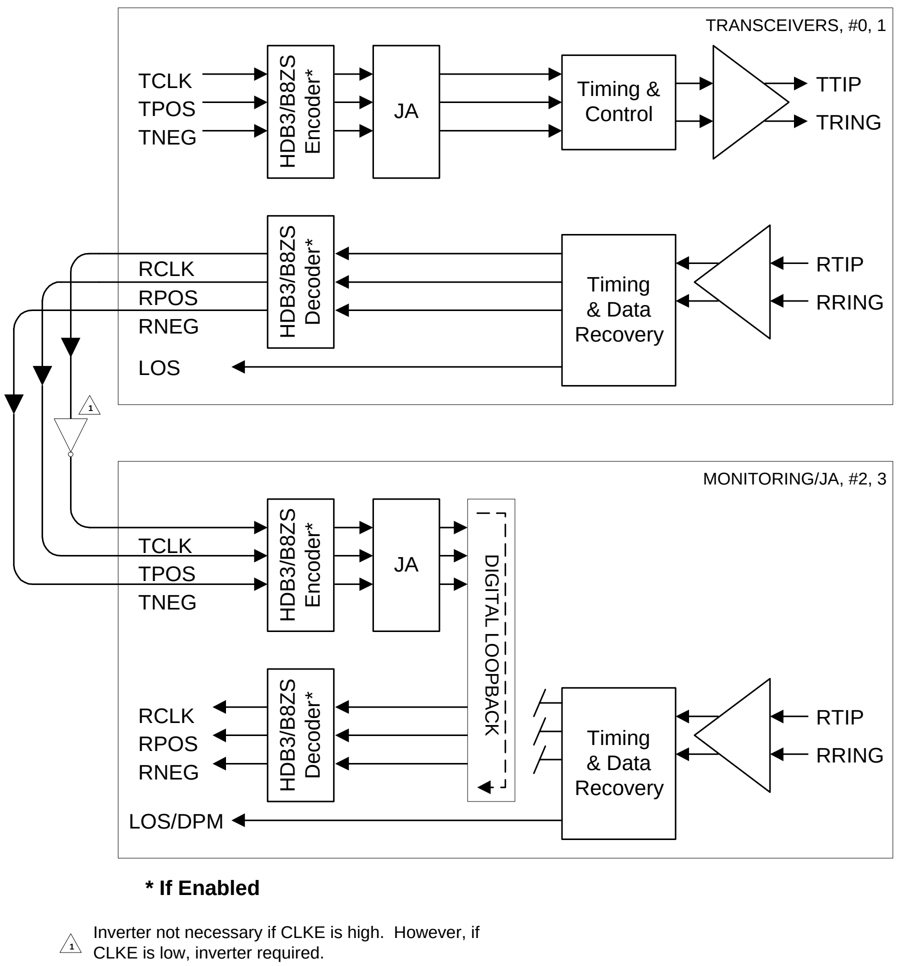


In Host Mode, the Global Control Register (GCR) determines whether the JAL is positioned in the receive path, transmit path or disabled. In Hardware Mode, the JAL position is determined by the JASEL pin.

2.7.1 Transmit and Receive Jitter Attenuation

Simultaneous transmit and receive jitter attenuation can be implemented using the additional jitter attenuators in the receiver/JA blocks 2 and 3. Please refer to Figure 8. In this example, the jitter attenuator in channels 0 and 1 is placed in the transmit path. Receive path jitter attenuation is obtained by routing the corresponding RCLK/RPOS/RNEG signals through the JAs in blocks 2 and 3. This is accomplished by enabling a digital loopback in these channels. Note that the CLKE pin should be tied High to allow direct connection between RCLK/RPOS/RNEG and TCLK/TPOS/TNEG. Connections in Figure 8 are shown for bipolar mode operation. In unipolar mode (TNEG=High), RCLK and RDATA should be connected to TCLK and TDATA. Bipolar violations for channels 0 and 1 will be reported at the BPV (RNEG) outputs in those channels.

Figure 8. Transmit and Receive Jitter Attenuation



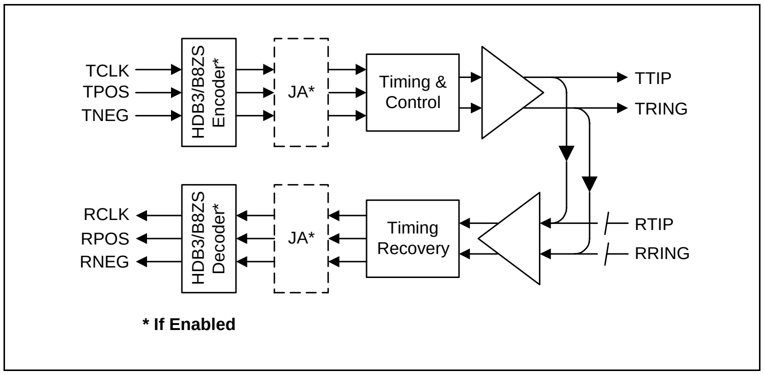
2.8 Loopbacks

The LXT388 offers three loopback modes for diagnostic purposes. In hardware mode, the loopback mode is selected with the LOOPn pins. In software mode, the ALOOP, DLOOP and RLOOP registers are employed.

2.8.1 Analog Loopback

When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP & RRING) as shown in Figure 9. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding transceiver. Note that signals on the RTIP & RRING pins are ignored during analog loopback.

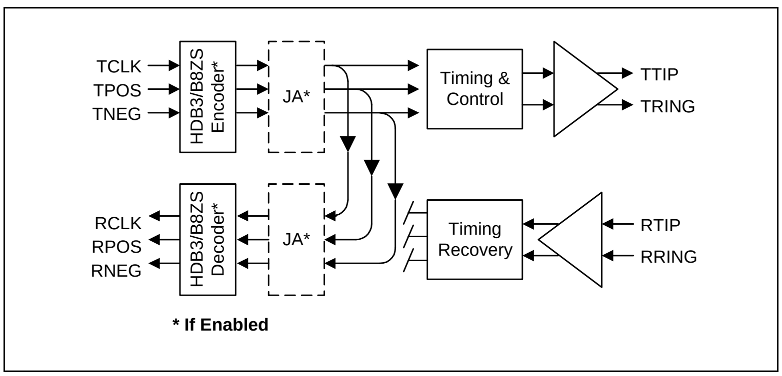
Figure 9. Analog Loopback



2.8.2 Digital Loopback

The digital loopback function is available in software and Hardware mode. When selected, the transmit clock and data inputs (TCLK, TPOS & TNEG) are looped back and output on the RCLK, RPOS & RNEG pins (Figure 10). The data presented on TCLK, TPOS & TNEG is also output on the TTIP & TRING pins. Note that signals on the RTIP & RRING pins are ignored during digital loopback.

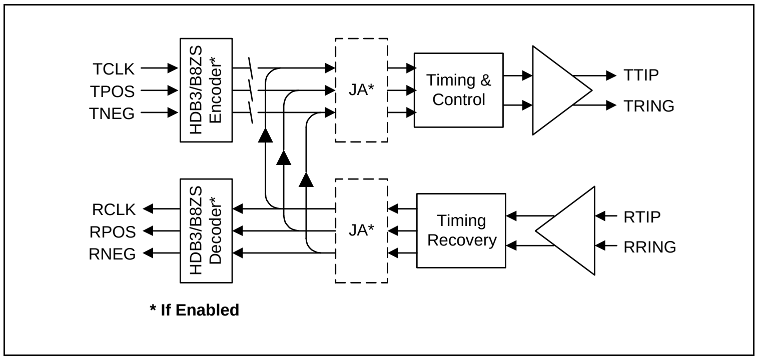
Figure 10. Digital Loopback



2.8.3 Remote Loopback

During remote loopback (Figure 11) the RCLK, RPOS & RNEG outputs routed to the transmit circuits and output on the TTIP & TRING pins. Note that input signals on the TCLK, TPOS & TNEG pins are ignored during remote loopback.

Figure 11. Remote Loopback



Note: In data recovery mode, the pulse template cannot be guaranteed while in a remote loopback.

2.8.4 Transmit All Ones (TAOS)

In Hardware mode, the TAOS mode is set by pulling TCLK High for more than 16 MCLK cycles. In software mode, TAOS mode is set by asserting the corresponding bit in the TAOS Register. In addition, automatic ATS insertion (in case of LOS) may be set using the ATS Register. Note that the TAOS generator uses MCLK as a timing reference, therefore TAOS doesn't work in data recovery mode. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability. DLOOP does not function with TOAS active.

Figure 12. TAOS Data Path

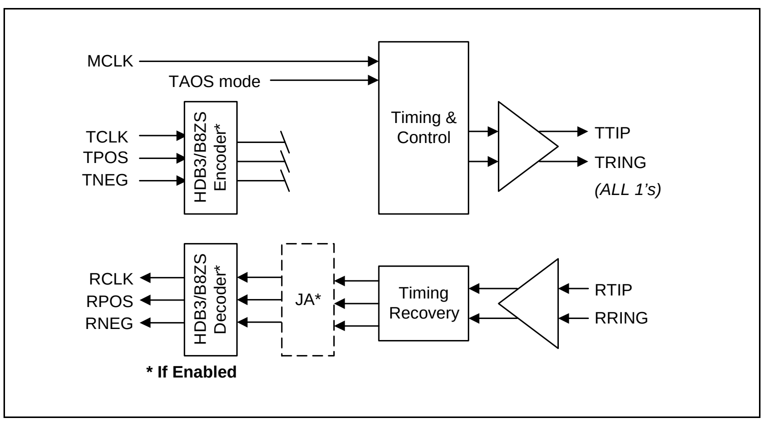


Figure 13. TAOS with Digital Loopback

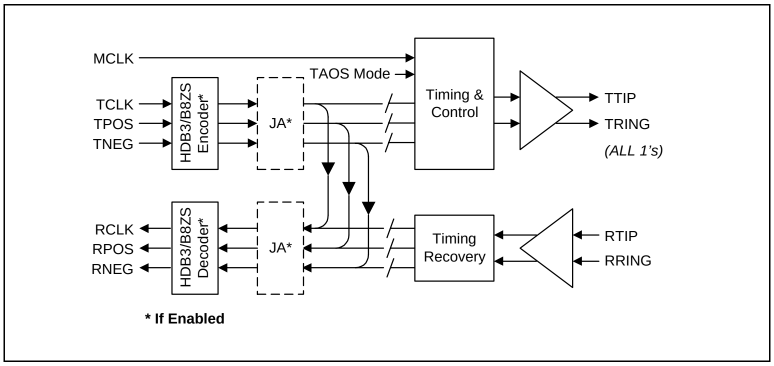
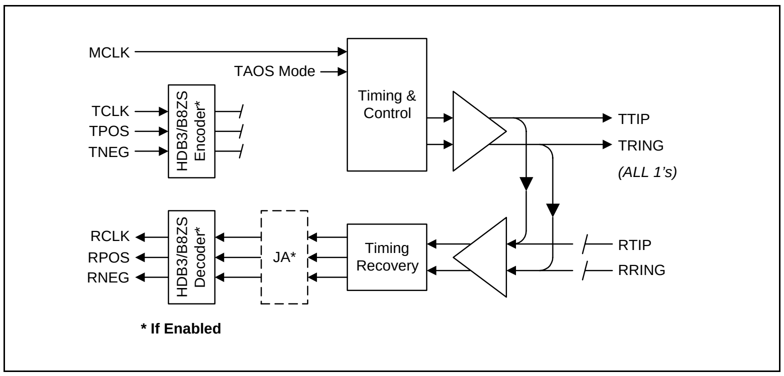


Figure 14. TAOS with Analog Loopback



2.9 Intel® Hitless Protection Switching (Intel® HPS)

The LXT388 transceivers include an output driver tristatability feature for T1/E1/J1 redundancy applications. This feature greatly reduces the cost of implementing redundancy protection by eliminating external relays. Please refer to Application Note 249134 “LXT380/1/4/6/8 Redundancy Applications” for guidelines on implementing redundancy systems for both T1/E1/J1 operation using the LXT380/1/4/6/8.

2.10 Operation Mode Summary

Table 8 lists summarizes all LXT388 hardware settings and corresponding operating modes.

Table 8. Operation Mode Summary

MCLK	TCLK	LOOP[1]	Receive Mode	Transmit Mode	Loopback
Clocked	Clocked	Open	Data/Clock recovery	Pulse Shaping ON	No Loopback
Clocked	Clocked	L	Data/Clock recovery	Pulse Shaping ON	Remote Loopback
Clocked	Clocked	H	Data/Clock recovery	Pulse Shaping ON	Analog Loopback

1. Hardware mode only.

Table 8. Operation Mode Summary (Continued)

MCLK	TCLK	LOOP[1]	Receive Mode	Transmit Mode	Loopback
Clocked	L	Open	Data/Clock recovery	Power down	No Loopback
Clocked	L	L	Data/Clock Recovery	Power down	No effect on op.
Clocked	L	H	Data/Clock Recovery	Power down	No Analog Loopback
Clocked	H	Open	Data/Clock Recovery	Transmit All Ones	No Loopback
Clocked	H	L	Data/Clock Recovery	Pulse Shaping ON	Remote Loopback
Clocked	H	H	Data/Clock Recovery	Transmit All Ones	No effect on op.
L	Clocked	Open	Power Down	Pulse Shaping ON	No Loopback
L	Clocked	L	Power Down	Pulse Shaping ON	No Remote Loopback
L	Clocked	H	Power Down	Pulse Shaping ON	No effect on op.
L	H	Open	Power Down	Pulse Shaping OFF	No Loopback
L	H	L	Power Down	Pulse Shaping OFF	No Remote Loop
L	H	H	Power Down	Pulse Shaping OFF	No effect on op.
L	L	X	Power Down	Power down	No Loopback
H	Clocked	Open	Data Recovery	Pulse Shaping ON	No Loopback
H	Clocked	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	Clocked	H	Data Recovery	Pulse Shaping ON	Analog Loopback
H	L	Open	Data Recovery	Power down	No Loopback
H	L	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	Open	Data Recovery	Pulse Shaping OFF	No Loopback
H	H	L	Data Recovery	Pulse Shaping OFF	Remote Loopback
H	H	H	Data Recovery	Pulse Shaping OFF	Analog Loopback

1. Hardware mode only.

2.11 Interfacing with 5V logic

The LXT388 can interface directly with 5V logic. The internal input pads are tolerant to 5V outputs from TTL and CMOS family devices.

2.12 Parallel Host Interface

The LXT388 incorporates a highly flexible 8-bit parallel microprocessor interface. The interface is generic and is designed to support both non-multiplexed and multiplexed address/data bus systems for Motorola and Intel bus topologies. Two pins (MUX and $\overline{\text{MOT}}$/INTL) select four different operating modes as shown in Table 9.

Table 9. Microprocessor Parallel Interface Selection

MUX	$\overline{\text{MOT}}$/INTL	Operating Mode
Low	Low	Motorola Non-Multiplexed
Low	High	Intel Non-Multiplexed
High	Low	Motorola Multiplexed
High	High	Intel Multiplexed

The interface includes an address bus (A4 - A0) and a data bus (D7 - D0) for non-multiplexed operation and an 8-bit address/data bus for multiplexed operation. $\overline{\text{WR}}$, $\overline{\text{RD}}$, R/$\overline{\text{W}}$, $\overline{\text{CS}}$, ALE, $\overline{\text{DS}}$, $\overline{\text{INT}}$ and RDY/$\overline{\text{ACK}}$ are used as control signals. A significant enhancement is an internal wait-state generator that controls an Intel and Motorola compatible handshake output signal (RDY/$\overline{\text{ACK}}$). In Motorola mode $\overline{\text{ACK}}$ Low signals valid information is on the data bus. During a write cycle a Low signal acknowledges the acceptance of the write data.

In Intel mode RDY High signals to the controlling processor that the bus cycle can be completed. While Low the microprocessor must insert wait states. This allows the LXT388 to interface with wait-state capable micro controllers, independent of the processor bus speed. To activate this function a reference clock is required on the MCLK pin.

There is one exception to write cycle timing for Intel non-multiplexed mode: Register 0Ah, the reset register. Because of timing issues, the RDY line remains high after the first part of the cycle is done, not signalling write cycle completion with another transition low. Add 2 microseconds of delay to allow the reset cycle to completely initialize the device before proceeding.

An additional active Low interrupt output signal indicates alarm conditions like LOS and DFM to the microprocessor.

The LXT388 has a 5 bit address bus and provides 18 user accessible 8-bit registers for configuration, alarm monitoring and control of the chip.

2.12.1 Motorola Interface

The Motorola interface is selected by asserting the $\overline{\text{MOT}}$/INTL pin Low. In non-multiplexed mode the falling edge of $\overline{\text{DS}}$ is used to latch the address information on the address bus. In multiplexed operation the address on the multiplexed address data bus is latched into the device with the falling edge of $\overline{\text{AS}}$. In non-multiplexed mode, $\overline{\text{AS}}$ should be pulled High.

The R/$\overline{\text{W}}$ signal indicates the direction of the data transfer. The $\overline{\text{DS}}$ signal is the timing reference for all data transfers and typically has a duty cycle of 50%. A read cycle is indicated by asserting R/$\overline{\text{W}}$ High with a falling edge on $\overline{\text{DS}}$. A write cycle is indicated by asserting R/$\overline{\text{W}}$ Low with a rising edge on $\overline{\text{DS}}$.

Both cycles require the $\overline{\text{CS}}$ signal to be Low and the Address pins to be actively driven by the microprocessor. Note that $\overline{\text{CS}}$ and $\overline{\text{DS}}$ can be connected together in Motorola mode. In a write cycle the data bus is driven by the microprocessor. In a read cycle the bus is driven by the LXT388.

2.12.2 Intel Interface

The Intel interface is selected by asserting the $\overline{\text{MOT}}$/INTL pin High. The LXT388 supports non-multiplexed interfaces with separate address and data pins when MUX is asserted Low, and multiplexed interfaces when MUX is asserted High. The address is latched in on the falling edge of ALE. In non-multiplexed mode, ALE should be pulled High. R/$\overline{\text{W}}$ is used as the $\overline{\text{RD}}$ signal and $\overline{\text{DS}}$ is used as the $\overline{\text{WR}}$ signal. A read cycle is indicated to the LXT388 when the processor asserts $\overline{\text{RD}}$ Low while the $\overline{\text{WR}}$ signal is held High. A write operation is indicated to the LXT388 by asserting $\overline{\text{WR}}$ Low while the $\overline{\text{RD}}$ signal is held High. Both cycles require the $\overline{\text{CS}}$ signal to be Low.

2.13 Interrupt Handling

2.13.1 Interrupt Sources

There are three interrupt sources:

1. Status change in the Loss Of Signal (LOS) status register (04H). The LXT388's analog/digital loss of signal processor continuously monitors the receiver signal and updates the specific LOS status bit to indicate presence or absence of a LOS condition.
2. Status change in the Driver Failure Monitoring (DFM) status register (05H). The LXT388's smart power driver circuit continuously monitors the output drivers signal and updates the specific DFM status bit to indicate presence or absence of a secondary driver short circuit condition.
3. Status change in the Alarm Indication Signal (AIS) status register (13H).The LXT388's receiver monitors the incoming data stream and updates the specific AIS status bit to indicate presence or absence of a AIS condition.

2.13.2 Interrupt Enable

The LXT388 provides a latched interrupt output ($\overline{\text{INT}}$). An interrupt occurs any time there is a transition on any enabled bit in the status register. Registers 06H, 07H and 14H are the LOS, DFM and AIS interrupt enable registers (respectively). Writing a logic "1" into the mask register will enable the respective bit in the respective Interrupt status register to generate an interrupt. The power-on default value is all zeroes. The setting of the interrupt enable bit does not affect the operation of the status registers.

Registers 08H, 09H and 15H are the LOS, DFM and AIS (respectively) interrupt status registers. When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (if one is not already pending). When an interrupt occurs, the $\overline{\text{INT}}$ pin is asserted Low. The output stage of the $\overline{\text{INT}}$ pin consists only of a pull-down device; an external pull-up resistor of approximately 10k ohm is required to support wired-OR operation.

2.13.3 Interrupt Clear

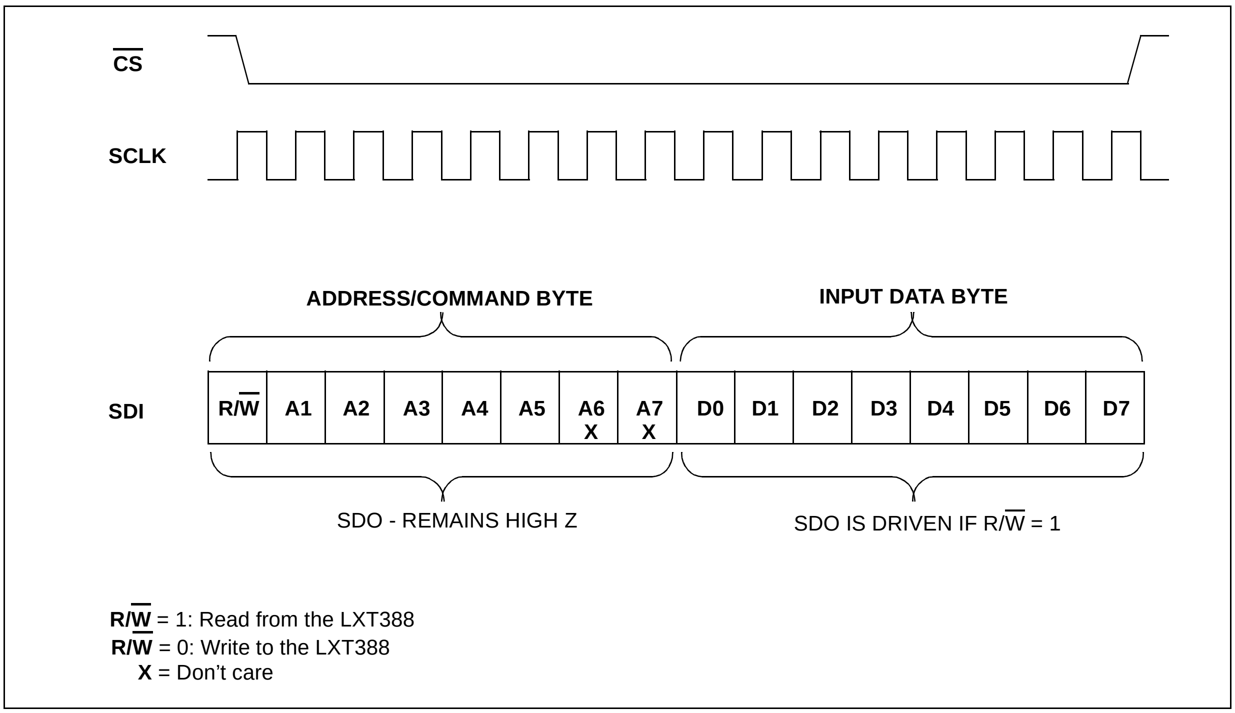
When an interrupt occurs, the interrupt service routine (ISR) should read the *interrupt status registers* (08H, 09H and 15H) to identify the interrupt source. Reading the Interrupt Status register clears the "sticky" bit set by the interrupt. Automatically clearing the register prepares it for the next interrupt. The ISR should then read the corresponding *status monitor register* to obtain the current status of the device. Note: there are three status monitor registers: the LOS (04H), the DFM

(05H) and the AIS (013H). Reading either status monitors register will clear its corresponding interrupts on the rising edge of the read or data strobe. When all pending interrupts are cleared, the $\overline{\text{INT}}$ pin goes High.

2.14 Serial Host Mode

The LXT388 operates in Serial Host Mode when the MODE pin is tied to VCC÷2. Figure 15 shows the SIO data structure. The registers are accessible through a 16 bit word: an 8bit Command/Address byte (bits R/$\overline{\text{W}}$ and A1-A7) and a subsequent 8bit data byte (bits D0-7). Bit R/$\overline{\text{W}}$ determines whether a read or a write operation occurs. Bits A5-0 in the Command/Address byte address specific registers (the address decoder ignores bits A7-6). The data byte depends on both the value of bit R/$\overline{\text{W}}$ and the address of the register as set in the Command/Address byte.

Figure 15. Serial Host Mode Timing



3.0 Register Descriptions

Table 10. Serial and Parallel Port Register Addresses

Name	Symbol	Address		Mode
		Serial Port A7-A1	Parallel Port A7-A0	
ID Register	ID	xx00000	xxx00000	R
Analog Loopback	ALOOP	xx00001	xxx00001	R/W
Remote Loopback	RLOOP	xx00010	xxx00010	R/W
TAOS Enable	TAOS	xx00011	xxx00011	R/W
LOS Status Monitor	LOS	xx00100	xxx00100	R
DFM Status Monitor	DFM	xx00101	xxx00101	R
LOS Interrupt Enable	LIE	xx00110	xxx00110	R/W
DFM Interrupt Enable	DIE	xx00111	xxx00111	R/W
LOS Interrupt Status	LIS	xx01000	xxx01000	R
DFM Interrupt Status	DIS	xx01001	xxx01001	R
Software Reset Register	RES	xx01010	xxx01010	R/W
Performance Monitoring	MON	xx01011	xxx01011	R/W
Digital Loopback	DL	xx01100	xxx01100	R/W
LOS/AIS Criteria Selection	LOSC	xx01101	xxx01101	R/W
Automatic TAOS Select	ATS	xx01110	xxx01110	R/W
Global Control Register	GCR	xx01111	xxx01111	R/W
Pulse Shaping Indirect Address Register	PSIAD	xx10000	xxx10000	R/W
Pulse Shaping Data Register	PSDAT	xx10001	xxx10001	R/W
Output Enable Register	OER	xx10010	xxx10010	R/W
AIS Status Register	AIS	xx10011	xxx10011	R
AIS Interrupt Enable	AISIE	xx10100	xxx10100	R/W
AIS Interrupt Status	AISIS	xx10101	xxx10101	R

Table 11. Register Bit Names

Register			Bit							
Name	Sym	RW	7	6	5	4	3	2	1	0
ID Register	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Analog Loopback	ALOOP	R/W	-	-	-	-	reserve d	reserved	AL1	AL0
Remote Loopback	RLOOP	R/W	-	-	-	-	reserve d	reserved	RL1	RL0

Table 11. Register Bit Names (Continued)

Register			Bit							
Name	**Sym**	**RW**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAOS Enable	TAOS	R/W	-	-	-	-	reserved	reserved	TAOS1	TAOS0
LOS Status Monitor	LOS	R	-	-	-	-	LOS3	LOS2	LOS1	LOS0
DFM Status Monitor	DFM	R	-	-	-	-	reserved	reserved	DFM1	DFM0
LOS Interrupt Enable	LIE	R/W	-	-	-	-	LIE3	LIE2	LIE1	LIE0
DFM Interrupt Enable	DIE	R/W	-	-	-	-	reserved	reserved	DIE1	DIE0
LOS Interrupt Status	LIS	R	-	-	-	-	LIS3	LIS2	LIS1	LIS0
DFM Interrupt Status	DIS	R	-	-	-	-	reserved	reserved	DIS1	DIS0
Software Reset Register	RES	R/W	-	-	-	-	RES3	RES2	RES1	RES0
Reserved	-	R/W	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Digital Loopback	DL	R/W	-	-	-	-	DL3	DL2	DL1	DL0
LOS/AIS Criteria Select	LACS	R/W	-	-	-	-	LACS3	LACS2	LACS1	LACS0
Automatic TAOS Select	ATS	R/W	-	-	-	-	reserved	reserved	ATS1	ATS0
Global Control Register	GCR	R/W	reserved	RAISEN	CDIS	CODEN	FIFO64	JACF	JASEL1	JASEL0
Pulse Shaping Indirect Address Register	PSIAD	R/W	reserved	reserved	reserved	reserved	reserved	LENAD2	LENAD1	LENAD0
Pulse Shaping Data Register	PSDAT	R/W	reserved	reserved	reserved	reserved	reserved	LEN2	LEN1	LEN0
Output Enable Register	OER	R/W	-	-	-	-	reserved	reserved	OE1	OE0
AIS Status Register	AIS	R	-	-	-	-	AIS3	AIS2	AIS1	AIS0
AIS Interrupt Enable	AISIE	R/W	-	-	-	-	AISIE3	AISIE2	AISIE1	AISIE0
AIS Interrupt Status	AISIS	R	-	-	-	-	AISIS3	AISIS2	AISIS1	AISIS0

Table 12. ID Register, ID (00H)

Bit	Name	Function
7-0	ID7-ID0	This register contains a unique revision code and is mask programmed. Revision — ID Code A1 — 00h B1 — 21h B2 — 22h

Table 13. Analog Loopback Register, ALOOP (01H)

Bit	Name	Function
1-0	AL1-AL0	Setting a bit to “1” enables analog local loopback for transceivers 1- 0 respectively.
7-2	-	Write “0” to these positions for normal operation.

Table 14. Remote Loopback Register, RLOOP (02H)

Bit	Name	Function
1-0	RL1-RL0	Setting a bit to “1” enables remote loopback for transceivers 1-0 respectively.
7-2	-	Write “0” to these positions for normal operation.

Table 15. TAOS Enable Register, TAOS (03H)

Bit[1]	Name	Function[2]
1-0	TAOS1-TAOS0	Setting a bit to “1” causes a continuous stream of marks to be sent out at the TTIP and TRING pins of the respective transceiver 1-0.
7-2	-	Write “0” to these positions for normal operation.

1. On power up all register bits are set to “0”.
2. MCLK is used as timing reference. If MCLK is not available then the channel TCLK is used as the reference. TAOS is not available in data recovery mode and line driver mode (MCLK=TCLK=High).

Table 16. LOS Status Monitor Register, LOS (04H)

Bit[1]	Name	Function
3-0	LOS3-LOS0	Respective bit(s) are set to “1” every time the LOS processor detects a valid loss of signal condition in receivers 3-0.

1. On power up all register bits are set to “0”. Any change in the state causes an interrupt. All LOS interrupts are cleared by a single read operation.

Table 17. DFM Status Monitor Register, DFM (05H)

Bit[1]	Name	Function
1-0	DFM1-DFM0	Respective bit(s) are set to “1” every time the short circuit monitor detects a valid secondary output driver short circuit condition in transceivers 1-0. Note that DFM is available only in configurations with no transmit series resistors (T1 mode with TVCC=3.3V).
7-2	-	Write “0” to these positions for normal operation.

1. On power-up all the register bits are set to “0”. All DFM interrupts are cleared by a single read operation.

Table 18. LOS Interrupt Enable Register, LIE (06H)

Bit[1]	Name	Function
3-0	LIE1-LIE0	Receiver 3-0 LOS interrupts are enabled by writing a “1” to the respective bit.
7-4	-	Write “0” to these positions for normal operation.
1. On power-up all the register bits are set to “0”and all interrupts are disabled.		

Table 19. DFM Interrupt Enable Register, DIE (07H)

Bit[1]	Name	Function
1-0	DIE13-DIE0	Transceiver 1-0 DFM interrupts are enabled by writing a “1” to the respective bit.
7-2	-	Write “0” to these positions for normal operation.
1. On power-up all the register bits are set to “0”and all interrupts are disabled.		

Table 20. LOS Interrupt Status Register, LIS (08H)

Bit	Name	Function
3-0	LIS3-LIS0	These bits are set to “1” every time a LOS status change has occurred since the last clear interrupt in receivers 3-0 respectively.

Table 21. DFM Interrupt Status Register, DIS (09H)

Bit	Name	Function
1-0	DIS1-DIS0	These bits are set to “1” every time a DFM status change has occurred since the last cleared interrupt in transceivers 1-0 respectively.

Table 22. Software Reset Register, RES (0AH)

Bit	Name	Function
3-0	RES3-RES0	Writing to this register initiates a 1 microsecond reset cycle, except in Intel non-multiplexed mode. When using Intel non-multiplexed host mode, extend cycle time to 2 microseconds. Please refer to Host Mode section for more information. This operation sets all LXT388 registers to their default values.

Table 23. Reserved (0BH)

Bit	Name	Function
7-0	reserved	Write “0” to these positions for normal operation.

Table 24. Digital Loopback Register, DL (0CH)

Bit[1]	Name	Function[2]
3-0	DL3-DL0	Setting a bit to “1” enables digital loopback for the respective channel.

1. On power up all register bits are set to “0”.
2. During digital loopback LOS and TAOS stay active and independent of TCLK, while data received on TPOS/TNEG/TCKLK is looped back to RPOS/RNEG/RCLK.

Table 25. LOS/AIS Criteria Register, LCS (0DH)

Bit[1]	Name	Function[2]
3-0	LCS3-LCS0[1]	T1 Mode[2] Don’t care. T1.231 compliant LOS/AIS detection is used. E1 Mode Setting a bit to “1” selects the ETS1 300233 LOS. Setting a bit to “0” selects G.775 LOS mode. AIS works correctly for both ETSI and ITU when the bit is cleared to “0”. See errata revision 10.3 or higher for a way to implement ETSI LOS and AIS.

1. On power-on reset the register is set to “0”.
2. T1 or E1 operation mode is determined by the PSDR settings.

Table 26. Automatic TAOS Select Register, ATS (0EH)

Bit[1]	Name	Function
1-0	ATS1-ATS0	Setting a bit to “1” enables automatic TAOS generation whenever a LOS condition is detected in the respective transceiver.
7-2	-	Write “0” to these positions for normal operation.

1. On power-on reset the register is set to “0”.This feature is not available in data recovery and line driver mode (MCLK= High and TCLK = High)

Table 27. Global Control Register, GCR (0FH)

<table>
<tr><th>Bit[1]</th><th>Name</th><th>Function</th></tr>
<tr><td>0</td><td>JASEL0</td><td rowspan="2">These bits determine the jitter attenuator position.
<table><tr><th>JASEL0</th><th>JASEL1</th><th>JA Position</th></tr><tr><td>1</td><td>0</td><td>Transmit Path</td></tr><tr><td>1</td><td>1</td><td>Receive Path</td></tr><tr><td>0</td><td>x</td><td>Disabled</td></tr></table></td></tr>
<tr><td>1</td><td>JASEL1</td></tr>
<tr><td>2</td><td>JACF</td><td>This bit determines the jitter attenuator low limit 3dB corner frequency. Refer to the Jitter Attenuator specifications for details (Table 46 on page 60).</td></tr>
<tr><td>3</td><td>FIFO64</td><td>This bit determines the jitter attenuator FIFO depth:
0 = 32 bit
1 = 64 bit</td></tr>
</table>

1. On power-on reset the register is set to “0”.

Table 27. Global Control Register, GCR (0FH) (Continued)

Bit[1]	Name	Function
4	CODEN	This bit selects the zero suppression code for unipolar operation mode: 0 = B8ZS/HDB3 (T1/E1 respectively) 1 = AMI
5	CDIS	This bit controls enables/disables the short circuit protection feature: 0 = enabled 1 = disabled
6	RAISEN	This bit controls automatic AIS insertion in the receive path when LOS occurs: 0 = Receive AIS insertion disabled on LOS 1 = RPOS/RNEG = AIS on LOS Note: this feature is not available in data recovery mode (MCLK=High). Disable AIS interrupts when changing this bit value to prevent inadvertent interrupts.
7	-	Reserved.
1. On power-on reset the register is set to “0”.		

Table 28. Pulse Shaping Indirect Address Register, PSIAD (10H)

Bit[1]	Name	Function
0-2	LENAD 0-2	The three bit value written to these bits determine the channel to be addressed: 0H = channel 0 1H = channel 1 2H = receiver 2 3H = receiver 3 Data can be read from (written to) the Pulse Shaping Data Register (PSDAT).
3 - 7	-	Reserved.
1. On power-on reset the register is set to “0”.		

Table 29. Pulse Shaping Data Register, PSDAT (11H)

<table>
<tr><th>Bit</th><th>Name</th><th colspan="6">Function</th></tr>
<tr><td rowspan="9">0-2</td><td rowspan="9">LEN 0-2 [1,3]</td><td colspan="6">LEN0-2 determine the LXT388 operation mode (T1 or E1) in all the receivers. In addition, for T1 operation, LEN2-0 set transmit pulse shaping in order to meet T1.102 pulse template at the DSX-1 cross-connect point for various cable lengths.</td></tr>
<tr><th>LEN2</th><th>LEN1</th><th>LEN0</th><th>Line Length</th><th>Cable Loss[2]</th><th>Operation Mode</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0 - 133 ft. ABAM</td><td>0.6 dB</td><td rowspan="5">T1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>133 - 266 ft. ABAM</td><td>1.2 dB</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>266 - 399 ft. ABAM</td><td>1.8 dB</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>399 - 533 ft. ABAM</td><td>2.4 dB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>533 - 655 ft. ABAM</td><td>3.0 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td colspan="2">E1 G.703, 75Ω coaxial cable and 120 Ω twisted pair cable.</td><td>E1</td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>3 - 7</td><td>-</td><td colspan="6">Reserved.</td></tr>
<tr><td colspan="8">1. On power-on reset the register is set to “0”.
2. Maximum cable loss at 772 KHz.
3. When reading LEN, bit values appear inverted. “B1” revision silicon will fix this so the bits read back correctly.</td></tr>
</table>

Table 30. Output Enable Register, OER (12H)

Bit[1]	Name	Function
1-0	$\overline{OE1}$ - $\overline{OE0}$	Setting a bit to “1” tristates the output driver of the corresponding transceiver.
7-2	-	Write “0” to these positions for normal operation.
1. On power-up all the register bits are set to “0”.		

Table 31. AIS Status Monitor Register, AIS (13H)

Bit[1]	Name	Function
3-0	AIS3-AIS0	Respective bit(s) are set to “1” every time the receiver detects a AIS condition in receivers 3-0.
1. On power-up all the register bits are set to “0”. All AIS interrupts are cleared by a single read operation.		

Table 32. AIS Interrupt Enable Register, AISIE (14H)

Bit[1]	Name	Function
3-0	AISIE3-AISIE0	Transceiver 3-0 AIS interrupts are enabled by writing a “1” to the respective bit.
7-4	-	Write “0” to these positions for normal operation.
1. On power-up all the register bits are set to “0”.		

Table 33. AIS Interrupt Status Register, AISIS (15H)

Bit[1]	Name	Function
3-0	AISIS3-AISIS0	These bits are set to “1” every time a AIS status change has occurred since the last clear interrupt in receivers 3-0 respectively.
1. On power-up all the register bits are set to “0”.		

4.0 JTAG Boundary Scan

4.1 Overview

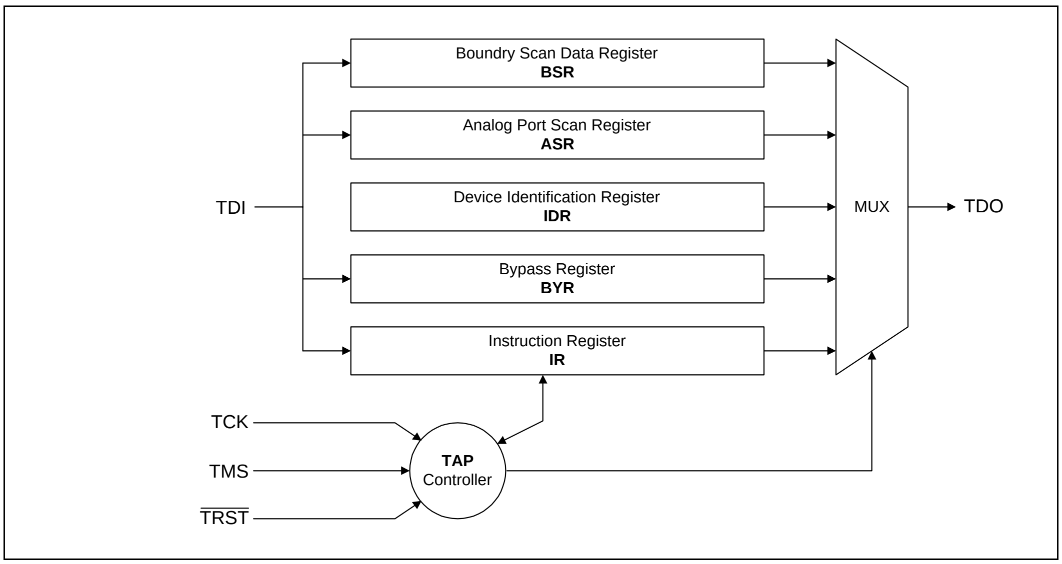
The LXT388 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

In addition to the traditional IEE1149.1 digital boundary scan capabilities, the LXT388 also includes analog test port capabilities. This feature provides access to the TIP and RING signals in each channel (transmit and receive). This way, the signal path integrity across the primary winding of each coupling transformer can be tested.

4.2 Architecture

Figure 16 represents the LXT388 basic JTAG architecture. The LXT388 JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

Figure 16. LXT388 JTAG Architecture



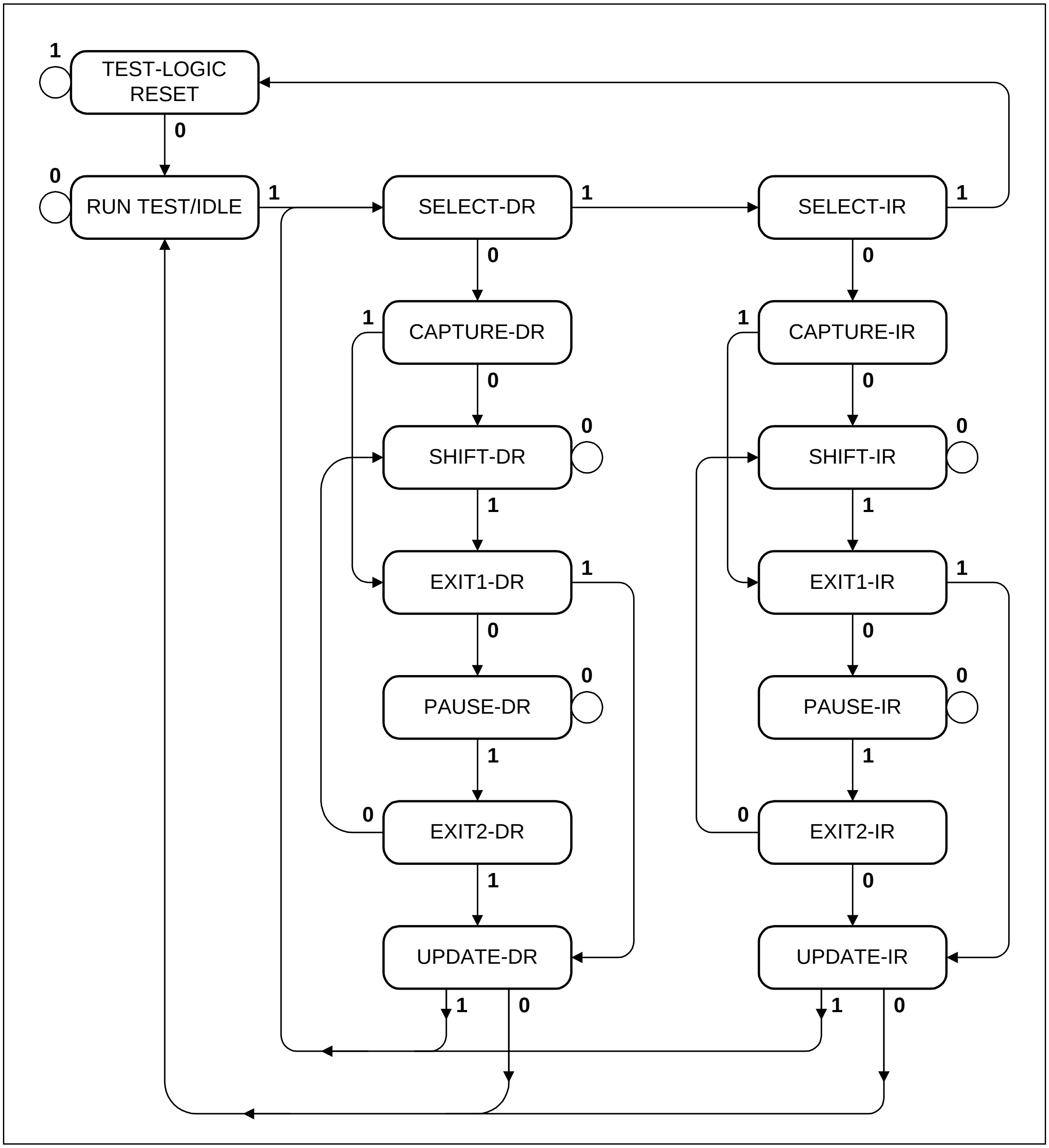
4.3 TAP Controller

The TAP controller is a 16 state synchronous state machine controlled by the TMS input and clocked by TCK (Figure 17).The TAP controls whether the LXT388 is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 34 describes in detail each of the states represented in Figure 17.

Table 34. TAP State Description

State	Description
Test Logic Reset	In this state the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test/Idle	The TAP controller stays in this state as long as TMS is low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage word its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 17. JTAG State Diagram



4.4 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 16.

4.4.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Table 35 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first.

Table 35. Boundary Scan Register (BSR)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
0	LOS3	O	LOS3	
	RNEG3	O	RNEG3	
	N/A	-	HIZ3	HIZ3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZ3 to “0” enables output on the pins. Setting HIZ3 to “1” tristates the pins.
	RPOS3	O	RPOS3	
	RCLK3	O	RCLK3	
	TNEG3	I	TNEG3	
	TPOS3	I	TPOS3	
	TCLK3	I	TCLK3	
	LOS2	O	LOS2	
	RNEG2	O	RNEG2	
	N/A	-	HIZ2	HIZ2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZ2 to “0” enables output on the pins. Setting HIZ2 to “1” tristates the pins.
	RPOS2	O	RPOS2	
	RCLK2	O	RCLK2	
	TNEG2	I	TNEG2	
	TPOS2	I	TPOS2	
	TCLK2	I	TCLK2	
	MCLK	I	MCLK	
	MODE	I	MODE	
	$\overline{\text{INT}}$	O	INTRUPTB	
	N/A	-	SDORDYENB	SDORDYENB controls the $\overline{\text{ACK}}$ pin. Setting SDORDYENB to “0” enables output on $\overline{\text{ACK}}$ pin. Setting SDORDYENB to “1” tristates the pin.
	$\overline{\text{ACK}}$	O	SDORDY	
	ALE	I	ALE	
	OE	I	OE	
	CLKE	I	CLKE	
	A0	I	A0	
	A1	I	A1	
	A2	I	A2	

1. LOOP4 corresponds to DLOOP0.
2. LOOP5 corresponds to DLOOP1.
3. LOOP6 corresponds to DLOOP2.
4. LOOP7 corresponds to DLOOP3..

Table 35. Boundary Scan Register (BSR) (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
	A3	I	A3	
	A4	I	A4	
	LOOP0	I/O	PADD0	
	LOOP0	I/O	PDO0	
	LOOP1	I/O	PADI1	
	LOOP1	I/O	PDO1	
	LOOP2	I/O	PADI2	
	LOOP2	I/O	PDO2	
	LOOP3	I/O	PADI3	
	LOOP3	I/O	PDO3	
	LOOP4[1]	I/O	PADI4	
	LOOP4[1]	I/O	PDO4	
	LOOP5[2]	I/O	PADI5	
	LOOP5[2]	I/O	PDO5	
	LOOP6[3]	I/O	PADI6	
	LOOP6[3]	I/O	PDO6	
	LOOP7[4]	I/O	PADI7	
	N/A	-	PDOENB	PDOENB controls the LOOP0 through LOOP7 pins. Setting PDOENB to “0” configures the pins as outputs. The output value to the pin is set in PDO[0..7]. Setting PDOENB to “1” tristates all the pins. The input value to the pins can be read in PADD[0..7].
	LOOP7	I/O	PDO7	
	$\overline{\text{CS}}$	I	CSB	
	MUX	I	MUX	
	$\overline{\text{RESET}}$	I	RSTB	
	$\overline{\text{MOT}}$/INTL	I	IMB	
	R/$\overline{\text{W}}$	I	RDB	
	$\overline{\text{DS}}$	I	WRB	
	TCLK1	I	TCLK1	
	TPOS1	I	TPOS1	
	TNEG1	I	TNEG1	
	RCLK1	O	RCLK1	
	RPOS1	O	RPOS1	
	N/A	-	HIZ1	HIZ1 controls the RPOS1, RNEG1 and RCLK1 pins. Setting HIZ1 to “0” enables output on the pins. Setting HIZ1 to “1” tristates the pins.

1. LOOP4 corresponds to DLOOP0.
2. LOOP5 corresponds to DLOOP1.
3. LOOP6 corresponds to DLOOP2.
4. LOOP7 corresponds to DLOOP3..

Table 35. Boundary Scan Register (BSR) (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
	RNEG1	O	RNEG1	
	LOS1	O	LOS1	
	TCLK0	I	TCLK0	
	TPOS0	I	TPOS0	
	TNEG0	I	TNEG0	
	RCLK0	O	RCLK0	
	RPOS0	O	RPOS0	
	N/A	-	HIZ0	HIZ0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZ0 to “0” enables output on the pins. Setting HIZ0 to “1” tristates the pins.
	RNEG0	O	RNEG0	
	LOS0	O	LOS0	

1. LOOP4 corresponds to DLOOP0.
2. LOOP5 corresponds to DLOOP1.
3. LOOP6 corresponds to DLOOP2.
4. LOOP7 corresponds to DLOOP3..

4.4.2 Device Identification Register (IDR)

The IDR register provides access to the manufacturer number, part number and the LXT388 revision. The register is arranged per IEEE 1149.1 and is represented in Table 36. Data into the IDR is shifted in LSB first.

Table 36. Device Identification Register (IDR)

Bit #	Comments
31 - 28	Revision Number
27 - 12	Part Number
11 - 1	Manufacturer Number
0	Set to “1”

4.4.3 Bypass Register (BYR)

The Bypass Register is a 1 bit register that allows direct connection between the TDI input and the TDO output.

4.4.4 Analog Port Scan Register (ASR)

The ASR is a 5 bit shift register used to control the analog test port at pins AT1, AT2. When the INTEST_ANALOG instruction is selected, TDI connects to the ASR input and TDO connects to the ASR output. After 5 TCK rising edges, a 5 bit control code is loaded into the ASR. Data into the ASR is shifted in LSB first.

Table 37 shows the 8 possible control codes and the corresponding operation on the analog port. The Analog Test Port can be used to verify continuity across the coupling transformers primary winding.

The Analog Test Port can be used to verify continuity across the coupling transformer's primary winding as shown in Figure 18. By applying a stimulus to the AT1 input, a known voltage will appear at AT2 for a given load. This, in effect, tests the continuity of a receive or transmit interface.

Table 37. Analog Port Scan Register (ASR)

ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11111	TTIP0	TRING0
11110	TTIP1	TRING1
11101	Reserved	
11100	Reserved	
11011	Reserved	
11010	Reserved	
11001	Reserved	
11000	Reserved	
10111	RTIP0	RRING0
10110	RTIP1	RRING1
10101	RTIP2	RRING2
10100	RTIP3	RRING3
10011	Reserved	
10010	Reserved	
10001	Reserved	
10000	Reserved	

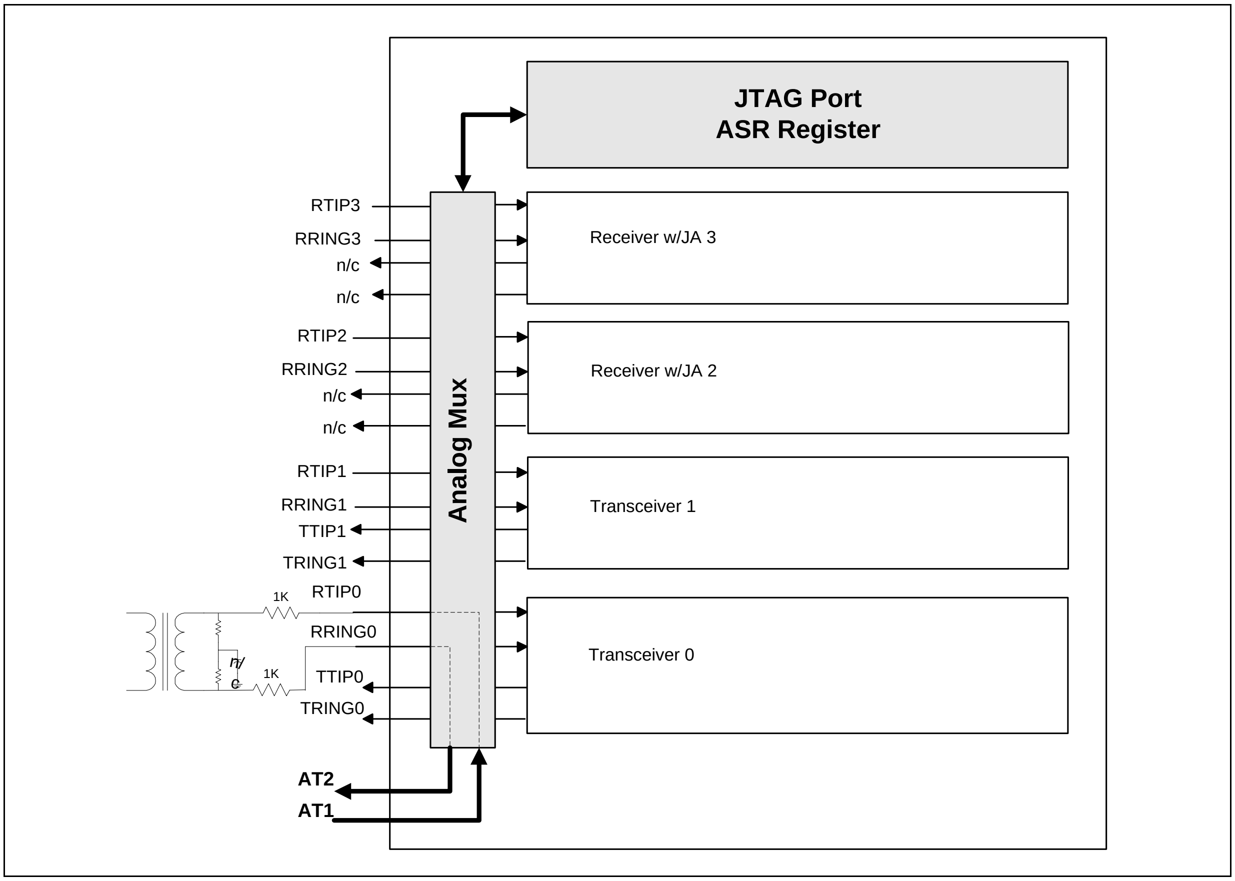
4.4.5 Instruction Register (IR)

The IR is a 3 bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 38 shows the valid instruction codes and the corresponding instruction description.

Table 38. Instruction Register (IR)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2. Refer to Table 37.
SAMPLE / PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT388 logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

Figure 18. Analog Test Port Application



5.0 Test Specifications

Table 39 through Table 58 and Figure 19 through Figure 36 represent the performance specifications of the LXT388 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 41 through Table 58 are guaranteed over the recommended operating conditions specified in Table Table 40.

Table 39. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC supply voltage	Vcc	-0.5	4.0	V
DC supply voltage	Tvcc 0-3	-0.5	7.0	V
Input voltage on any digital pin	Vin	GND-0.5	5.5	V
Input voltage on RTIP, RRING[1]	Vin	GND-0.5	VCC + 0.5 VCC + 0.5	V
ESD voltage on any Pin [2]	Vin	2000	–	V
Transient latch-up current on any pin	Iin		100	mA
Input current on any digital pin [3]	Iin	-10	10	mA
DC input current on TTIP, TRING [3]	Iin	–	±100	mA
DC input current on RTIP, RRING [3]	Iin	–	±100	mA
Storage temperature	Tstor	-65	+150	°C
Case Temperature, 100 pin LQFP package	T_{case}	–	120	mW
Case Temperature, 160 pin PBGA package	T_{case}	–	120	°C/W

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
1. Referenced to ground.
2. Human body model.
3. Constant input current.

Table 40. Recommended Operating Conditions

Parameter	LEN	Sym	Min	Typ	Max	Unit	Test Condition
Digital supply voltage (VCC)		VCC	3.135	3.3	3.465	V	3.3V ± 5%
Transmitter supply voltage, TVCC=5V nominal		TVCC	4.75	5.0	5.25	V	5V ± 5%
Transmitter supply voltage, TVCC=3.3V nominal		TVCC	3.135	3.3	3.465	V	3.3V ± 5%
Ambient operating temperature		Ta	-40	25	+85	°C	
Average Digital Power Supply Current [1, 4]		I_{VCC}	-	45	60	mA	

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. Power consumption includes power absorbed by line load and external transmitter components.
3. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).
4. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.

Table 40. Recommended Operating Conditions (Continued)

Parameter			LEN	Sym	Min	Typ	Max	Unit	Test Condition
Average Transmitter Power Supply Current, T1 Mode [1, 2, 3]				I_{TVCC}	-	108 60	123 -	mA mA	100% 1's 50% 1's
Output load at TTIP and TRING				Rl	25	–	–	Ω	
Device Power Consumption									
Mode	**TVCC**	**Load**	**LEN**			**Typ**	**Max[1,2]**	**Unit**	**Test Condition**
E1	3.3V	75 Ω	000	-	-	350	-	mW	50% 1's
				-	-	-	470	mW	100% 1's
		120 Ω	000	-	-	330	-	mW	50% 1's
				-	-	-	430	mW	100% 1's
T1[3]	3.3V	100 Ω	101-111	-	-	410	-	mW	50% 1's
				-	-	-	640	mW	100% 1's
E1	5.0V	75 Ω	000	-	-	470	-	mW	50% 1's
				-	-	-	640	mW	100% 1's
		120 Ω	000	-	-	440	-	mW	50% 1's
				-	-	-	650	mW	100% 1's
T1[3]	5.0V	100 Ω	101-111	-	-	580	-	mW	50% 1's
				-	-	-	870	mW	100% 1's

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. Power consumption includes power absorbed by line load and external transmitter components.
3. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).
4. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.

Table 41. DC Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
High level input voltage		Vih	2	–	–	V	
Low level input voltage		Vil	–	–	0.8	V	
High level output voltage[1]		Voh	2.4	–	VCC	V	IOUT= 400µA
Low level output voltage[1]		Vol	–	–	0.4	V	IOUT= 1.6mA
MODE, LOOP0-3 and JASEL	Low level input voltage	Vinl	–	–	1/3VCC-0.2	V	
	Midrange level input voltage	Vinm	1/3VCC+0.2	1/2VCC	2/3VCC-0.2	V	
	High level input voltage	Vinh	2/3VCC+0.2	–	–	V	
	Low level input current	Iinl	–	–	50	µA	
	High level input current	Iinh	–	–	50	µA	
Input leakage current		Iil	-10		+10	µA	
Tri state leakage current		Ihz	-10		+10	µA	

Table 41. DC Characteristics (Continued)

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Tri state output current	Ihz	–	–	1	µA	TTIP, TRING
Line short circuit current	–	–	–	50	mA RMS	2 x 11 Ω series resistors and 1:2 transformer
Input Leakage (TMS, TDI, $\overline{TRST}$)	–	–	–	50	µA	

Table 42. E1 Transmit Transmission Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Output pulse amplitude	75Ω 120Ω	–	2.14 2.7	2.37 3.0	2.60 3.3	V V	Tested at the line side
Peak voltage of a space	75Ω 120Ω	–	-0.237 -0.3		0.237 0.3	V V	
Transmit amplitude variation with supply		–	-1		+1	%	
Difference between pulse sequences		–			200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		–	0.95		1.05		At the nominal half amplitude
Transmit transformer turns ratio for 75/120Ω characteristic impedance		–		1:2			Rt = 11 Ω ± 1%
Note: Transmit return loss 75 Ω coaxial cable[1]	***Note:*** 51kHz to 102 kHz ***Note:*** 102 kHz to 2.048 MHz ***Note:*** 2.048 MHz to 3.072 MHz	–	15 15 15	17 17 17	–	dB dB dB	Using components in the LXD384 evaluation board.
Transmit return loss 120 Ω twisted pair cable[1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	20 20 20	–	dB dB dB	Using components in the LXD384 evaluation board.
Transmit intrinsic jitter; 20Hz to 100kHz		–	–	0.030	0.050	U.I.	Tx path TCLK is jitter free
Transmit path delay	Bipolar mode			2		U.I.	JA Disabled
	Unipolar mode			7		U.I.	

1. Guaranteed by design and other correlation methods.

Table 43. E1 Receive Transmission Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Permissible cable attenuation	–	–	–	12	dB	@1024 kHz
Receiver dynamic range	DR	0.5	–	–	Vp	
Signal to noise interference margin	S/I	-15	–	–	dB	Per G.703, O.151 @ 6 dB cable Attenuation
Data decision threshold	SRE	43	50	57	%	Rel. to peak input voltage
Data slicer threshold	–	–	150	–	mV	

1. Guaranteed by design and other correlation methods.

Table 43. E1 Receive Transmission Characteristics (Continued)

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	–	32 2048	–	–	G.775 recommendation ETSI 300 233 specification
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	1Hz to 20Hz 20Hz to 2.4kHz 18kHz to 100kHz	–	36 1.5 0.2	–	–	U.I. U.I. U.I.	G735 recommendation Note 1 Cable Attenuation is 6 dB
Differential receiver input impedance		–	–	70	–	k Ω	@1.024 MHz
Input termination resistor tolerance		–	–	–	±1	%	
Common mode input impedance to ground		–	–	20	–	k W	
Input return loss[1]	51 kHz - 102 kHz 102 - 2048 kHz 2048kHz - 3072 kHz	–	20 20 20		–	dB dB dB	Measured against nominal impedance using components in the LXD384 evaluation board.
LOS delay time		–	–	30	–	∝σ	Data recovery mode
LOS reset		–	10	–	255	marks	Data recovery mode
Receive intrinsic jitter, RCLK output		–	–	0.040	0.0625	U.I.	Wide band jitter
Receive path delay	Bipolar mode			1		U.I.	JA Disabled
	Unipolar mode			6		U.I.	

1. Guaranteed by design and other correlation methods.

Table 44. T1 Transmit Transmission Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Output pulse amplitude		–	2.4	3.0	3.6	V	Measured at the DSX
Peak voltage of a space		–	-0.15	–	+0.15	V	
Driver output impedance[1]		–	–	1	–	Ω	@ 772 KHz
Transmit amplitude variation with power supply		–	-1	–	+1	%	
Ratio of positive to negative pulse amplitude		–	0.95	–	1.05	–	T1.102, isolated pulse
Difference between pulse sequences		–	–	–	200	mV	For 17 consecutive pulses, GR-499-CORE
Pulse width variation at half amplitude		–	–	–	20	ns	
Jitter added by Transmitter[1]	10Hz - 8KHz 8KHz - 40KHz 10Hz - 40KHz Wide Band	–	–	–	0.020 0.025 0.025 0.050	UI_{pk-pk}	AT&T Pub 62411 TCLK is jitter free.
Output power levels[2]	@ 772 KHz @ 1544 KHz	–	12.6 -29	–	17.9	dBm dBm	T1.102 - 1993 Referenced to power at 772 KHz

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 44. T1 Transmit Transmission Characteristics (Continued)

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Transmit return loss [1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	21 21 21	–	dB dB dB	With transmit series resistors (TVCC=5V). Using components in the LXD384 evaluation board.
Transmit path delay	Bipolar mode			2		U.I.	JA Disabled
	Unipolar mode			7		U.I.	

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 45. T1 Receive Transmission Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@ 772 KHz
Receiver dynamic range		DR	0.5	–	–	Vp	
Signal to noise interference margin		S/I	-16.5	–	–	dB	@ 655 ft. of 22 ABAM cable
Data decision threshold		SRE	63	70	77	%	Rel. to peak input voltage
Data slicer threshold		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	100	175	250	–	T1.231 - 1993
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	0.1Hz to 1Hz 4.9Hz to 300Hz 10KHz to 100KHz	-	138 28 0.4	-	-	U.I. U.I. U.I.	AT&T Pub. 62411
Differential receiver input impedance		-	-	70	-	k Ω	@772 kHz
Input termination resistor tolerance		-	-		±1	%	
Common mode input impedance to ground		-	-	20	-	k Ω	
Input return loss[1]	51 KHz - 102 KHz 102 - 2048 KHz 2048 KHz - 3072 KHz	-	20 20 20	-	-	dB dB dB	Measured against nominal impedance. Using components in the LXD384 evaluation board.
LOS delay time		-	-	30	-	µs	Data recovery mode
LOS reset		-	10	-	255	-	Data recovery mode
Receive intrinsic jitter, RCLK output[1]		-	-	0.035	0.0625	U.I.	Wide band jitter
Receive path delay	Bipolar mode			1		U.I.	JA Disabled
	Unipolar mode			6		U.I.	

1. Guaranteed by design and other correlation methods.

Table 46. Jitter Attenuator Characteristics

Parameter			Min	Typ	Max	Unit	Test Condition
E1 jitter attenuator 3dB corner frequency, host mode[1]	JACF = 0	32bit FIFO	-	2.5	-	Hz	Sinusoidal jitter modulation
		64bit FIFO	-	3.5	-	Hz	
	JACF = 1	32bit FIFO	-	2.5	-	Hz	
		64bit FIFO	-	3.5	-	Hz	
T1 jitter attenuator 3dB corner frequency, host mode[1]	JACF = 0	32bit FIFO	-	3	-	Hz	
		64bit FIFO	-	3	-	Hz	
	JACF = 1	32bit FIFO	-	6	-	Hz	
		64bit FIFO	-	6	-	Hz	
Jitter attenuator 3dB corner frequency, hardware mode[1]		E1	-	3.5	-	Hz	
		T1	-	6	-	Hz	
Data latency delay		32bit FIFO	-	17	-	UI	Delay through the Jitter attenuator only. Add receive and transmit path delay for total throughput delay.
		64bit FIFO	-	33	-	UI	
Input jitter tolerance before FIFO overflow or underflow		32bit FIFO	-	24	-	UI	
		64bit FIFO	-	56	-	UI	
E1 jitter attenuation	@ 3 Hz @ 40 Hz @ 400 Hz @ 100 KHz		-0.5 -0.5 +19.5 +19.5	–	–	dB	ITU-T G.736, See Figure 35 on page 76
T1 jitter attenuation	@ 1 Hz @ 20 Hz @ 1 KHz @ 1.4 KHz @ 70 KHz		0 0 33.3 40 40	–	–	dB	AT&T Pub. 62411, See Figure 35 on page 76
Output Jitter in remote loopback[1]				0.060	0.11	UI	ETSI CTR12/13 Output jitter

1. Guaranteed by design and other correlation methods.

Table 47. Analog Test Port Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
3 dB bandwidth	At13db	-	5	-	MHz	
Input voltage range	At1iv	0	-	VCC	V	
Output voltage range	At2ov	0	-	VCC	V	

Figure 19. Transmit Clock Timing Diagram

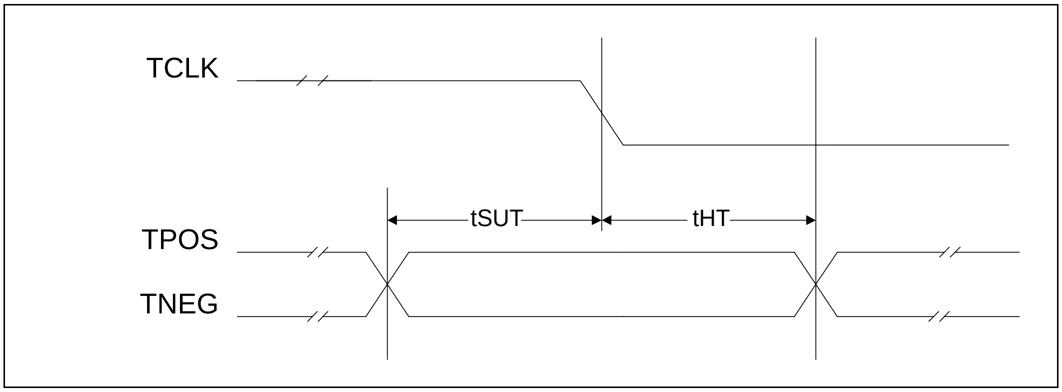


Table 48. Transmit Timing Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		–	-100	–	100	ppm	
Master clock duty cycle		–	40	–	60	%	
Output pulse width	E1	Tw	219	244	269	ns	
	T1	Tw	291	324	356	ns	
Transmit clock frequency	E1	Tclke1	-	2.048	-	MHz	
	T1	Tclkt1	-	1.544	-	MHz	
Transmit clock tolerance		Tclkt	-50	–	+50	ppm	
Transmit clock burst rate		Tclkb	-	–	20	MHz	Gapped transmit clock
Transmit clock duty cycle		Tdc	10	–	90	%	NRZ mode
E1 TPOS/TNEG pulse width (RZ mode)		Tmpwe1	236	–	252	ns	RZ mode (TCLK = H for >16 clock cycles)
TPOS/TNEG to TCLK setup time		Tsut	20	-	-	ns	
TCLK to TPOS/TNEG hold time		Tht	20	-	-	ns	
Delay time OE Low to driver High Z		Toez	-	-	1	µs	
Delay time TCLK Low to driver High Z		Ttz	50	60	75	µs	

Table 49. Receive Timing Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Condition
Clock recovery capture range	E1	–	–	±80	–	ppm	Relative to nominal frequency MCLK = ±100 ppm
	T1	–	–	±180	–	ppm	
Receive clock duty cycle [1]		Rckd	40	50	60	%	
Receive clock pulse width [1]	E1	Tpw	447	488	529	ns	
	T1	Tpw	583	648	713	ns	
Receive clock pulse width Low time	E1	Tpwl	203	244	285	ns	
	T1	Tpwl	259	324	389	ns	
Receive clock pulse width High time	E1	Tpwh	203	244	285	ns	
	T1	Tpwh	259	324	389	ns	
Rise/fall time [4]		Tr	20	–	–	ns	@ CL=15 pF
RPOS/RNEG pulse width (MCLK=H) [2]	E1	Tpwdl	200	244	300	ns	
	T1	Tpwdl	250	324	400	ns	
RPOS/RNEG to RCLK rising setup time	E1	Tsur	200	244	–	ns	
	T1		200	324	–	ns	
RCLK Rising to RPOS/RNEG hold time	E1	Thr	200	244	–	ns	
	T1		200	324	–	ns	
Delay time between RPOS/RNEG and RCLK		–	–	–	5	ns	MCLK = H [3]

1. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).
2. Clock recovery is disabled in this mode.
3. If MCLK = H the receive PLLs are replaced by a simple EXOR circuit.
4. For all digital outputs.

Figure 20. Receive Clock Timing Diagram

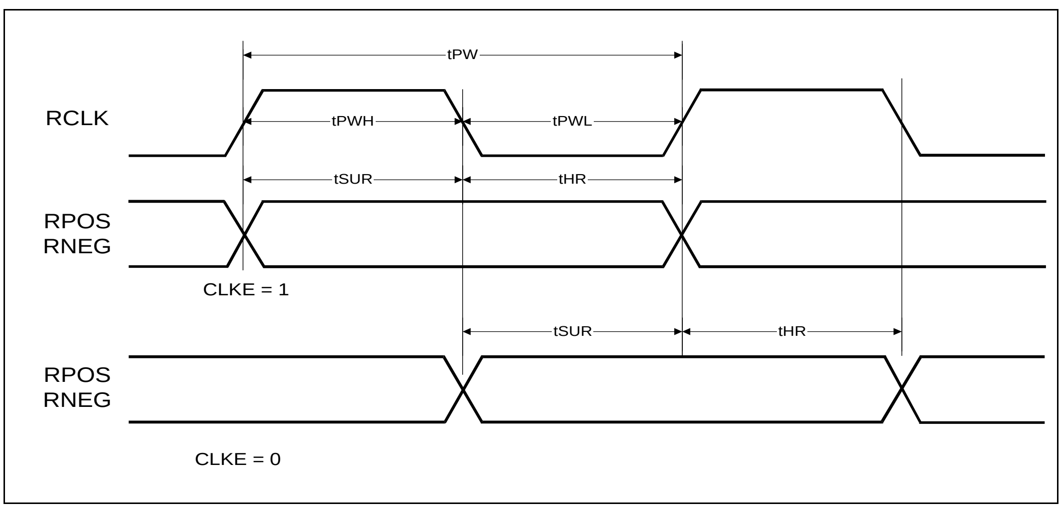


Table 50. Intel Mode Read Timing Characteristics

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to latch	Tsalr	10	–	–	ns	
Valid address latch pulse width	Tvl	30	–	–	ns	
Latch active to active read setup time	Tslr	10	–	–	ns	
Chip select setup time to active read	Tscsr	0	–	–	ns	
Chip select hold time from inactive read	Thcsr	0	–	–	ns	
Address hold time from inactive ALE	Thalr	5			ns	
Active read to data valid delay time	Tprd	10	–	50	ns	
Address setup time to $\overline{RD}$ inactive	Thar	1	–	–	ns	
Address hold time from $\overline{RD}$ inactive	Tsar	5	–	–	ns	
Inactive read to data tri-state delay time	Tzrd	3	–	35	ns	
Valid read signal pulse width	Tvrd	60	–	–	ns	
Inactive read to inactive $\overline{INT}$ delay time	Tint	–	–	10	ns	
Active chip select to RDY delay time	Tdrdy	0	–	12	ns	
Active ready Low time	Tvrdy	–	–	40	ns	
Inactive ready to tri-state delay time	Trdyz	–	–	3	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7, all other outputs are loaded with 50pF.

Table 51. JTAG Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Cycle time	Tcyc	200	-	-	ns	
J-TMS/J-TDI to J-TCK rising edge time	Tsut	50	-	-	ns	
J-CLK rising to J-TMS/L-TDI hold time	Tht	50	-	-	ns	
J-TCLK falling to J-TDO valid	Tdod	-	-	50	ns	

Figure 21. JTAG Timing

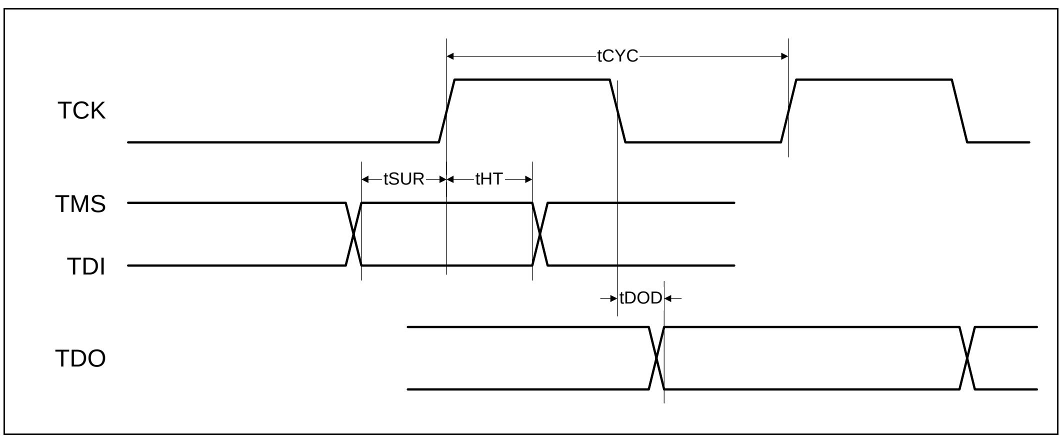


Figure 22. Non-Multiplexed Intel Mode Read Timing

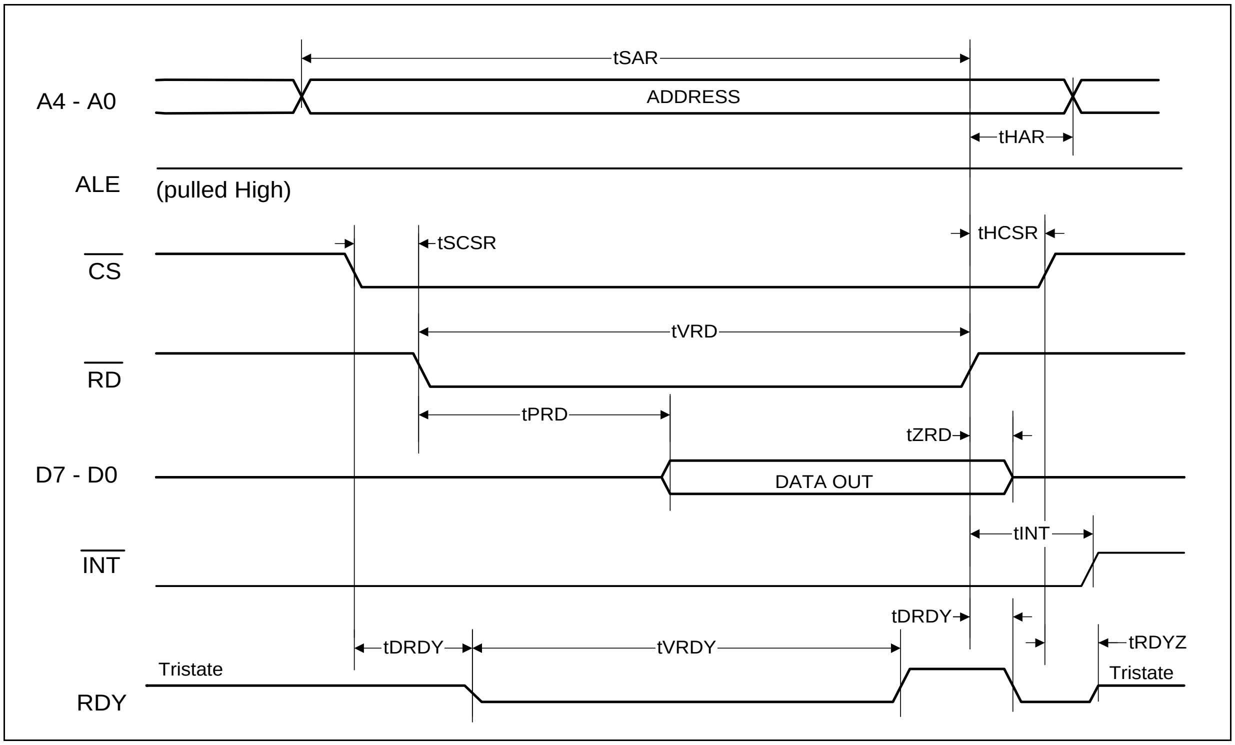


Figure 23. Multiplexed Intel Read Timing

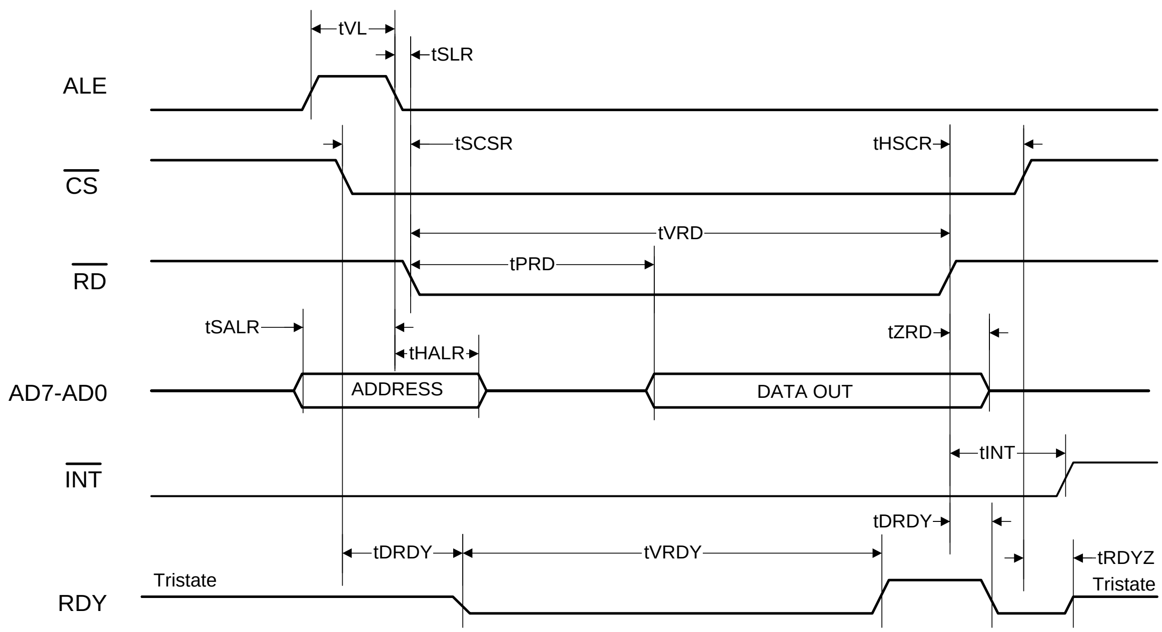


Table 52. Intel Mode Write Timing Characteristics

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to latch	Tsalw	10	–	–	ns	
Valid address latch pulse width	Tvl	30	–	–	ns	
Latch active to active write setup time	Tslw	10	–	–	ns	
Chip select setup time to active write	Tscsw	0	–	–	ns	
Chip select hold time from inactive write	Thcsw	0	–	–	ns	
Address hold time from inactive ALE	Thalw	5			ns	
Data valid to write active setup time	Tsdw	40	–	–	ns	
Data hold time to active write	Thdw	30	–	–	ns	
Address setup time to $\overline{WR}$ inactive	Thaw	2	–	–	ns	
Address hold time from $\overline{WR}$ inactive	Tsaw	6	–	–	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7, all other outputs are loaded with 50pF.
3. These times don't apply for Reset Register 0Ah, since RDY line goes low once during the cycle. Please refer to Reset Operation and Host Mode sections for more information.

Table 52. Intel Mode Write Timing Characteristics (Continued)

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Valid write signal pulse width	Tvwr	60	–	–	ns	
Inactive write to inactive $\overline{INT}$ delay time	Tint	–	–	10	ns	
Chip select to RDY delay time[3]	Tdrdy	0	–	12	ns	
Active ready Low time	Tvrdy	–	–	40	ns	
Inactive ready to tri-state delay time[3]	Trdyz	–	–	3	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7, all other outputs are loaded with 50pF.
3. These times don't apply for Reset Register 0Ah, since RDY line goes low once during the cycle. Please refer to Reset Operation and Host Mode sections for more information.

Figure 24. Non-Multiplexed Intel Mode Write Timing

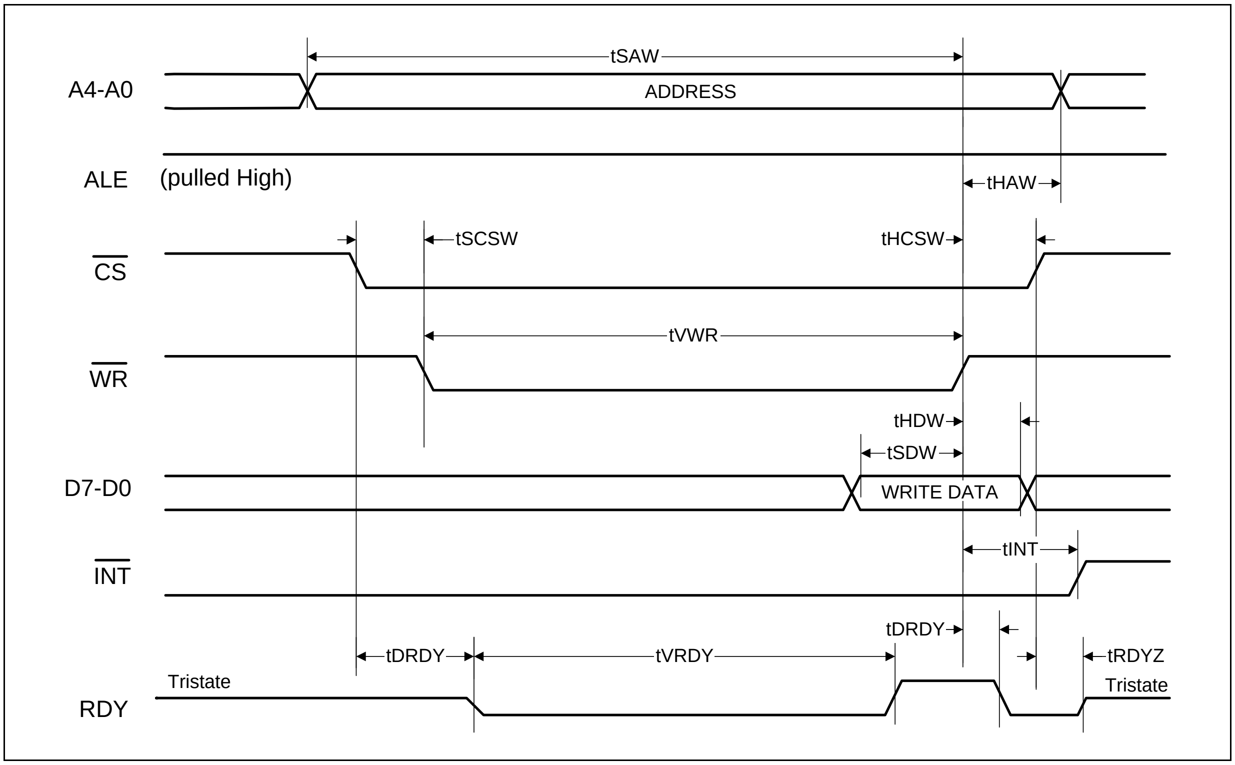


Figure 25. Multiplexed Intel Mode Write Timing

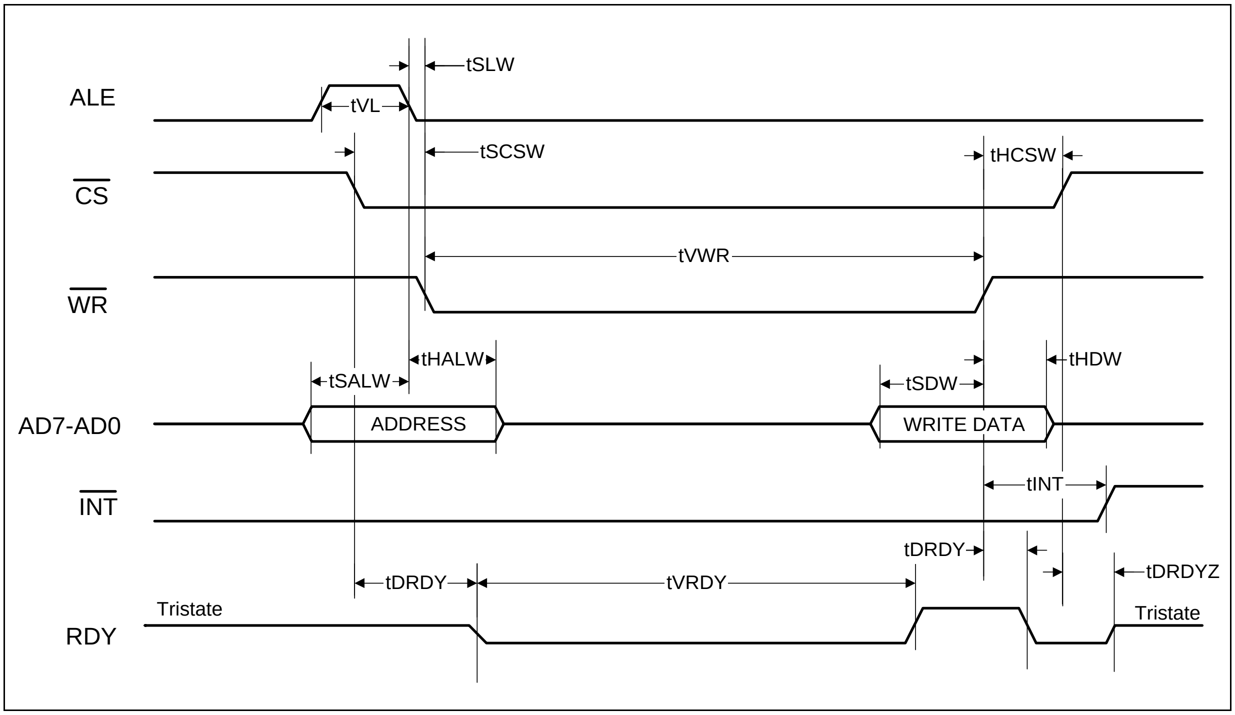


Table 53. Motorola Bus Read Timing Characteristics

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to address or data strobe	Tsar	10	–	–	ns	
Address hold time from address or data strobe	Thar	5	–	–	ns	
Valid address strobe pulse width	Tvas	95	–	–	ns	
R/$\overline{W}$ setup time to active data strobe	Tsrw	10	–	–	ns	
R/$\overline{W}$ hold time from inactive data strobe	Thrw	0	–	–	ns	
Chip select setup time to active data strobe	Tscs	0	–	–	ns	
Chip select hold time from inactive data strobe	Thcs	0	–	–	ns	
Address strobe active to data strobe active delay	Tasds	20	–	–	ns	
Delay time from active data strobe to valid data	Tpds	3	–	30	ns	
Delay time from inactive data strobe to data High Z	Tdz	3	–	30	ns	
Valid data strobe pulse width	Tvds	60	–	–	ns	
Inactive data strobe to inactive $\overline{INT}$ delay time	Tint	–	–	10	ns	
Data strobe inactive to address strobe inactive delay	Tdsas	15	–	–	ns	
$\overline{DS}$ asserted to $\overline{ACK}$ asserted delay	Tdackp	–	–	40	ns	
$\overline{DS}$ deasserted to $\overline{ACK}$ deasserted delay	Tdack	–	–	10	ns	
Active $\overline{ACK}$ to valid data delay	Tpack	–	–	0	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L = 100pF on D0-D7, all other outputs are loaded with 50pF.

Figure 26. Non-Multiplexed Motorola Mode Read Timing

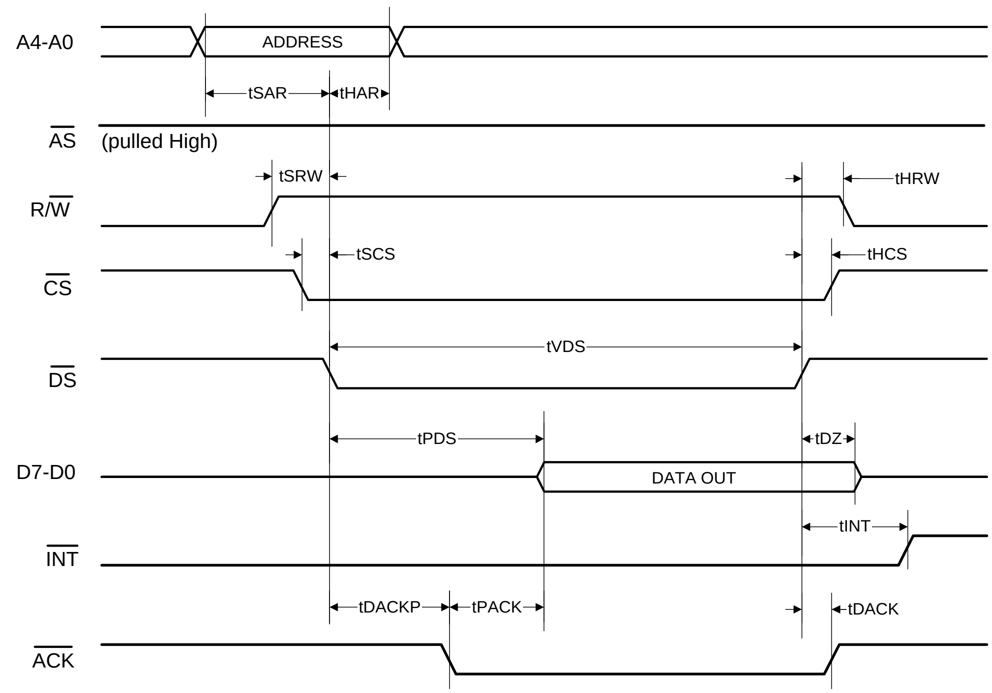


Figure 27. Multiplexed Motorola Mode Read Timing

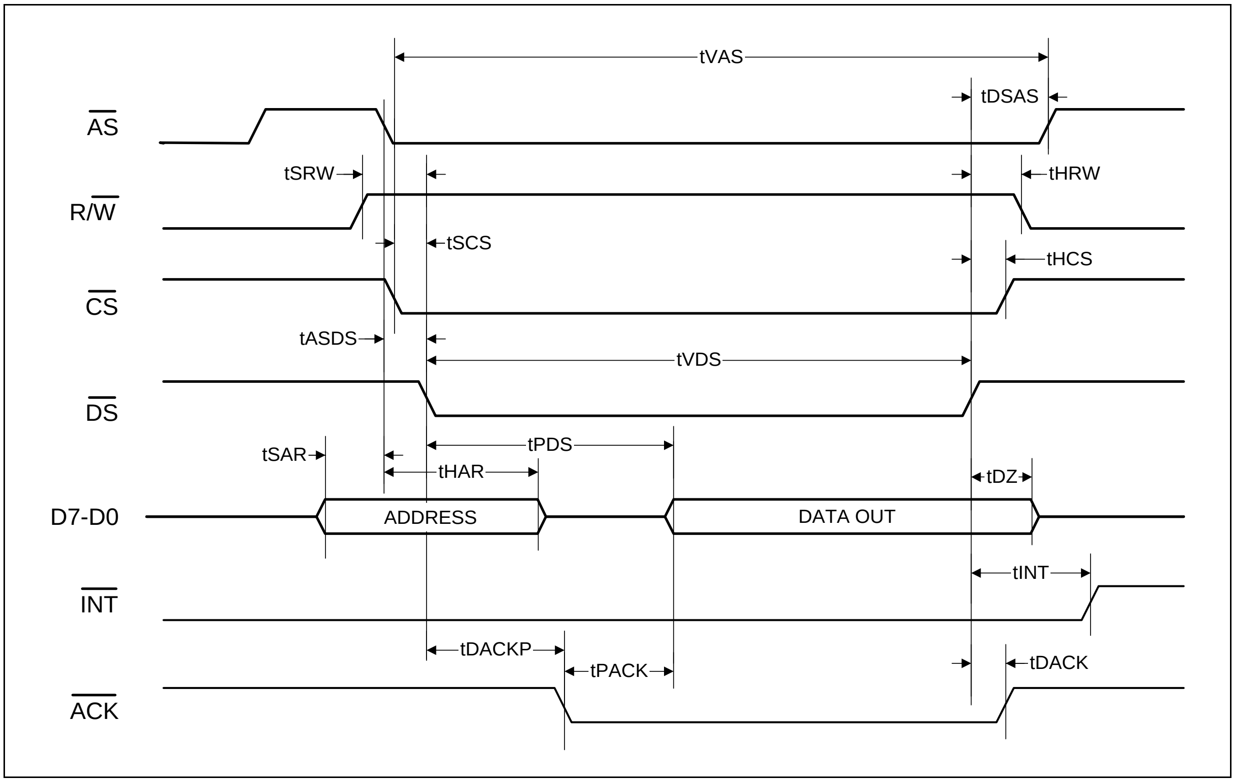


Table 54. Motorola Mode Write Timing Characteristics

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to address strobe	Tsas	10	–	–	ns	
Address hold time to address strobe	Thas	5	–	–	ns	
Valid address strobe pulse width	Tvas	95	–	–	ns	
R/$\overline{W}$ setup time to active data strobe	Tsrw	10	–	–	ns	
R/$\overline{W}$ hold time from inactive data strobe	Thrw	0	–	–	ns	
Chip select setup time to active data strobe	Tscs	0	–	–	ns	
Chip select hold time from inactive data strobe	Thcs	0	–	–	ns	
Address strobe active to data strobe active delay	Tasds	20	–	–	ns	
Data setup time to $\overline{DS}$ deassertion	Tsdw	40	–	–	ns	
Data hold time from $\overline{DS}$ deassertion	Thdw	30	–	–	ns	
Valid data strobe pulse width	Tvds	60	–	–	ns	
Inactive data strobe to inactive $\overline{INT}$ delay time	Tint	–	–	10	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7, all other outputs are loaded with 50pF.

Table 54. Motorola Mode Write Timing Characteristics (Continued)

Parameter[2]	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Data strobe inactive to address strobe inactive delay	Tdsas	15	–	–	ns	
Active data strobe to $\overline{\text{ACK}}$ output enable time	Tdack	0	–	12	ns	
$\overline{\text{DS}}$ asserted to $\overline{\text{ACK}}$ asserted delay	Tdackp		–	40	ns	

1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
2. C_L= 100pF on D0-D7, all other outputs are loaded with 50pF.

Figure 28. Non-Multiplexed Motorola Mode Write Timing

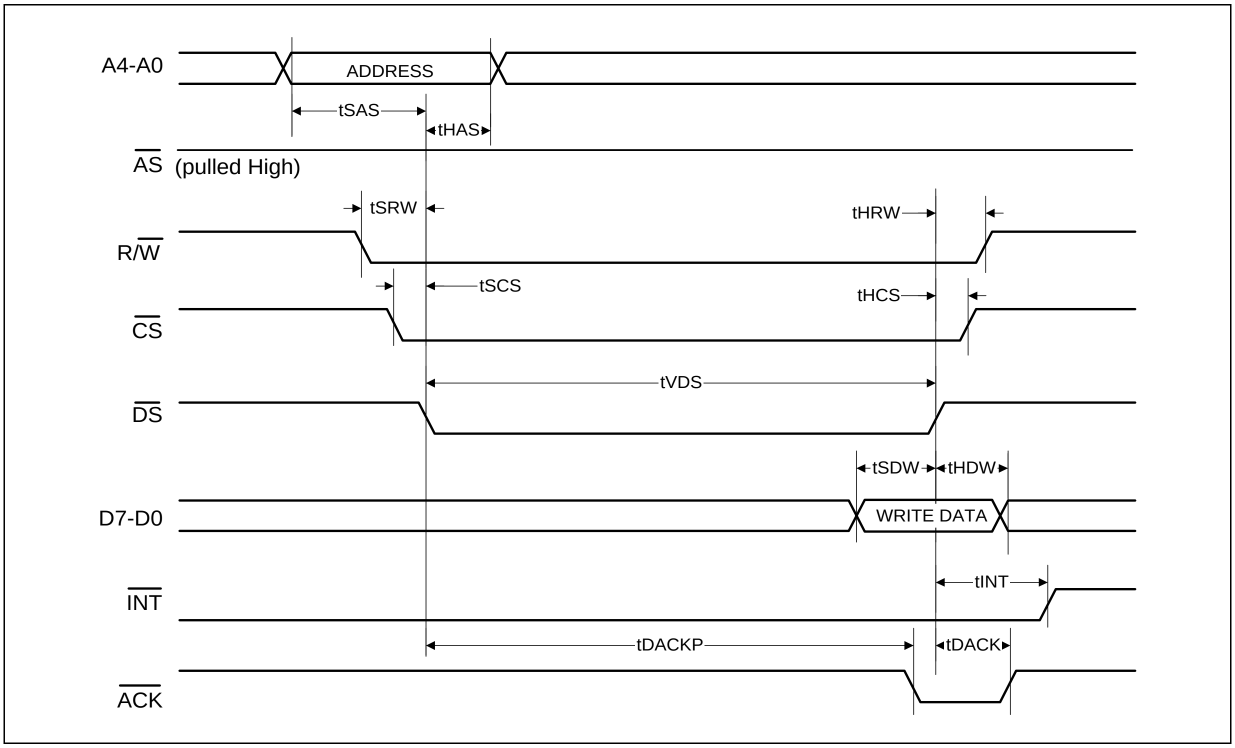


Figure 29. Multiplexed Motorola Mode Write Timing

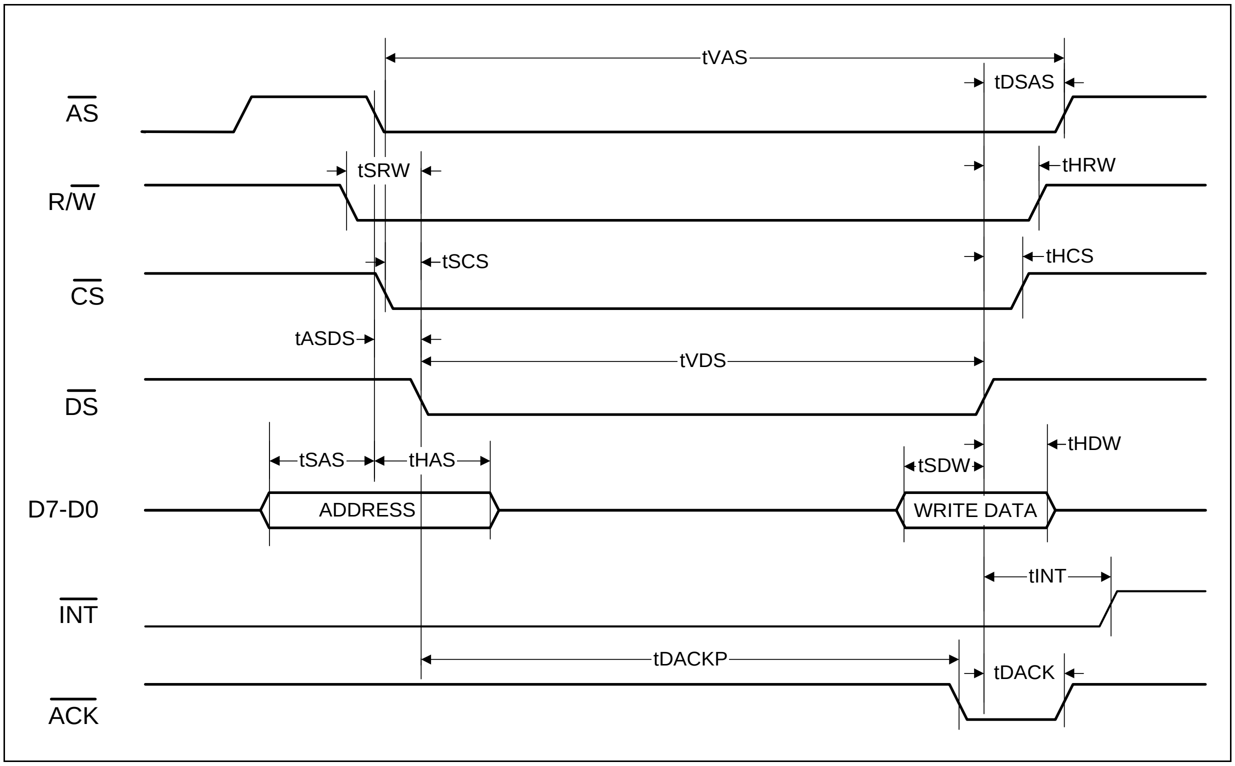


Table 55. Serial I/O Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Condition
Rise/fall time any pin	Trf	-	-	100	ns	Load 1.6mA, 50 pF
SDI to SCLK setup time	Tdc	5	-	-	ns	
SCLK to SDI hold time	Tcdh	5	-	-	ns	
SCLK Low time	Tcl	25	-	-	ns	
SCLK High time	Tch	25	-	-	ns	
SCLK rise and fall time	Tr, Tf	-	-	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	Tcc	10	-	-	ns	
Last SCLK edge to $\overline{CS}$ rising edge	Tcch	10	-	-	ns	
$\overline{CS}$ inactive time	Tcwh	50	-	-	ns	
SCLK to SDO valid delay time	Tcdv	-	-	5	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO High Z	Tcdz	-	10	-	ns	

1. Typical figures are at 25 C° and are for design aid only; not guaranteed and not subject to production testing.

Figure 30. Serial Input Timing

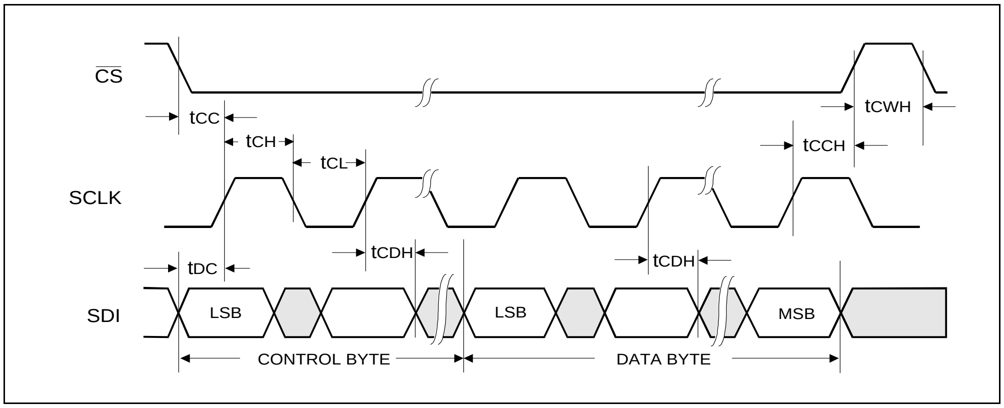


Figure 31. Serial Output Timing

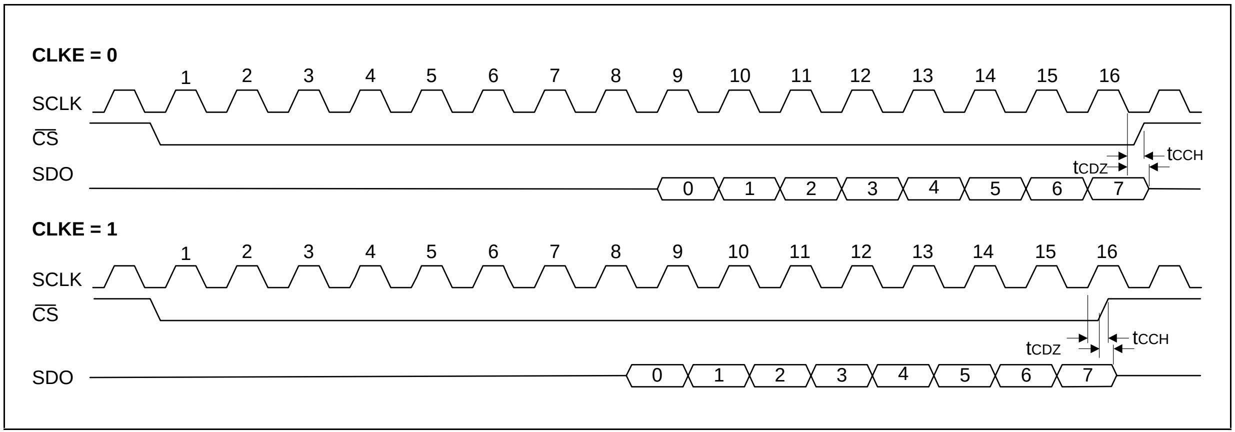


Table 56. Transformer Specifications[3]

Tx/Rx	Turns Ratio[1]	Primary Inductance mH (min.)	Leakage Inductance µH (max.)	Interwinding Capacitance pF (max.)	DCR Ω (max.)	Dielectric Breakdown Voltage V[2] (min.)
TX	1:2	1.2	0.60	60	0.70 pri 1.20 sec	1500 Vrms
RX	1:2	1.2	0.60	60	1.10 pri 1.10 sec	1500 Vrms

1. Transformer turns ratio accuracy is ± 2%.
2. This parameter is application dependent.LIU side: Line side.
3. Refer to the FAQ or Application Note “Transformer Specification for Intel® Transceiver Applications “ for recommended magnetics.

Table 57. G.703 2.048 Mbit/s Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 32. E1, G.703 Mask Templates

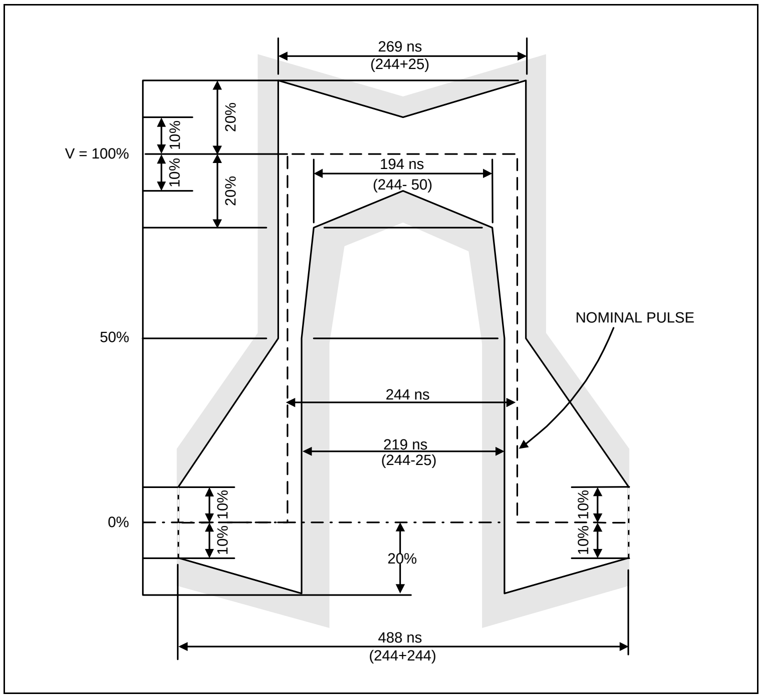


Table 58. T1.102 1.544 Mbit/s Pulse Mask Specifications

Parameter	Cable	Unit
	TWP	
Test load impedance	100	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ±0.15	V
Nominal pulse width	324	ns
Ratio of positive and negative pulse amplitudes	95-105	%

Figure 33. T1, T1.102 Mask Templates

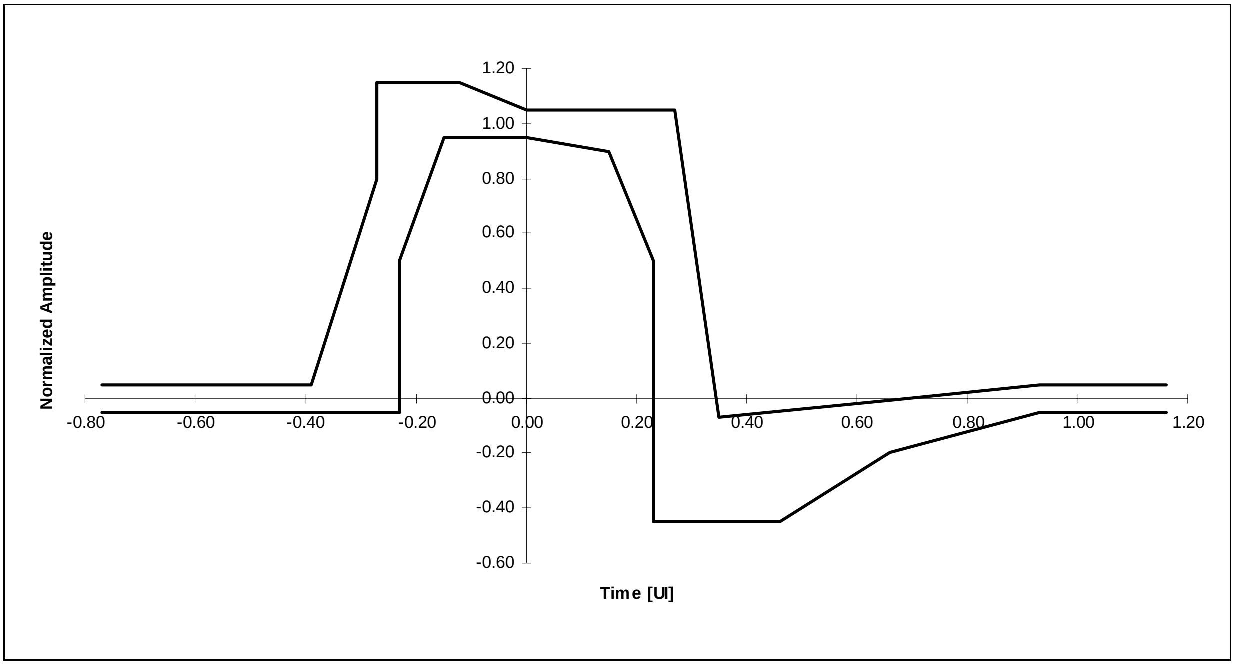


Figure 34. Jitter Tolerance Performance

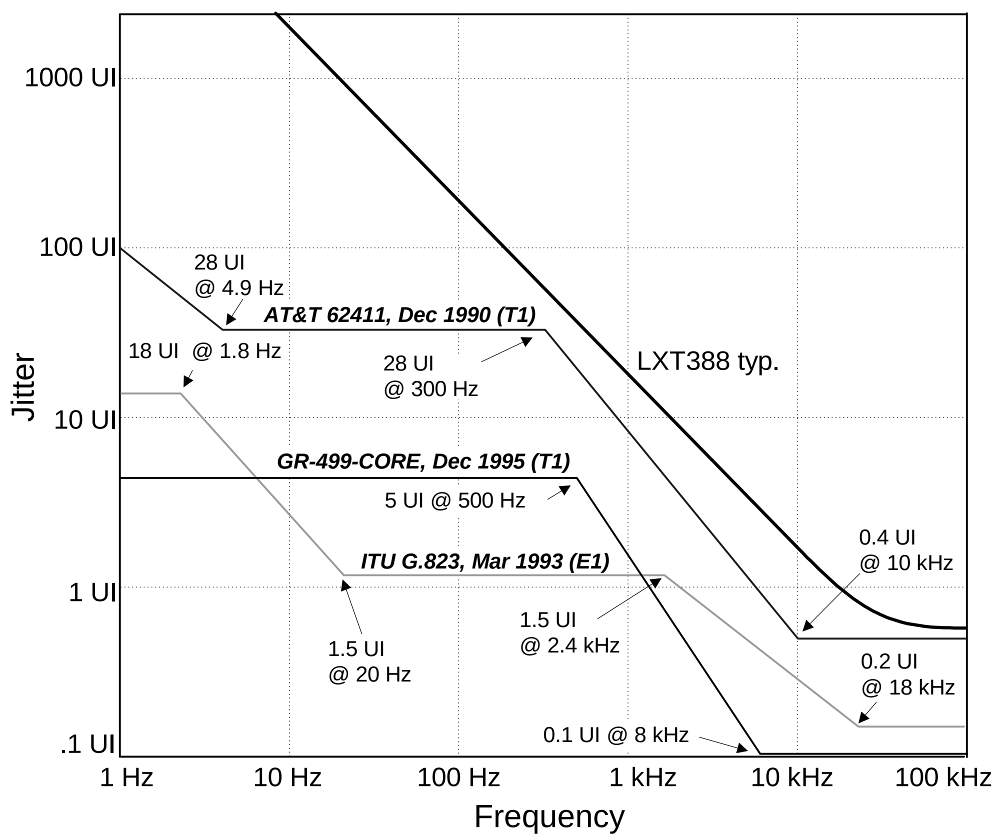


Figure 35. Jitter Transfer Performance

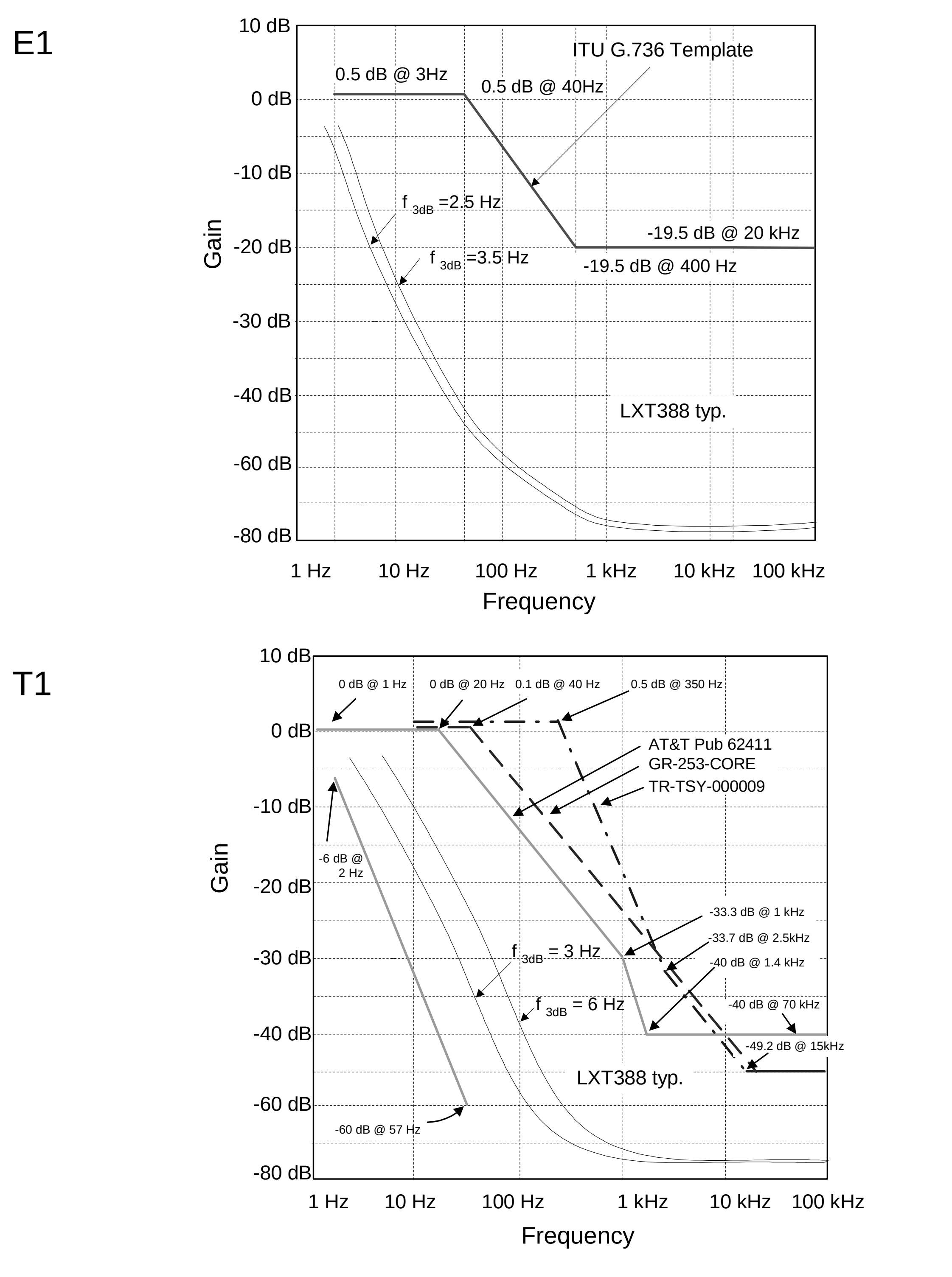
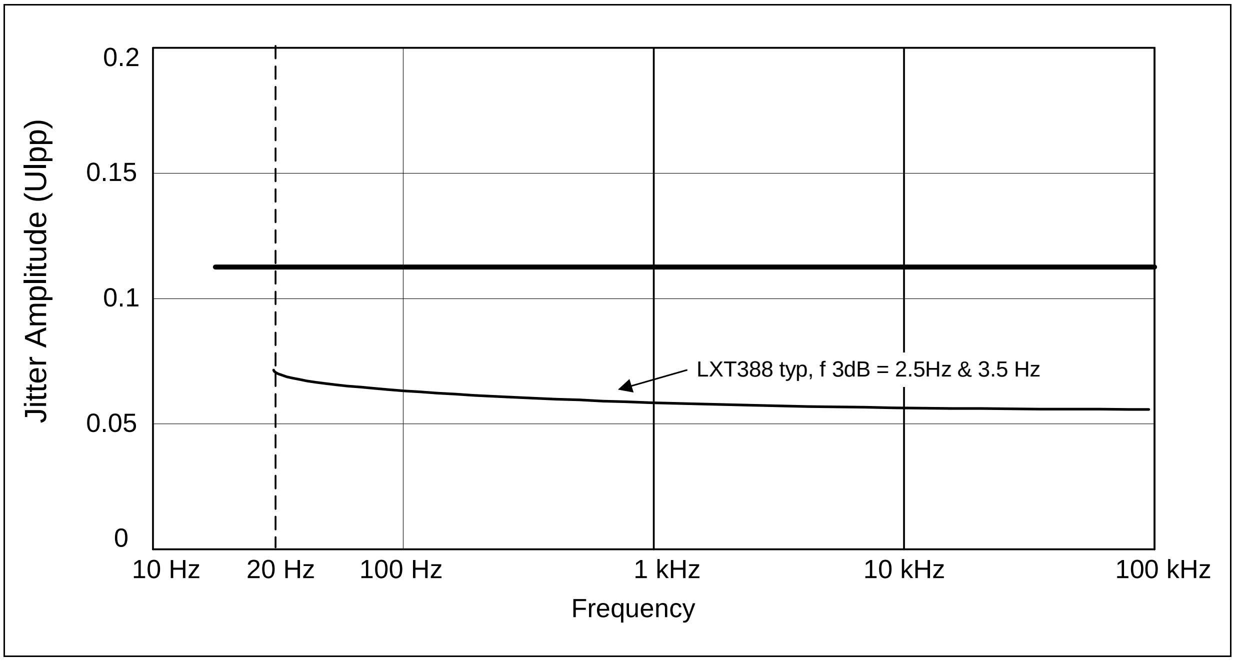


Figure 36. Output Jitter for CTR12/13 applications



5.1 Recommendations and Specifications

AT&T	Pub 62411
ANSI T1.102 -	199X Digital Hierarchy Electrical Interface
ANSI T1.231 -	1993 Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring
Bellcore	TR-TSY-000009 Asynchronous Digital Multiplexes Requirements and Objectives
Bellcore	GR-253-CORE SONET Transport Systems Common Generic Criteria
Bellcore	GR-499-CORE Transport Systems Generic Requirements
G.703	Physical/electrical characteristics of hierarchical digital interfaces
G. 704	Functional characteristics of interfaces associated with network nodes
G.735	Characteristics of Primary PCM multiplex equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
G.736	Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
G.772	Protected Monitoring Points provided on Digital Transmission Systems
G.775	Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria
G.783	Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks
G.823	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
O.151	Specification of instruments to measure error performance in digital systems
	OFTEL OTR-001 Short Circuit Current Requirements
ETS 300166	Physical and Electrical Characteristics
ETS 300386-1	Electromagnetic Compatibility Requirement

6.0 Mechanical Specifications

Figure 37. Low Quad Flat Package (LQFP) Dimensions

100 Pin LQFP

- Part Number LXT388LE
- Extended Temperature Range (-40°C to 85° C)

ALL DIMENSIONS IN MILLIMETERS

All dimensions and tolerances conform to ANSI Y14.5M-1982.