4 x 8-bit Multilevel Pipeline Register — L29C520/521

FEATURES

- Four 8-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD AM29520 and AM29521
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC (Type C)

DESCRIPTION

The Logic Devices **L29C520** and **L29C521** are pin-for-pin compatible with the Advanced Micro Devices AM29520 and AM29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the L29C520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The L29C521 devices differ from the L29C520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1

I_1	I_0	L29C520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

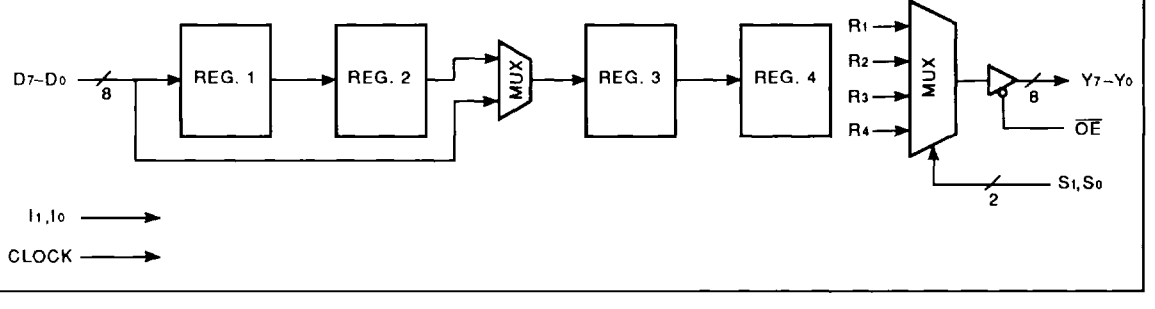
TABLE 2

I_1	I_0	L29C521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

L29C520/521 BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6.5 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

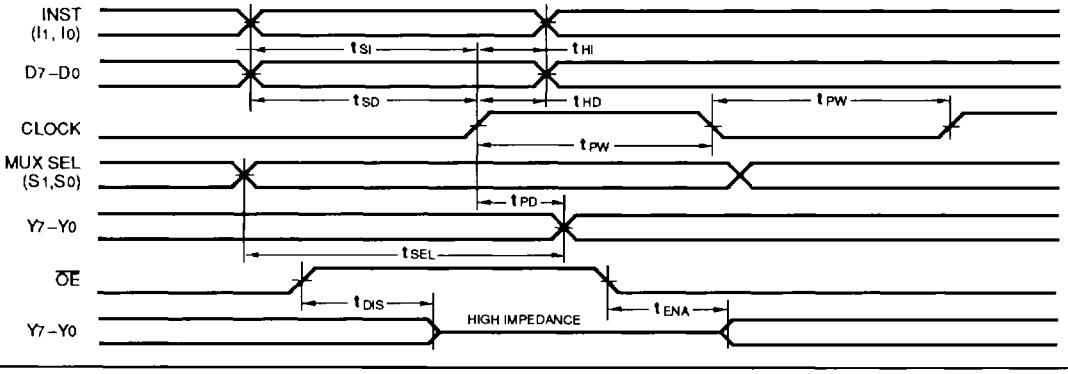
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C520/521-			
		25		22	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0		25		22
t_{SEL}	S_1,S_0 to Y_7–Y_0		25		20
t_{SD}	D_7–D_0 to CLK Setup	13		10	
t_{HD}	CLK to D_7–D_0 Hold	3		3	
t_{SI}	I_1,I_0 to CLK Setup	13		10	
t_{HI}	CLK to I_1,I_0 Hold	3		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21
t_{PW}	Clock Pulse Width	10		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C520/521-			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	CLK to Y_7–Y_0		30		24
t_{SEL}	S_1,S_0 to Y_7–Y_0		30		22
t_{SD}	D_7–D_0 to CLK Setup	15		10	
t_{HD}	CLK to D_7–D_0 Hold	5		3	
t_{SI}	I_1,I_0 to CLK Setup	15		10	
t_{HI}	CLK to I_1,I_0 Hold	5		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22
t_{PW}	Clock Pulse Width	15		10	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

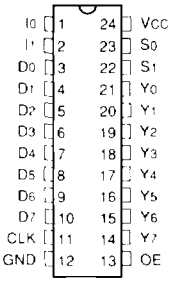
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

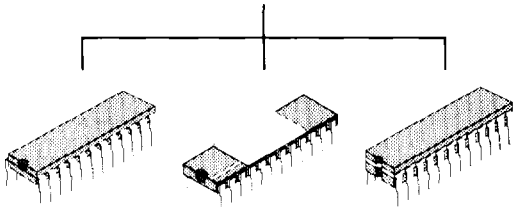
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

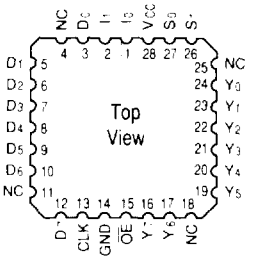
ORDERING INFORMATION

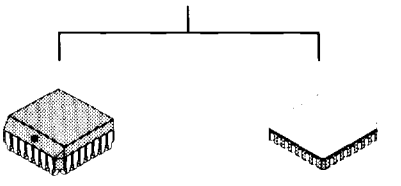
24-pin
(0.3" wide)





28-pin





Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening				
25 ns 22 ns	L29C520PC – 25 / 22 or L29C521PC	L29C520DC – 25 / 22 or L29C521DC	L29C520CC – 25 / 22 or L29C521CC	L29C520JC – 25 / 22 or L29C521JC	L29C520KC – 25 / 22 or L29C521KC
	–55°C to +125°C — Commercial Screening				
30 ns 24 ns		L29C520DM – 30 / 24 or L29C521DM	L29C520CM – 30 / 24 or L29C521CM		L29C520KM – 30 / 24 or L29C521KM
	–55°C to +125°C — Extended Screening				
30 ns 24 ns		L29C520DME – 30 / 24 or L29C521DME	L29C520CME – 30 / 24 or L29C521CME		L29C520KME – 30 / 24 or L29C521KME
	–55°C to +125°C — MIL-STD-883 Compliant				
30 ns 24 ns		L29C520DMB – 30 / 24 or L29C521DMB	L29C520CMB – 30 / 24 or L29C521CMB		L29C520KMB – 30 / 24 or L29C521KMB

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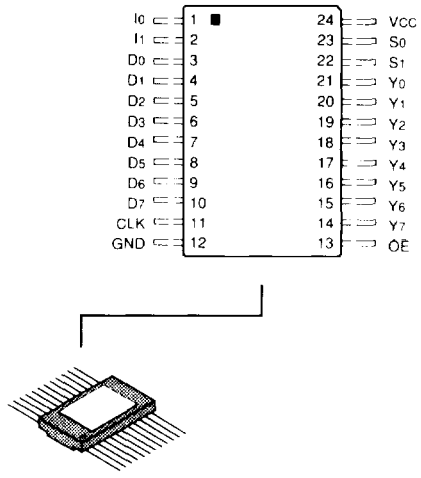
ORDERING INFORMATION

24-pin



Speed	Flatpack (F1)		
	0°C to +70°C — Commercial Screening		
25 ns 22 ns	L29C520FC or L29C521FC — 25 / 22		
	–55°C to +125°C — Commercial Screening		
30 ns 24 ns	L29C520FM or L29C521FM — 30 / 24		
	–55°C to +125°C — Extended Screening		
30 ns 24 ns	L29C520FME or L29C521FME — 30 / 24		
	–55°C to +125°C — MIL-STD-883 Compliant		
30 ns 24 ns	L29C520FMB or L29C521FMB — 30 / 24		