



Description

The GM76C28A is 2,048 words x 8 bits asynchronous, static random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

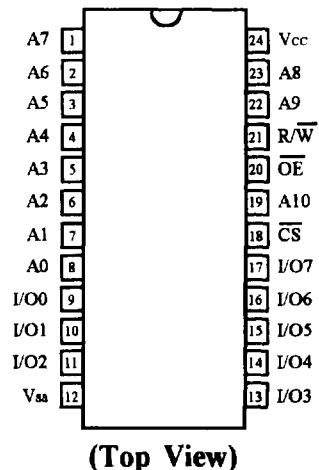
Features

- Access time : 100/120ns
- Low Power Consumption
Standby : 1 μ A (Typ.)
Operation : 25/30mA (Typ.)
- Complete static operation
- Single power supply : 5V $\pm$ 10%
- TTL compatible inputs and outputs
- 3-state output with Wired-OR capability
- Non-volatile storage with back-up batteries
- Standard 24 DIP, 24 SOP and 24 S-DIP

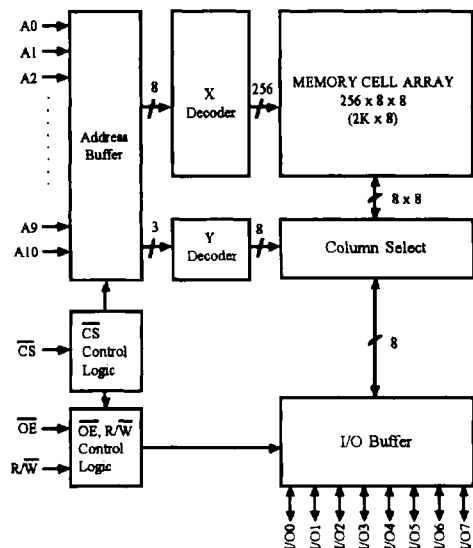
Pin Description

Pin	Function
A0-A10	Address Inputs
R/W	Read/Write
OE	Output Enable
CS	Chip Select
I/O0-I/O7	Data Input/Output
Vcc	Power Supply (+5V)
Vss	Ground

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	℃
T _{STO}	Storage Temperature	-65 ~ 150	℃
V _{IN} /V _{OUT}	Voltage on any Pin Relative to V _{SS}	-0.5 ~ 7.0	V
P _D	Power Dissipation	1.0	W

*Note: Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{HI}	Input High Voltage	2.2	-	6.0	V
V _{LI}	Input Low Voltage	-0.5	-	0.8	V

*All voltages are referenced to V_{SS} pin = 0V.

Truth Table

$\overline{CS}$	$\overline{OE}$	R/ $\overline{W}$	A0 to A10	DATA I/O	MODE	I _{CC}
H	X	X	X	Hi-Z	Unselected	I _{CC1} , I _{CC2}
L	L	H	Stable	Output Data	Read	I _{CC}
L	H	L	Stable	Input Data	Write	I _{CC}
L	L	L	Stable	Input Data	Write	I _{CC}

*Note: X means "H", "L" or "Hi-Z"

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter	Conditions	GM76C28A-10			GM76C28A-12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
V _{OL}	Low Level Output Voltage	I _{OL} = 4.0mA			0.4			0.4	V
V _{OH}	High Level Output Voltage	I _{OH} = -1.0mA	2.4			2.4			V
I _{CC1}	Operation Supply Current	$\overline{CS} = V_{LI}$, I _{VO} = 0mA		30	60		25	50	mA
I _{CC2}		V _{HI} = 3.5V, V _{LI} = 0.6V, I _{VO} = 0mA		16			16		mA
I _{CC}	Average Operating Current	Min cycle, duty=100%, I _{VO} = 0mA		30	60		25	50	mA
I _{CC1}	Standby Supply Current	$\overline{CS} = V_{HI}$		1.5	3.0		1.5	3.0	mA
I _{CC2}		$\overline{CS} = V_{CC} - 0.2V$		1	50		1	50	μA
I _{IL}	Input Leakage Current	V _{CC} = 5.5V, V _I = 0 to V _{CC}	-1		1	-1		1	μA
I _{OO}	Output Leakage Current	$\overline{CS} = V_{HI}$, or $\overline{OE} = V_{HI}$, V _{VO} = 0 to V _{CC}	-1		1	-1		1	μA

*Typical values are for reference with V_{CC} = 5V and T_A = 25℃ assumed.

AC Operating Characteristics

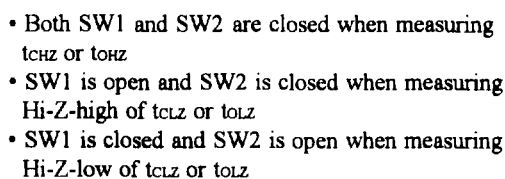
Read Cycle ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ\text{C}$)

Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	100		120		ns
t_{AA}	Address Access Time			100		120	ns
t_{ACS}	$\overline{CS}$ Access Time			100		120	ns
t_{OE}	$\overline{OE}$ Access Time			55		60	ns
t_{OH}	Output Hold Time		10		10		ns
t_{CLZ}	$\overline{CS}$ Output Set-up Time	*2	10		10		ns
t_{OLZ}	$\overline{OE}$ Output Set-up Time		5		10		ns
t_{CHZ}	$\overline{CS}$ Output Floating		0	40	0	40	ns
t_{OHZ}	$\overline{OE}$ Output Floating		0	40	0	40	ns

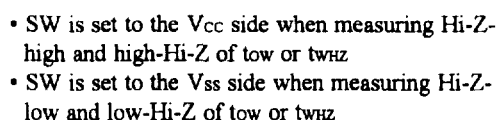
Write Cycle ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ\text{C}$)

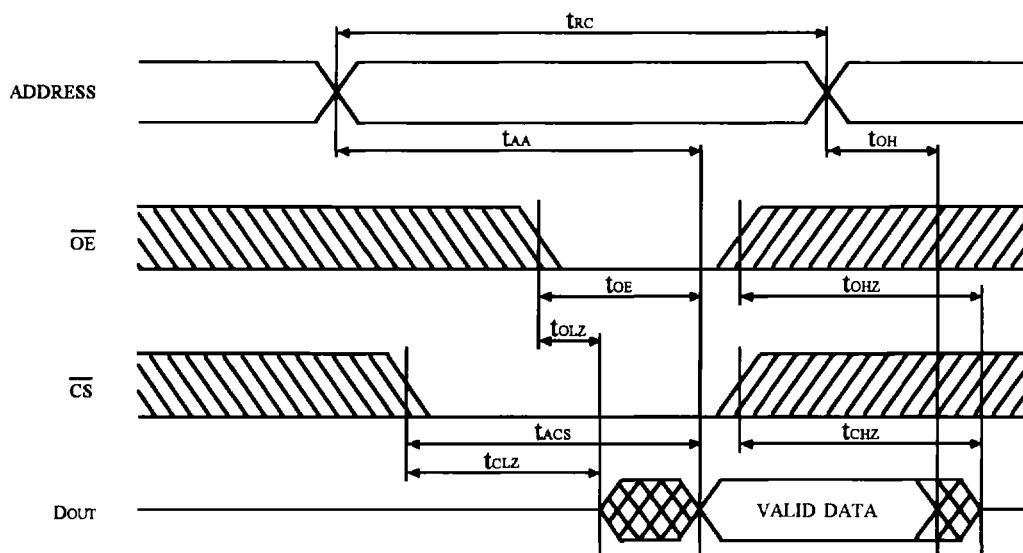
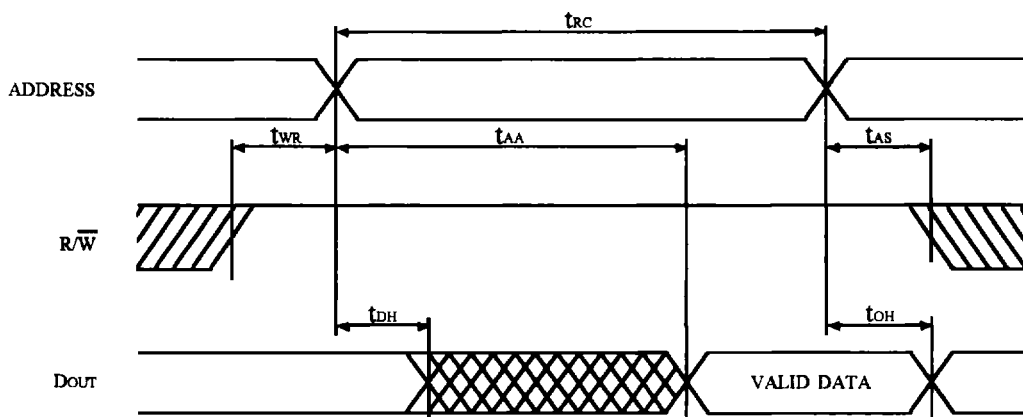
Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	100	-	120	-	ns
t_{CW}	Chip Select Time ($\overline{CS}$)		80	-	85	-	ns
t_{AW}	Address Enable Time		80	-	85	-	ns
t_{AS}	Address Set-up Time		0	-	0	-	ns
t_{WP}	Write Pulse Width		65	-	70	-	ns
t_{WR}	Address Hold Time		0	-	0	-	ns
t_{DW}	Input Data Set-up Time		45	-	50	-	ns
t_{DH}	Input Data Hold Time		0	-	0	-	ns
t_{WIZ}	$R/\overline{W}$ Output Floating	*3	0	45	0	50	ns
t_{OW}	$R/\overline{W}$ Output Setup Time		5	-	10	-	ns

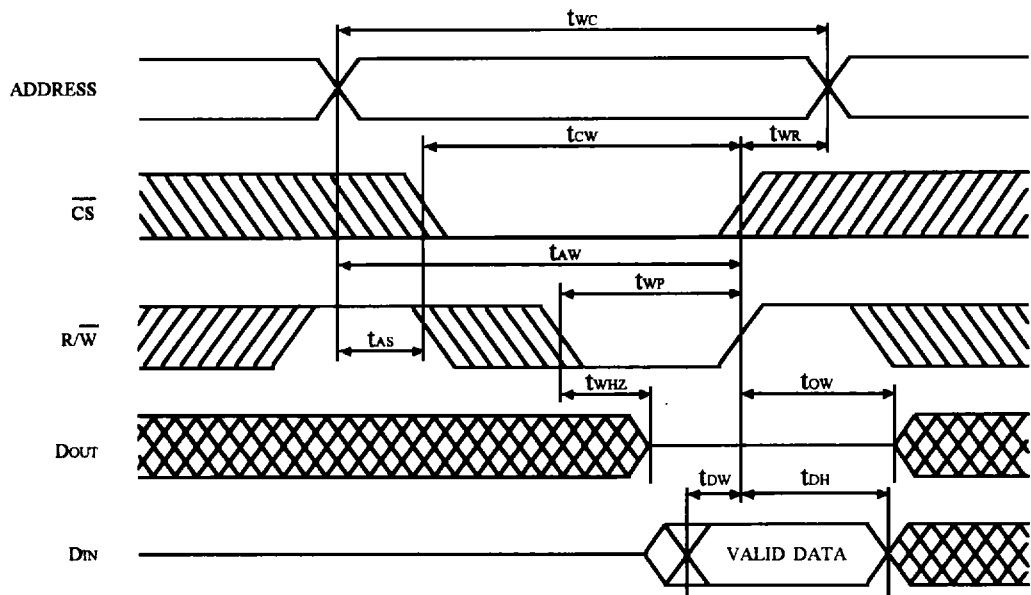
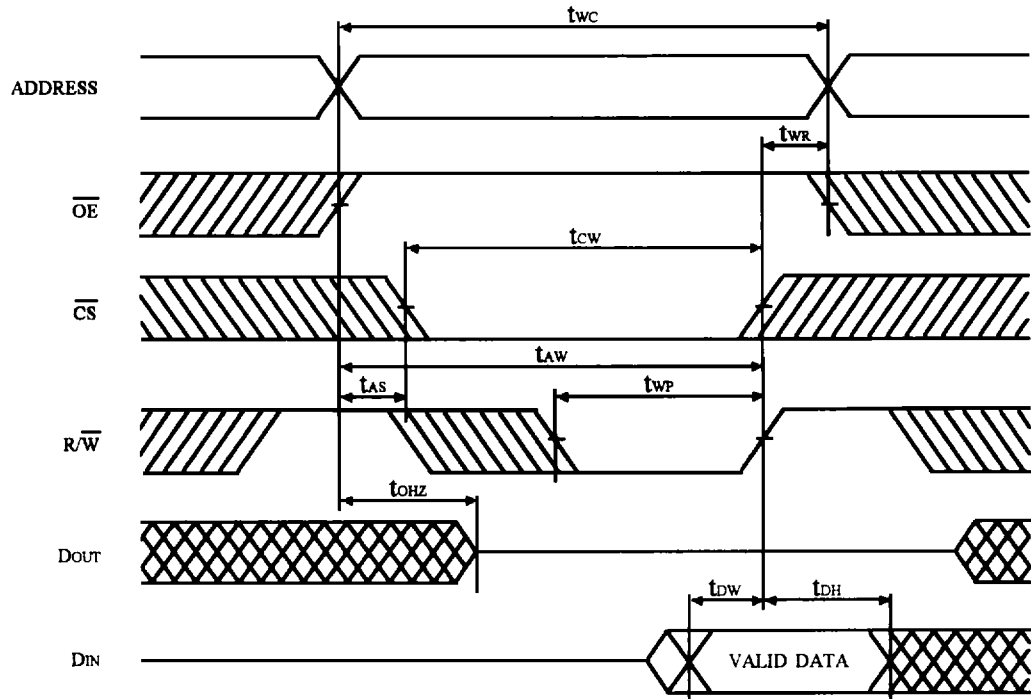
1. Input pulse level : 0.8V to 2.2V
2. $t_r = t_f = 10\text{ns}$
3. Test circuit

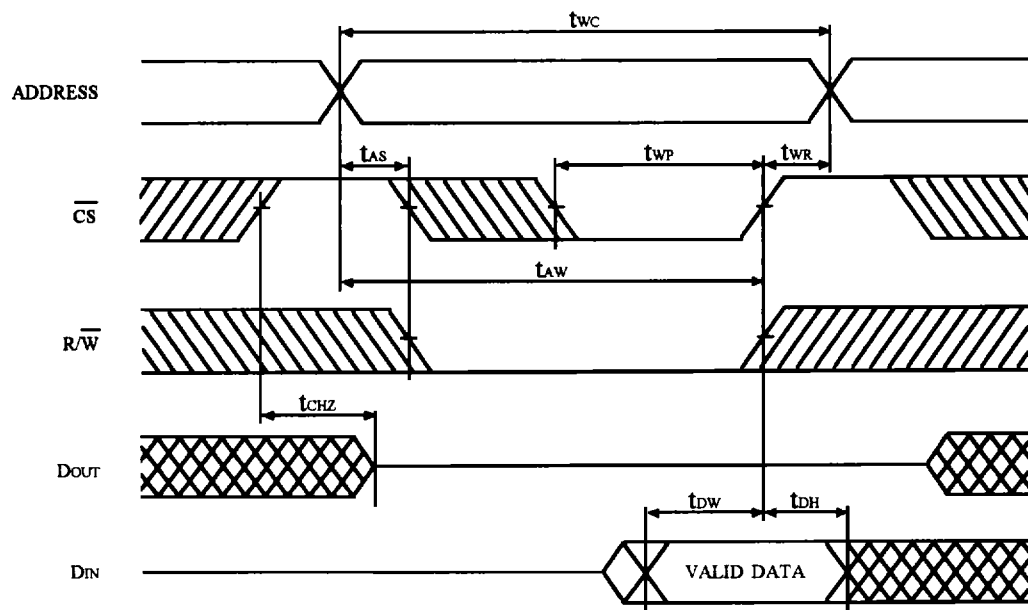


1. Input pulse level : 0.8V to 2.2V
2. $t_r = t_f = 10\text{ns}$
3. Test circuit



READ CYCLE 1 ($\overline{OE}$, $\overline{CS}$ CONTROL, $R/\overline{W}$ = HIGH)**READ CYCLE 2 ($R/\overline{W}$ CONTROL, $\overline{OE}$ = LOW, $\overline{CS}$ = LOW)**

WRITE CYCLE 1 (R/W CONTROL, $\overline{OE} = \text{LOW}$)**WRITE CYCLE 2 (R/W CONTROL)**

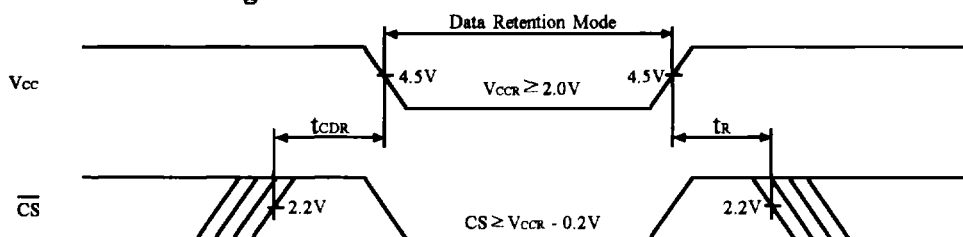
WRITE CYCLE 3 ($\overline{\text{CS}}$ CONTROL, $\overline{\text{OE}} = \text{LOW}$)

Capacitance ($f = 1\text{MHz}$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	Input Capacitance	$V_i = 0\text{V}$	-	4	6	pF
C_{io}	I/O Capacitance	$V_{io} = 0\text{V}$	-	6	8	pF

Data Retention Characteristics ($T_A = 0 \sim 70^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	-	5.5	V
I_{CCR}	Data Retention Current	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq 2.8\text{V}$	-	-	25	μA
t_{CDR}	Chip Select Data Hold Time	Refer to the figure below	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}^*	-	-	ns

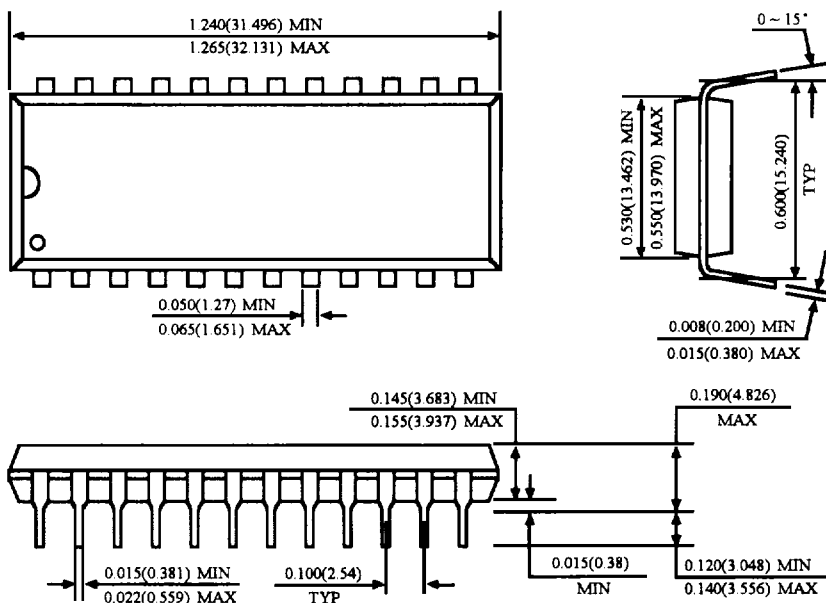
* t_{RC} : read cycle time**Data Retention Timing**

*Note: When retaining data in standby mode, supply voltage can be lowered within a certain range.
 Read or write cycle cannot be performed while the supply voltage is low.

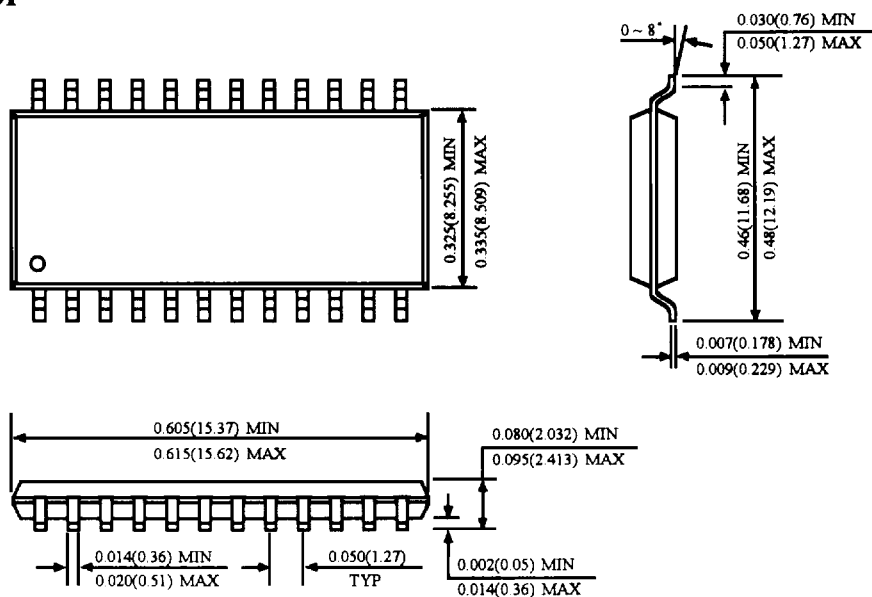
Package Dimensions

Unit: Inches (mm)

24 DIP



24 SOP



Unit: Inches (mm)

24 SKINNY DIP

