PRELIMINARY

CY7C109D
CY7C1009D

1-Mbit (128K x 8) Static RAM

Features

- **Pin- and function-compatible with CY7C109B/CY7C1009B**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— I_{CC} = 60 mA @ 10 ns**
- **Low CMOS standby power**
  - **— I_{SB2} = 1.2 mA ('L' Version only)**
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**
- **Available in Pb-Free Packages**

Functional Description[1]

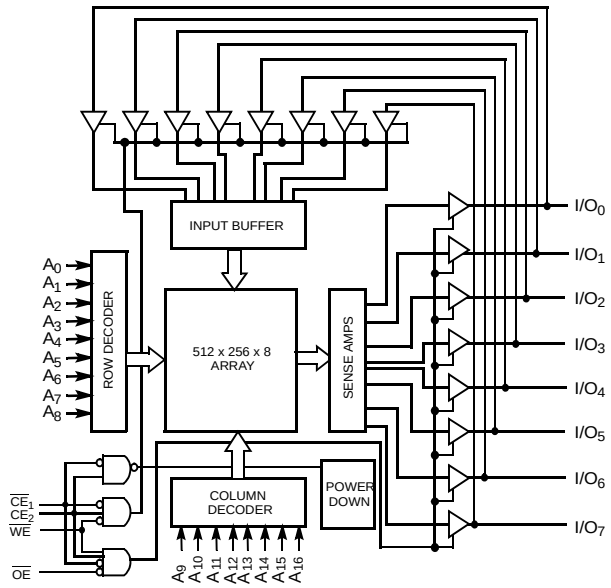
The CY7C109D/CY7C1009D is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

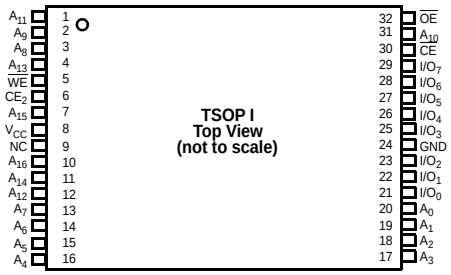
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

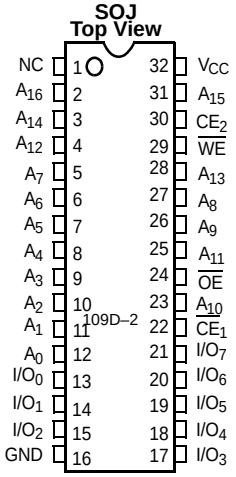
The CY7C109D is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009D is available in a 300-mil-wide SOJ Pb-Free package. The CY7C1009D and CY7C109D are functionally equivalent in all other respects.

Logic Block Diagram



Pin Configurations





Selection Guide

		CY7C109D-10 CY7C1009D-10	CY7C109D-12 CY7C1009D-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current		60	50	mA
Maximum CMOS Standby Current	Non-L Com'l / Ind'l	3	3	mA
	Low Power Version	1.2	1.2	

Note:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[2] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C109D-10 7C1009D-10 Min.	7C109D-10 7C1009D-10 Max.	7C109D-12 7C1009D-12 Min.	7C109D-12 7C1009D-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			60		50	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}			10		10	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ – 0.3V, or $CE_2 \leq$ 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f = 0			3		3	mA
			L		1.2		1.2	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		8	pF

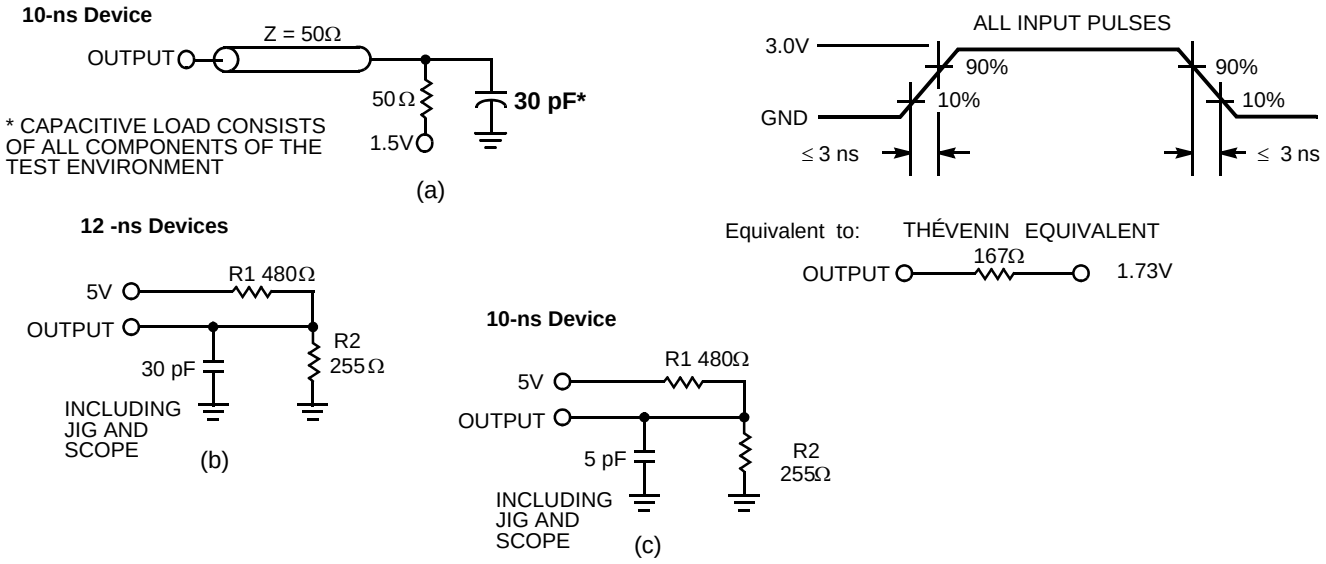
Thermal Resistance[4]

Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[4]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[4]		TBD	°C/W

Notes:

2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C109D-10 7C1009D-10		7C109D-12 7C1009D-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}[5]	V_{CC}(typical) to the first access	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		5		6	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[8, 9]		5		6	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		10		12	ns
Write Cycle[10]						
t_{WC}	Write Cycle Time[11]	10		12		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	8		10		ns
t_{AW}	Address Set-Up to Write End	7		10		ns

Notes:

5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

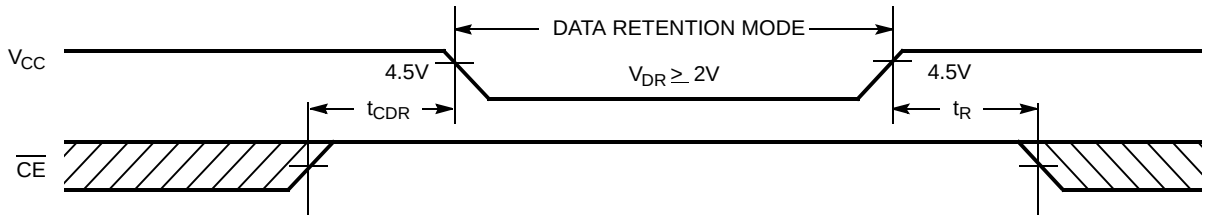
Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C109D-10 7C1009D-10		7C109D-12 7C1009D-12		Unit
		Min.	Max.	Min.	Max.	
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		10		ns
t_{SD}	Data Set-Up to Write End	6		7		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		6		6	ns

Data Retention Characteristics Over the Operating Range

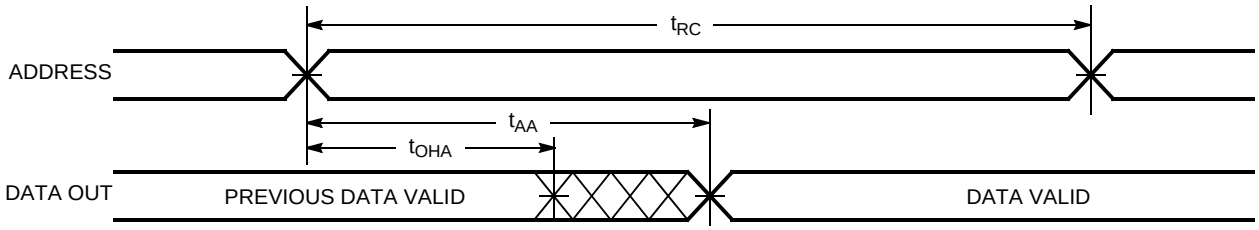
Parameter	Description		Conditions	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		$\overline{V_{CC}} = V_{DR} = 2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l / Ind'l			3	mA
		L-Version Only			1.2	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[6]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Switching Waveforms

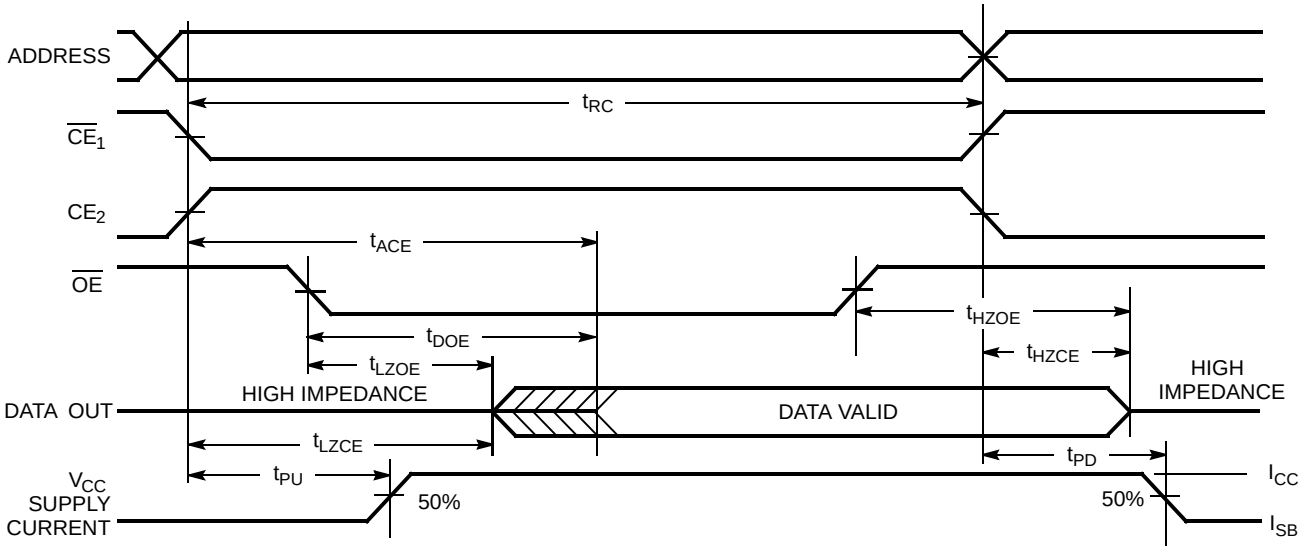
Read Cycle No. 1[12, 13]



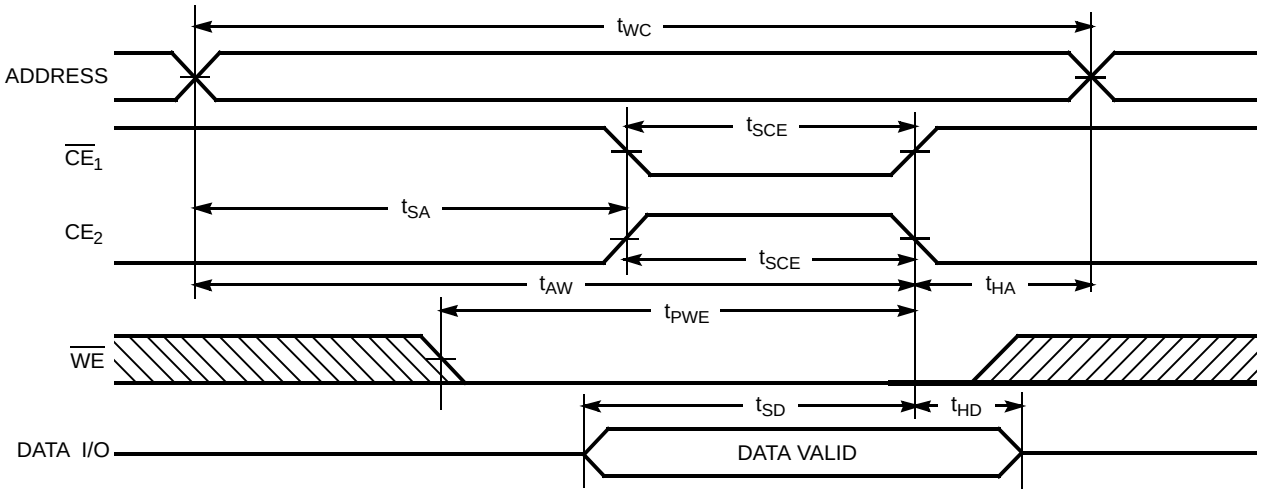
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



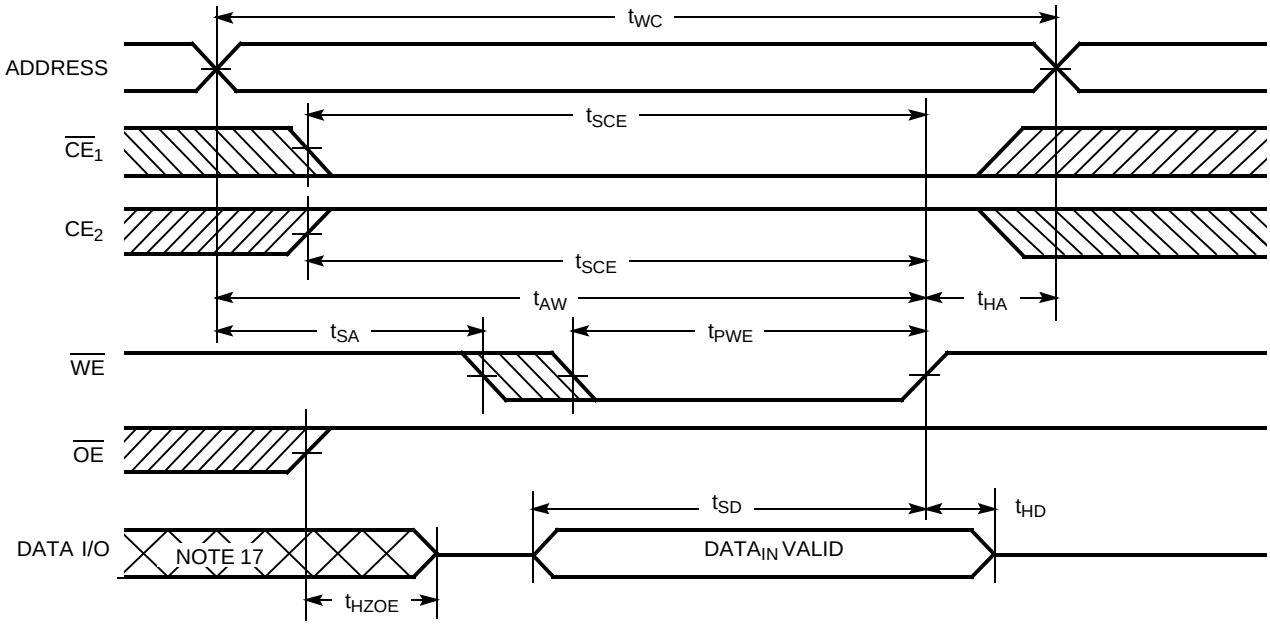
Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[15, 16]



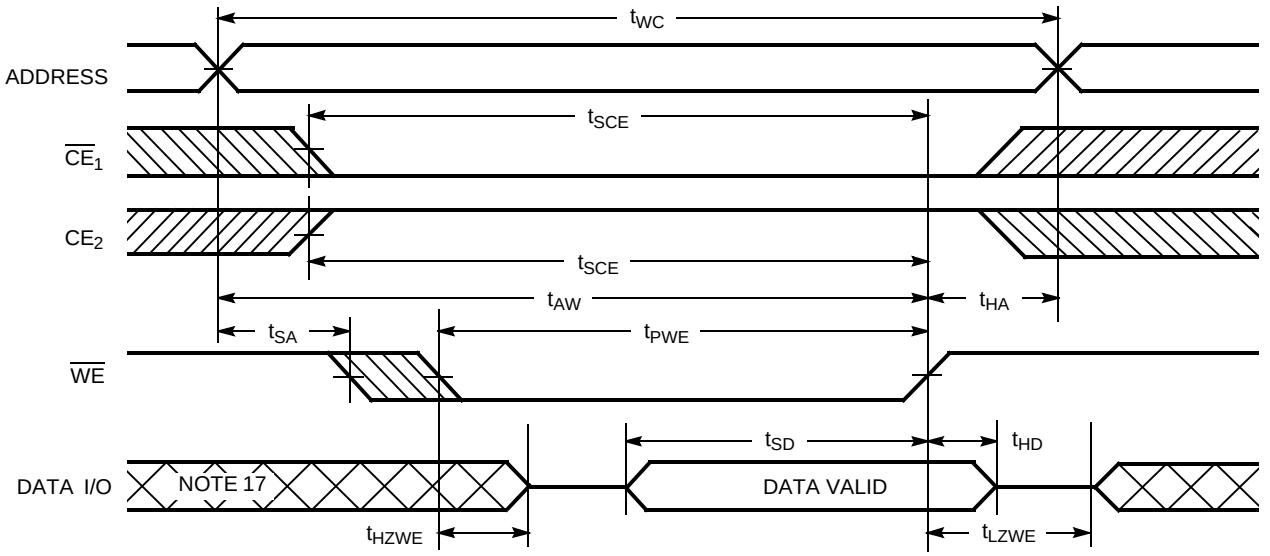
Notes:
14. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Note:
17. During this period the I/Os are in the output state and input signals should not be applied.

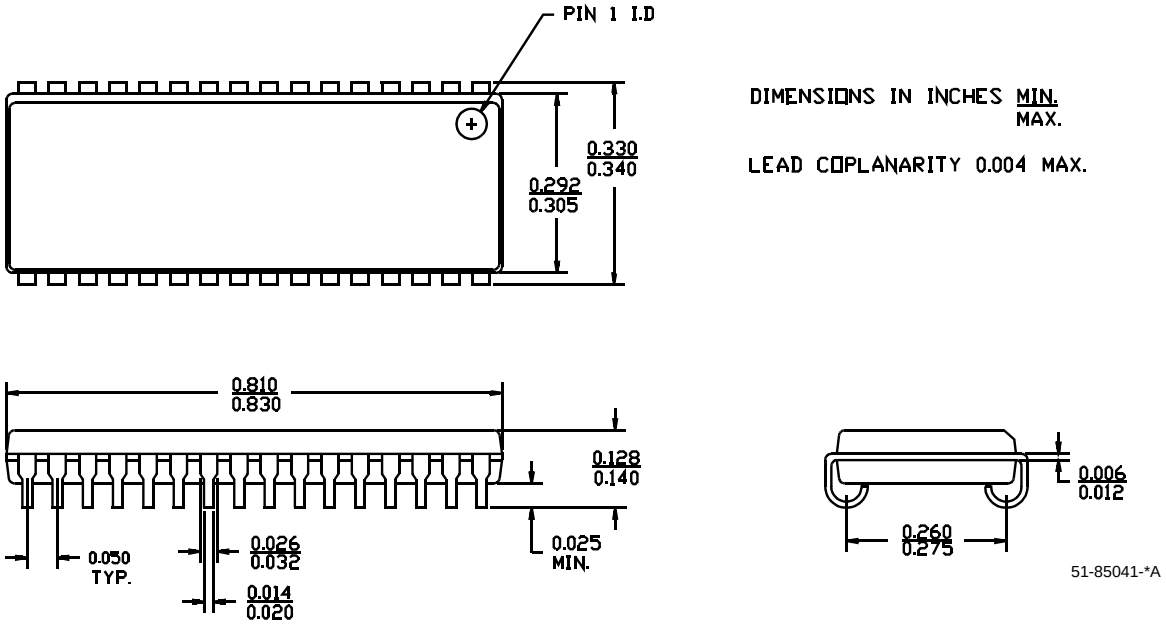
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C109D-10VXC	V33	32-Lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1009D-10VXC	V32	32-Lead (300-Mil) Molded SOJ (Pb-Free)	
	CY7C109D-10ZXC	Z32	32-Lead TSOP Type I (Pb-Free)	
	CY7C109D-10VXI	V33	32-Lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1009D-10VXI	V32	32-Lead (300-Mil) Molded SOJ (Pb-Free)	
	CY7C109D-10ZXI	Z32	32-Lead TSOP Type I (Pb-Free)	
12	CY7C109D-12VXC	V33	32-Lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1009D-12VXC	V32	32-Lead (300-Mil) Molded SOJ (Pb-Free)	
	CY7C109D-12ZXC	Z32	32-Lead TSOP Type I (Pb-Free)	
	CY7C109D-12VXI	V33	32-Lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1009D-12VXI	V32	32-Lead (300-Mil) Molded SOJ (Pb-Free)	
	CY7C109D-12ZXI	Z32	32-Lead TSOP Type I (Pb-Free)	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

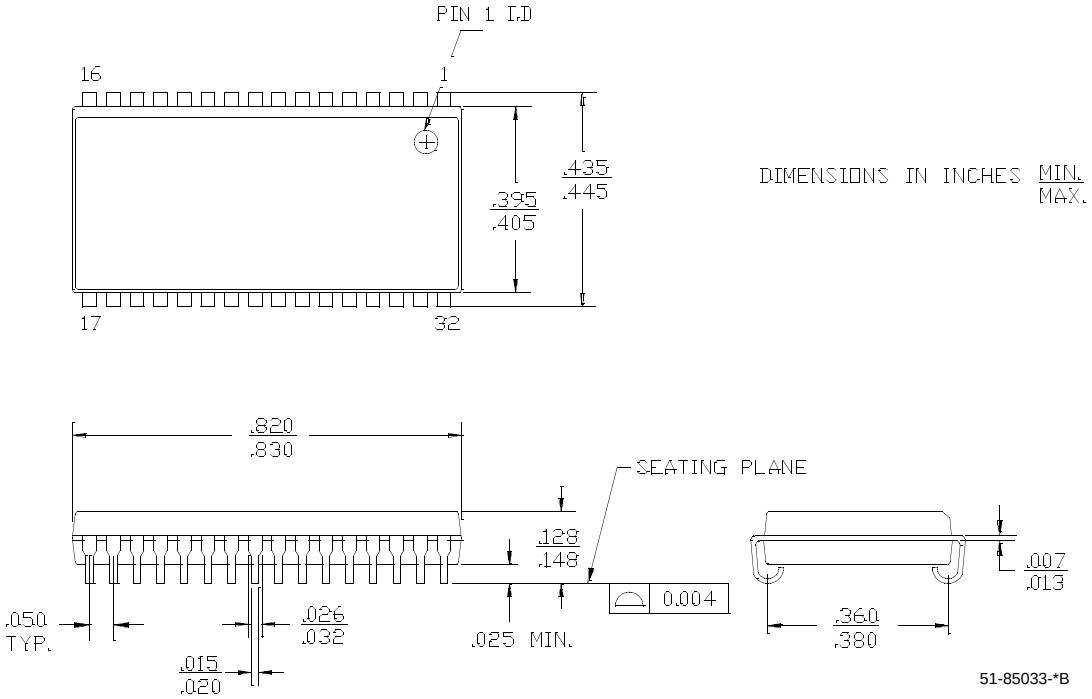
Package Diagrams

32-Lead (300-Mil) Molded SOJ V32

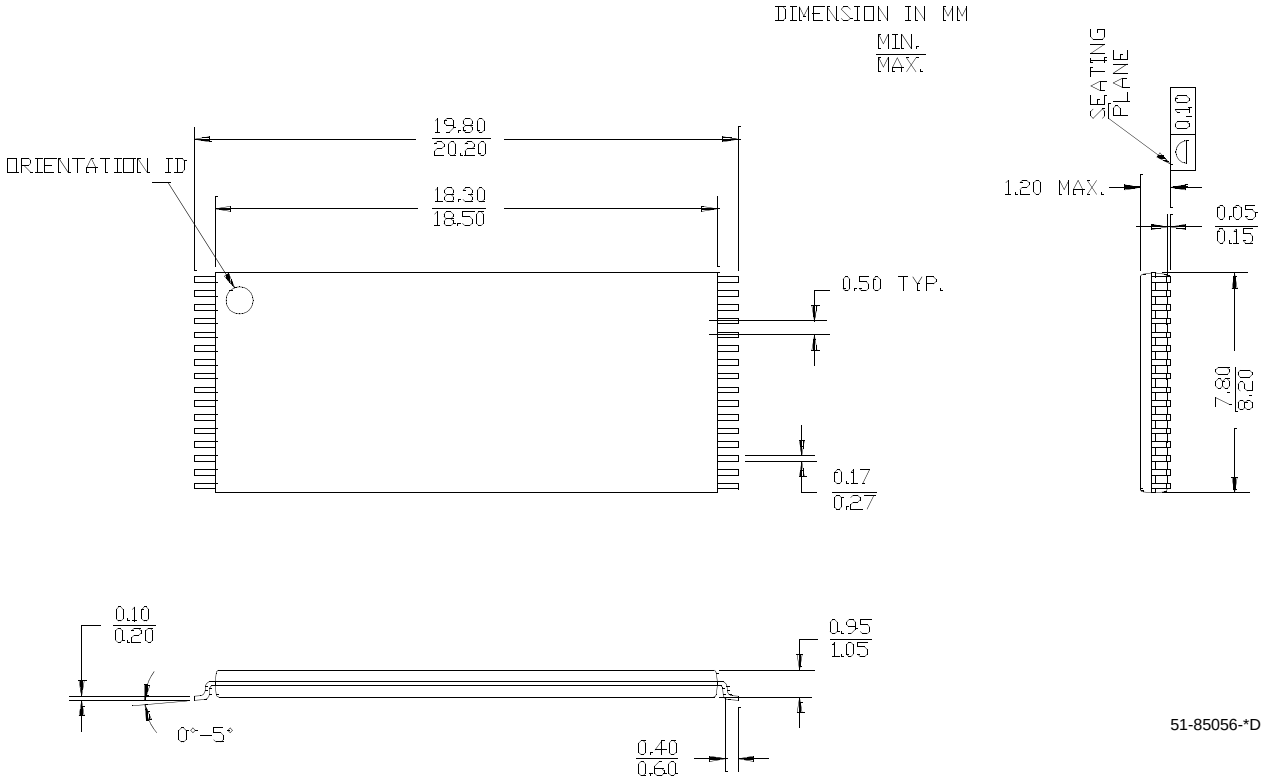


Package Diagrams (continued)

32-Lead (400-Mil) Molded SOJ V33



32-Lead Thin Small Outline Package Type I (8x20 mm) Z32



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Document History Page

Document Title: CY7C109D, CY7C1009D 1-Mbit (128K x 8) SRAM (Preliminary) Document Number: 38-05468				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307596	See ECN	RKF	Reduced Speed bins to -10 and -12 ns